Errata

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HP References in this Manual

This manual may contain references to HP or Hewlett-Packard. Please note that Hewlett-Packard's former test and measurement, semiconductor products and chemical analysis businesses are now part of Agilent Technologies. We have made no changes to this manual copy. The HP XXXX referred to in this document is now the Agilent XXXX. For example, model number HP8648A is now model number Agilent 8648A.

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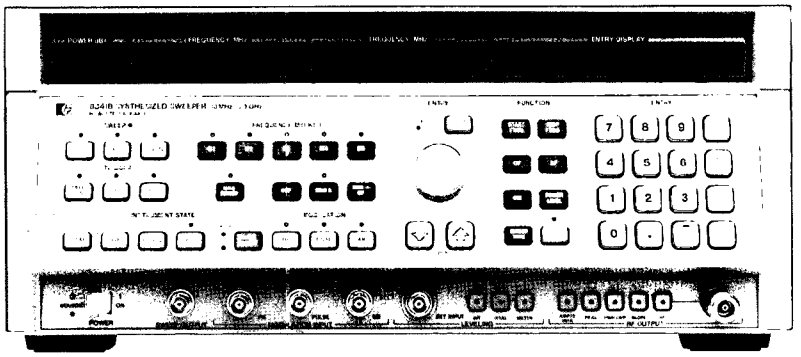
ASSEMBLY LEVEL SERVICE MANUAL

HP 8341B OPTION 003 SYNTHESIZED SWEEPER

10 MHz to 20 GHz



HEWLETT PACKARD

HP 8341B OPTION 003
SYNTHESIZED SWEEPER
10 MHz to 20 GHz
(Including Option 004)

SERIAL NUMBERS

This manual applies directly to the HP 8341B Option 003 Synthesized Sweeper prefixed 2745A.

For additional information about serial numbers, refer to INSTRUMENTS COVERED BY THE MANUAL in Section I.

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HP 8341B Option 003 Assembly-Level Service

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Assembly-Level Service Introduction

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HP 8341B Option 003 Assembly-Level Service Introduction

This volume provides assembly-level troubleshooting information for the HP 8341B Option 003 synthesized sweeper (to be known as, the SOURCE or DUT).

The introduction provides information on:

- Manual format.
- The tools required to service the instrument.
- Interconnect cables and mnemonics.
- Overall instrument theory and troubleshooting.

MANUAL FORMAT

This service volume is divided into subsections based on functional groups. The first major subsection A, Assembly-Level Service Introduction, contains the information that applies to the whole instrument. Such as:

Overall Instrument Theory

This portion details overall instrument theory of operation, and includes an overall instrument block diagram.

Calibration Constants

This is a description of the instrument's stored calibration constants.

Troubleshooting Aids

This part of the service section contains descriptions of the troubleshooting aids built into the instrument:

- The instrument self-test
- Front panel diagnostics.

Overall Instrument Troubleshooting

This troubleshooting guide begins with a symptom and leads you to one of the eight major functional areas of the instrument (see below). In some cases, this guide leads you directly to the faulty assembly.

Repair

This portion contains cautions concerning the repair of the SOURCE. Please read these cautions. They contain important notices concerning personal safety and instrument repair.

This portion also contains a description of the module exchange program, and after-service safety checks.

The subsections that follow contain information that is specific to a functional group.

Major Functional Groups

A functional group is a group of assemblies and/or microcircuits that work together to perform a task. There are eight such groups in this instrument:

- Reference M/N loops
- 20-30 (phase lock) loops
- Sweep generator – YO (YIG oscillator) loop
- Motherboard
- Controller (processor and related assemblies)
- Front/rear panel
- RF section
- Power supplies

A functional group provides assembly-level troubleshooting information. Each functional group section contains assembly-level theory of operation, block diagrams, troubleshooting information, and assembly-level replaceable parts.

NOTE: To avoid unnecessary troubleshooting, verify the internally stored calibration constants. If these constants have been incorrectly modified, the instrument can activate an error annunciator (see **CALIBRATION CONSTANTS**).

REQUIRED TOOLS

See Tables A-1 and A-2:

- Service Kit, HP part number 08340-60134
- A soldering iron with a grounded tip
- A low static solder removal tool
- Grounding wrist strap

Table A-1. Tools Supplied in Service Kit

Item	Description	HP Part Number
Adapters	3.5 mm Female to Female 3.5 mm Female to Type-N Male	5061-5311 1250-1744
Adapter Tee	SMB Male-Male-Male	1250-0670
PC Board Extenders	24-pin 30-pin 36-pin 44-pin 48-pin 62-pin 110-pin	08340-60095 08505-60041 08505-60042 08350-60031 08340-60050 08340-60096 08340-60033
IC Test Clip	16-pin 20-pin	1400-0734 1400-0979
Adjustment Tool	Fits adjustment slot on components	8830-0024
Service Cables	BNC (Male) to SMB (Female) (2 required) 61 mm (2 ft), 0.85 in., semi-rigid, SMA Male to SMA Male (2 required) 30 mm (12 in) SMB (Female) to SMB (Female)	85680-60093 08340-20124 5061-1022
Nut Driver	9/16 inch, to replace front panel BNC nuts	08340-20099
Wrench	5/16-inch slotted box/open end	08555-20097

Table A-2. Equipment Required but not Supplied in the Service Kit

Item	Description	HP Part Number
RMA Solder	Rosin Mildly Activated	8090-0587
EDSYN SILVERSTAT	Low static solder removal tool	8690-0227
Replacement Tip	For low-static solder removal tool	8690-0253
Wrist Strap	Anti-static wrist strap, 4 ft cord and alligator clip	9300-0791

INTERCONNECT CABLES AND MNEMONICS

All interconnect cables and their associated connectors are listed in the motherboard-wiring list functional group.

All signal mnemonics are defined, the point-to-point distribution of each signal to and from the PC board sockets and the cable connectors on the A62 motherboard assembly are referenced, and the assembly that generated the signal is defined in the motherboard-wiring list functional group.

Assembly-Level Service
Overall Instrument Theory

The **HP 8341B Option 003** is a synthesized sweeper that covers the frequency range from 10 MHz to 20.0 GHz, in four bands.

The instrument bands are:

- Band 0
  10 MHz to 2.3 GHz
- Band 1
  2.3 to 7.0 GHz
- Band 2
  7.0 to 13.5 GHz
- Band 3
  13.5 to 20.0 GHz

Internal to the instrument are 7 phase-lock loops, 17 high frequency microcircuits, and a 16-bit microprocessor.

REFERENCE LOOPS

Frequency accuracy and stability are tied to either the 10 MHz internal frequency standard or an external 5 or 10 MHz source. The reference loop uses this 10 MHz to generate all of the translation and reference signals used by other phase-lock loops in the instrument. These signals are:

- 400 MHz and 20 MHz signals used in the M/N loop to produce the M/N output frequency.
- 10 MHz and 100 MHz signals used as reference signals in the 20-30 loops.
- A separate, lower power 100 MHz output sent to the RF section to phase lock the 3.7 GHz oscillator to the 10 MHz reference.

M/N LOOP

The M/N loop produces an output between 177 and 197 MHz that drives a sampler in the YO loop. The variables M and N are integers generated by the processor, and control the output frequency of the M/N loop. The output from the sampler in the YO loop must always be between 20 and 30 MHz to be compared and phase locked to the output of the 20-30 phase lock loops.

With the YO at a specific frequency between 2.3 and 7.0 GHz, there is an M/N output frequency between 177 and 197 MHz. When a harmonic of this frequency is mixed with the YO frequency in the sampler, an IF output between 20 and 30 MHz results. The sampler output is then compared to the 20-30 loop output by the YO loop phase/frequency detector in the YO loop.

20-30 LOOPS

The 20-30 loops contain three phase-locked loops used together to provide the YO loop with 1 Hz CW resolution, and with analog sweep widths from 100 Hz to 5 MHz. For sweep widths of 5 MHz or less, the YO Loop remains phase-locked during the sweep, and the 20-30 Loop is swept the desired amount. For sweep widths greater than 5 MHz, all phase-lock loops lock at the beginning of sweep, the 20-30 Loop remains fixed, and the YO is swept. This is called lock and roll, and will be discussed later.

The 20-30 loop generates an output between 20 and 30 MHz in CW mode, and between 15 and 30 MHz when swept. This loop has an output resolution of 1 Hz. Comparing and locking the down-converted YO frequency to the 20-30 output produces a 1 Hz resolution in the YO frequency.

YO LOOP

The YO Loop contains the YIG oscillator (YO), which is the tunable local oscillator source for all frequency bands. When the instrument is set to a specific CW frequency, the instrument processor sets the frequency of the M/N and 20-30 loops accordingly. The instrument processor also sets the YO pretune voltage, which tunes the YO to the approximate frequency.

The output of the YO is fed through the A45 directional coupler to the RF section. The directional coupler splits off part of the YO signal, which goes to the sampler. The M/N output frequency and its harmonics are mixed with the YO frequency in the sampler to produce an IF signal between 20 and 30 MHz. The 20 to 30 MHz IF from the sampler is compared to the 20-30 loop output in the phase/frequency detector.

The error-induced voltage from the phase/frequency detector is fed through a sample/hold circuit and is summed with the pretune voltage that drives the YO tuning coils. The YO frequency changes until the output voltage from the phase/frequency detector goes to zero and phase-lock is achieved. For sweep widths greater than 5 MHz, the YO is phase-locked at the start of the sweep.

The sample/hold circuit is then set to hold, breaking the loop, and allowing the YO to sweep. The sweep generator initiates a voltage sweep (VSWP) ramp that is summed with the YO pretune voltage. This voltage causes the YO to sweep to the STOP frequency. This action is referred to as Lock and Roll. During multi-band sweeps, the YO phase-locks at the start of each band before continuing on with the sweep, ensuring frequency accuracy at the beginning of each band.

CONTROLLER SECTION

The controller section performs all data transfer, and coordinates the control signals that operate the instrument. It contains a 16-bit microprocessor, a total of 34K X 16 ROM and 8K X 16 RAM. This section also contains interface circuitry for communicating with the rest of the instrument.

Digital information is exchanged between the microprocessor and other sections of the instrument on a bi-directional bus. At power on instrument preset, the controller runs through an instrument self-test. The microprocessor also sets the front panel controls to preset conditions if instrument preset was pressed.

The rear panel interface signals (e.g. HP-IB, SWEEP OUTPUT, Z-AXIS) are also routed through or generated in the controller functional group. The sweep control signal from the controller stops and starts the sweep generator. As mentioned, during bandcrossings, the sweep must be stopped to phase lock the YO before the sweep can continue. The controller monitors sweep events such as bandcrossings, end of sweep, and markers, and executes specific instructions according to each sweep event.

FRONT PANEL – REAR PANEL

Front Panel

The front panel contains the user-interface displays and keyboard as well as various input and output connectors. The displays have a dedicated microprocessor that keeps them updated. When the instrument processor places display data into the display interface latch, it signals the display processor that information is ready. The display processor immediately takes the data from the latch and stores it in internal memory. The data is handled when the display processor has time.

The keyboard communicates directly with the instrument processor. When a key is pressed, the instrument processor either executes that key (if it is a single key operation), or waits for completion of the key sequence. Different key sequences not only allow you to set the instrument for normal operation, but also allow access to internal registers, latches, D to A converters, and calibration constants for troubleshooting.

Rear Panel

A rear panel schematic shows all interconnections between the rear panel connectors and related internal assemblies.

RF SECTION

The RF Section contains the microcircuits and control circuits that produce the 10 MHz to 20.0 GHz RF output from the 2.3 to 7.0 GHz YO loop output.

The RF output from the A45 directional coupler in the YO loop is fed to the modulator/splitter (mod/splitter) in the RF section. Band 0 (10 MHz to 2.3 Ghz) is the heterodyne band and is produced by mixing a swept LO drive from the mod/splitter with the phase-locked 3.7 GHz oscillator output. The IF signal from the low band mixer is routed through the low band power amplifier, the switched-YIG-tuned multiplier (SYTM), the high band coupler, and the 90 dB step attenuator before it reaches the RF output connector. The SYTM and high band coupler perform no function in this band.

Band 1 (2.3 to 7.0 GHz) is the same as the YO fundamental frequency. The RF from the high band output on the mod/splitter is amplified by the high band power amplifier and passes through the SYTM to the high band coupler. Part of the RF is coupled to the high band detector for leveling through the ALC Loop. After the coupler, the RF passes through the 90 dB step attenuator, to the RF OUTPUT.

The remaining bands (7.0 GHz to the maximum output frequency) are generated by multiplying the YO frequency in the SYTM. A step recovery diode (SRD) in the SYTM, when biased properly, generates harmonics of the input signal. A YIG-tuned filter tracks the desired harmonic, allowing it to pass through to the high band coupler and step attenuator to the RF output. The SYTM driver provides the necessary circuitry for the YIG-tuned filter in the SYTM to properly track the YO. Leveling in these bands is the same as in band 1.

Pulse modulation is produced by the pulse modulator driver and two fast response time pulse modulators. The low band pulse modulator, located just before the low band mixer, is used when the instrument operates below 2.3 GHz. Operation above 2.3 GHz uses the high band pulse modulator inside the mod/splitter.

ALC modulation (fixed power, AM, etc.) is produced by the ALC modulator driver and the ALC modulators. The low band modulator is located in the 3.7 GHz oscillator; the high band modulator is located in the mod/splitter.

POWER SUPPLIES

The power supply produces eight regulated voltage levels, four positive supplies and four negative supplies:

- +22, +20, +12, +5.2, −5.2, −10, −15, and −40V

The +22 volt supply powers the 10 MHz reference oscillator heater coil. This is the only supply that actually produces an output when the instrument is switched to STANDBY.

All supplies except for the + 22 volt supply are referenced either directly or indirectly to the +20 volt supply. In STANDBY mode, the +20 volt supply shuts down. This in turn shuts down the regulators for all other supplies (except the +22 volt supply).

NOTE: Although these supplies are shut down, line power is still on, the line module, transformer, motherboard, rectifiers, and filter caps still have full voltage potentials on them. Therefore, hazardous voltages exist in these sections of the instrument even when the front panel power switch is set to standby.

The +20, −15, −10, and −40V supplies deliver current to the low noise analog circuits and the microcircuits. The +12, +5.2, −5.2, and −15V supplies deliver power to the digital and noncritical analog circuits. Over-temperature protection, current limit, and over-voltage protection are built into each supply. The output voltage of each supply (excluding the +22V supply) is monitored. If any of these supplies drop out of regulation, the instrument microprocessor is flagged.

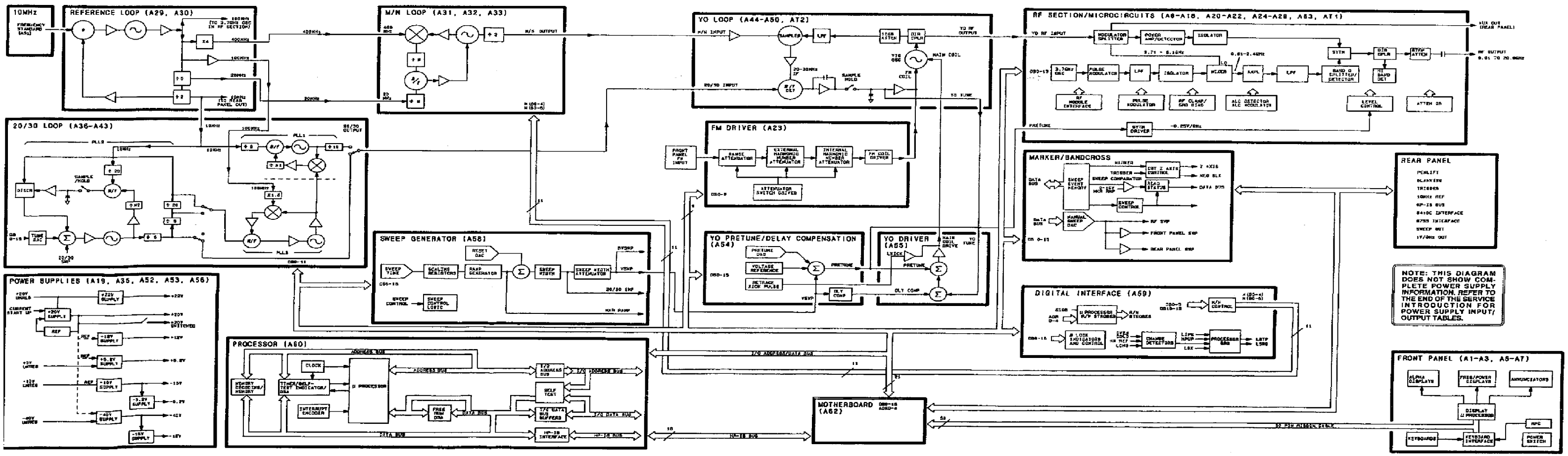


Figure A-1. HP 8341B Option 003 Block Diagram

Assembly-Level Service Calibration Constants

Three sets of calibration constants containing calibration data, serial number, option, HP-IB address, and checksum information, are maintained by the instrument:

- Working Data

  This data contains the calibration information that is required for optimum instrument performance. This is the only set of calibration constants accessed during normal operation. Working data is stored in RAM on the A60 processor assembly, and is maintained by a battery with enough energy to support RAM for three full years when the instrument is disconnected from ac mains.

- Protected Data

  This data resides in EEPROM and contains calibration information that is essentially the same as in the working data. (PEAK and SHIFT PEAK auto tracking functions change noncritical calibration constants in working data to optimize performance. This is the one area where working and protected data can normally differ.) If any unacceptable difference occurs between working and protected data, the instrument copies the protected data values into working data RAM memory. You can view or update this data.

- Default Data

  This data resides in UVEPROM, and differs from the working and protected data. ROM-based default data has immunity to improper value changes. The data, however is not for a specific instrument, rather, it is data representing the typical instrument. When using default calibration constants, instrument performance is good, but not optimized for peak performance. To return the instrument to peak performance, manually enter into protected and working memory the instrument-optimized calibration constants from the printed copy of calibration constants shipped with your instruments (see **HOW TO RESTORE FACTORY-OPTIMIZED CALIBRATION CONSTANTS**, in this section).

  The instrument only selects default data if a problem exists in both working and protected data. If this occurs, the **CAL DEFAULTED** message appears in the ENTRY DISPLAY and the FAULT indicator lights.

INSTRUMENT ACCESS

During normal operation, the instrument accesses working data to obtain the calibration information required for optimum operation. In addition, the instrument accesses working data after an instrument preset, but only to verify that the CHECKSUM (cal constant #99) is accurate (see Figure A-2).

When you press **[INSTR PRESET]**, the working data cal constants 1 through 98 are summed and then complemented. The result is compared with the CHECKSUM. If the two numbers agree, the instrument continues normal operation. If not, protected data is written into the working data memory location and the CHECKSUM test is repeated. If the checksum test passes, the data in protected data is stored as working data. **CALIBRATION RESTORED** appears in the ENTRY DISPLAY.

If the CHECKSUMs do not agree, default data is written to the working data. Working data now contains the default values, the front panel FAULT light lights, and **CAL DEFAULTED** is displayed.

Press **[SHIFT] [MANUAL]** to display the FAULT diagnostics in the ENTRY DISPLAY; the CAL light flashes (note that the protected data was not changed. For troubleshooting, this data can be written into the working data and viewed — see **USER ACCESS**).

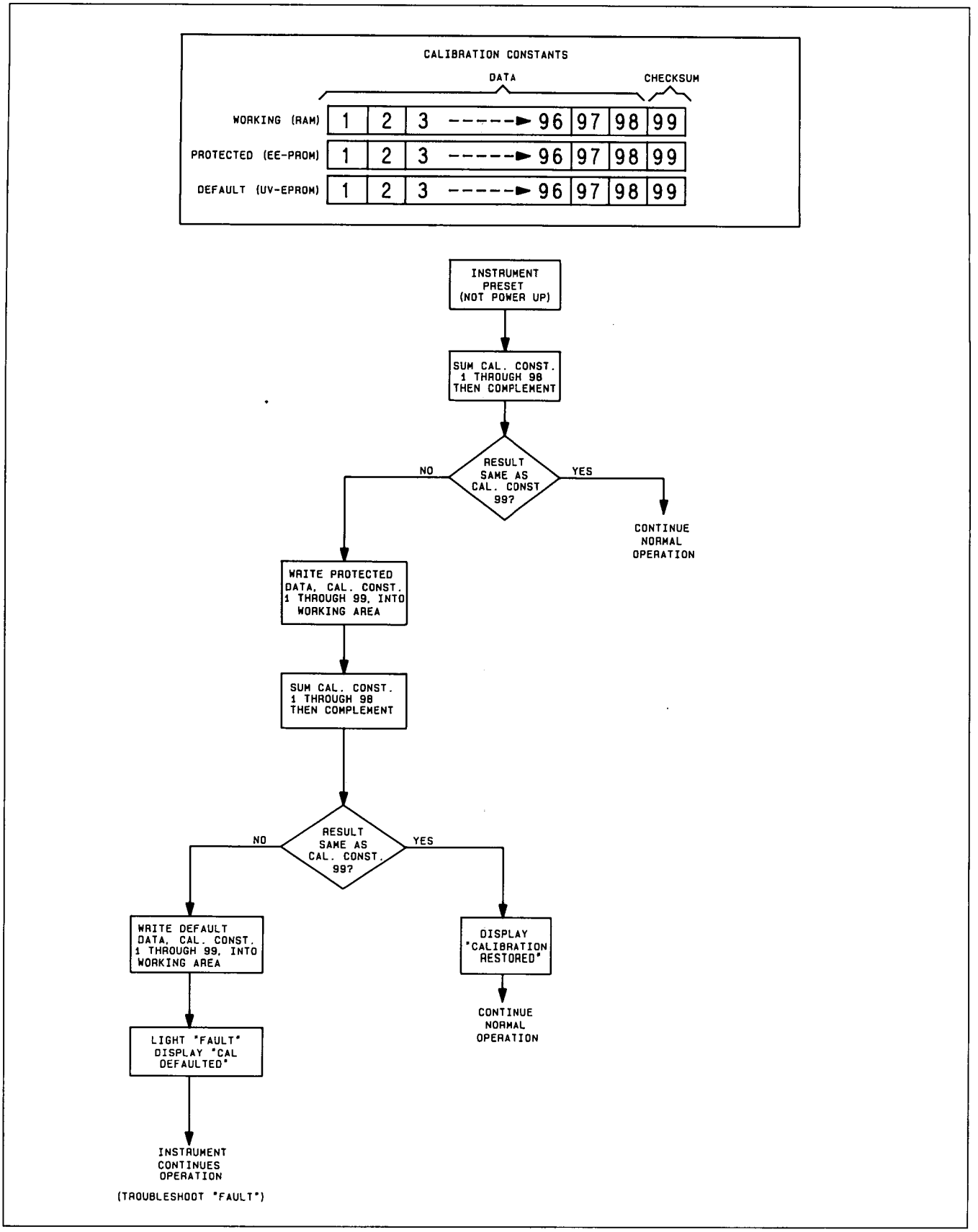


Figure A-2. Instrument Preset Calibration Constant Verification Sequence

USER ACCESS

CAUTION

The following are methods of intentionally changing the values of calibration constants.

When correcting a cal constant error, the CHECKSUM is automatically updated when the first cal constant is corrected. This causes the CAL FAULT indication to go away on the next [INSTR PRESET], whether ALL the corrections were made or not. This means that if only a few cal constants are updated, the balance are still using default data.

[SHIFT] [PEAK] (optimize power output) updates working cal constants and also resets the FAULT indication.

Calibration Constant Access

NOTE: If the calibration constants will not change when you perform the following procedure, the calibration constant password feature is active (see **How to Enter a Password**). To disable the password function, re-install jumper A59W2.

1. To access calibration constants, press:

   [SHIFT] [GHz] [#] [#] [Hz]
   (I/O CHANNEL: ## = the desired Cal Constant number to be viewed)

   [SHIFT] [MHz] [1] [2] [Hz]
   (I/O SUBCHANNEL: 12 displayed in ENTRY DISPLAY)

   [SHIFT] [kHz] [2] [2] [Hz]
   (I/O WRITE: 22 displayed in ENTRY DISPLAY)

   This lets you direct access the desired cal constant in working data. The cal constant value is displayed in the ENTRY DISPLAY and you can either see or change it.

2. To change the cal constant value, use the front panel knob or the entry keyboard.

3. To execute the change and update the checksum, press **[Hz]**.

4. To scroll through the other calibration constants, use the up and down **[STEP]** keys.

NOTE: Using this method changes only the working data. To permanently change the protected data, follow the procedure described in **Working Data to Protected Data Transfer**.

HP-IB Address Access

1. Press:

   [SHIFT] [LOCAL]

   This lets you see the HP-IB address in the ENTRY DISPLAY.

2. To change the HP-IB address (00 to 30):

   a. Rotate the front panel knob or use the keyboard entry.

   b. When the desired address is set, press **[Hz]**. The HP-IB address is changed, and the CHECK-SUM updated (note that only the working data is updated).

3. To write protect the HP-IB address, set bit 5 of cal constant #57 and lock out the **[SHIFT] [LOCAL]** function:

   a. Access the working data cal constant #57 as described above.
   b. Set bit 5 by adding 32 to the HP-IB address. Enter this value.
   c. Press **[Hz]**.

Automatic SYTM to YTO Tracking (Power Optimization)

1. To recalculate and store the working data checksum, and update the SYTM GAIN calibration constants (#9 through 12 and 50 through 53) for peak RF output power, press:

   [SHIFT] [PEAK]

   This also automatically turns off the **CAL FAULT** indicator without performing an instrument preset.

Working Data to Protected Data Transfer

1. To recalculate and store the working data checksum, and store working data as protected data, press:

   [SHIFT] [MHz] [1] [4] [Hz]
   [SHIFT] [kHz] [5] [3] [4] [9] [Hz]

   This is the only way to to update protected data. If this data transfer fails, the message **EEPROM FAILURE, CAL NOT RESTORED** is displayed in the ENTRY DISPLAY.

Protected Data to Working Data Transfer

1. To recall protected data and store it in the working data memory location, press:

   [SHIFT] [1Hz] [1] [4] [Hz]
   [SHIFT] [kHz] [1] [9] [4] [6] [Hz]2.

   After writing over the working data, press **[SHIFT] [PEAK]** to optimize instrument operation.

Save/Recall Register Initialization

1. To reinitialize the save/recall registers in RAM (this function does not effect the Cal Constants), press:

   [SHIFT] [MHz] [1] [8]
   [SHIFT] [kHz] [0] [Hz]

2. Turn the instrument off then on, and press **[INSTR PRESET]**.

Calibration Constant Password Enable

This procedure lets you prevent viewing or manipulation of instrument calibration constants without a password (number)

NOTE: Once the password is entered, the instrument allows calibration constant access until **[INSTR PRESET]** is pressed.

1. To activate the password function, press:

   [SHIFT] [GHz] [8] [2] [Hz]
   [SHIFT] [MHz] [1] [2] [Hz]
   [SHIFT] [kHz] [2] [2] [Hz]
   [-] [2] [3] [8] [7] [5] [Hz]

   This key sequence accesses cal constant #82 (LOCKWORD ENABLE) and sets it to −23,875, enabling the lockword function.

2. To change the password number:

   The password number is held in cal constant #81 (LOCKWORD) and is factory set to 0.

   a. Access cal constant #81 (press the down arrow STEP key).
   b. Use the ENTRY keyboard to enter a number between −32,768 and 32,767.
   c. To terminate the entry, press **[Hz]**.

   The number entered is the password required to access the calibration constants.

3. Remove jumper A59W2 on the A59 digital interface assembly.

4. If you forget the password, re-install jumper A59W2 to disable the password function.

How to Enter a Password

1. To access the location (subchannel) where the password is required, press:

   [SHIFT] [MHz] [2] [0] [Hz]
   [SHIFT] [kHz]

2. Enter the password:

   a. Use the keyboard to enter the password number.
   b. Press **[Hz]**.

NOTE: To enter a password via HP-IB, type **"SHMZ20HZ SHKZ###HZ"** (### is the password number).

When the correct password is entered, you can access the calibration constants as described in the preceding procedures.

The password allows access to calibration constants until you press **[INSTR PRESET]** (HP-IB: IP).

CALIBRATION CONSTANTS DESCRIPTION

Table A-3 lists the calibration constants with a description of each. The values in the **Range** column show the amount of adjustment possible with the cal constant. The numbers shown are the only numbers you should enter. You can enter values out of the given range, but they do not represent the values used by the instrument.

The column labeled **Significance** gives the units associated with the cal constant. For example, the value entered for LOCK DWELL TIME represents the number of milliseconds the instrument waits, after phase lock, at the beginning of a sweep, or at bandcross, before it continues its sweep. Another example is the ALC 9 GHz SLOPE, for each count, a power compensation of 0.0025 dB/GHz is added to the RF output [if 10 is entered, a 0.025 dB/GHz slope (10 times 0.0025 dB/GHz) is added for a sweep within the 9 to 20 GHz range].

Five of the Cal Constants [PRESET OPTION (#56), HP-IB ADD & LOCK (#57), RETRACE DWELL (#58), ATTENUATOR CONFIG (#59), and CONFIGURATION (#60)] use their bit configuration to store more than one piece of information. For example, the HP-IB ADDRESS sets up the HP-IB address and allows or disallows the SHIFT LOCAL, SHIFT SAVE, and SHIFT RECALL functions. If a you wish to set up an HP-IB address of 19, disallow the SHIFT LOCAL and RECALL functions, and allow the SHIFT SAVE function, enter 179 for Cal Constant #57. You find the appropriate calibration constant (179 in this example) by adding the appropriate calibration constants for the individual functions:

```
  19 (HP-IB address)
  32 (disallows SHIFT LOCAL)
   0 (allows SHIFT SAVE)
 128 (disallows SHIFT RECALL)
 ---
 179
```

The other four cal constants work the same way.

Table A-3. Calibration Constants (1 of 6)

No.	Name	Function	Range (Counts)	Significance
1	DWELL TIME	Defines time to wait after phase lock at beginning of sweep and at bandcross.	0-500	0.2 ms/count
2	YTM BX DLY 2	Compensates for YTM Delay in Band 2 after bandcross from Band 1 to Band 2.	0-131	2.4 MHz/ms/count
3	YTM BX DLY 3	Compensates for YTM Delay in Band 3 after bandcross from Band 2 to Band 3.	0-131	2.4 MHz/ms/count
4	YTM BX DLY 4	Compensates for YTM Delay in Band 4 after bandcross from Band 3 to Band 4.	0-131	2.4 MHz/ms/count
5	YTM DLY 1	Compensates for YTM Delay in Band 1.	0-131	2.4 MHz/ms/count
6	YTM DLY 2	Compensates for YTM Delay in Band 2 for single band sweeps or multi-band sweeps that begin in Band 2.	0-131	2.4 MHz/ms/count
7	YTM DLY 3	Compensates for YTM Delay in Band 3 for single band sweeps or multi-band sweeps that begin in Band 3.	0-131	2.4 MHz/ms/count
8	YTM DLY 4	Compensates for YTM Delay in Band 4 for single band sweep.	0-131	2.4 MHz/ms/count
9	YTM GAIN 1	Adjusts Band 1 in YTM slow speed tracking.	0-2040	−4% - +4% of YTM Frequency
10	YTM GAIN 2	Adjusts Band 2 YTM slow speed tracking.	0-2040	−2% - +2% of YTM Frequency
11	YTM GAIN 3	Adjusts Band 3 YTM slow speed tracking.	0-2040	−1.33% - +1.33% of YTM Frequency
12	YTM GAIN 4	Adjusts Band 4 YTM slow speed tracking	0-2040	−1% - +1% of YTM Frequency
13	LO SLOPE	Slope compensation for RF power in Band 0.	0-255	0.005 dB/GHz/count
14	HI SLOPE	Slope compensation for RF power from 2.3 to 9.0 GHz.	0-255	0.005 dB/GHz/count
15	9 GZ SLOPE	Slope compensation for RF power from 9.0 to 20.0 GHz.	0-255	0.0025 dB/GHz/count
16	20 GZ SLOPE	Slope compensation for RF power from 20.0 to 26.5 GHz.	0-255	0.01 dB/GHz/count
17	AT10 OFFSET	Offset compensation for RF power at 10 dB attenuator setting from 0.01 to 26.5 GHz.	0-100	0.05 dB/count
18	AT20 OFFSET	Offset compensation for RF power at 20 dB attenuator setting from 0.01 to 26.5 GHz.	0-100	0.05 dB/count
19	AT30 OFFSET	Offset compensation for RF power at 30 dB attenuator setting from 0.01 to 26.5 GHz.	0-100	0.05 dB/count
20	AT40 OFFSET	Offset compensation for RF power at 40 dB attenuator setting from 0.01 to 26.5 GHz.	0-100	0.05 dB/count

Table A-3. Calibration Constants (2 of 6)

No.	Name	Function	Range (Counts)	Significance
21	AT50 OFFSET	Offset compensation for RF power at 50 dB attenuator setting from 0.01 to 26.5 GHz.	0-100	0.05 dB/count
22	AT60 OFFSET	Offset compensation for RF power at 60 dB attenuator setting from 0.01 to 26.5 GHz.	0-100	0.05 dB/count
23	AT70 OFFSET	Offset compensation for RF power at 70 dB attenuator setting from 0.01 to 26.5 GHz.	0-100	0.05 dB/count
24	AT80 OFFSET	Offset compensation for RF power at 80 dB attenuator setting from 0.01 to 26.5 GHz.	0-100	0.05 dB/count
25	AT90 OFFSET	Offset compensation for RF power at 90 dB attenuator setting from 0.01 to 26.5 GHz.	0-100	0.05 dB/count
26	AT10 SLOPE	Slope compensation for RF power at 10 dB attenuator setting from 2.3 to 20.0 GHz.	0-255	0.005 dB/GHz/count
27	AT20 SLOPE	Slope compensation for RF power at 20 dB attenuator setting from 2.3 to 20.0 GHz.	0-255	0.005 dB/GHz/count
28	AT30 SLOPE	Slope compensation for RF power at 30 dB attenuator setting from 2.3 to 20.0 GHz.	0-255	0.005 dB/GHz/count
29	AT40 SLOPE	Slope compensation for RF power at 40 dB attenuator setting from 2.3 to 20.0 GHz.	0-255	0.005 dB/GHz/count
30	AT50 SLOPE	Slope compensation for RF POWER at 50 dB attenuator setting from 2.3 to 20.0 GHz.	0-255	0.005 dB/GHz/count
31	AT60 SLOPE	Slope compensation for RF power at 60 dB attenuator setting from 2.3 to 20.0 GHz.	0-255	0.005 dB/GHz/count
32	AT70 SLOPE	Slope compensation for RF power at 70 dB attenuator setting from 2.3 to 20.0 GHz.	0-255	0.005 dB/GHz/count
33	AT80 SLOPE	Slope compensation for RF power at 80 dB attenuator setting from 2.3 to 20 GHz.	0-255	0.005 dB/GHz/count
34	AT90 SLOPE	Slope compensation for RF power at 90 dB attenuator setting from 2.3 to 20 GHz.	0-255	0.005 dB/GHz/count
35	LEV DAC OFF; SYS	Level DAC offset for mm system leveling.	−100 - +100	0.05 dB/count
36	LEV DAC GAIN; SYS	Level DAC gain for mm system leveling.	−100 - +100	−10% - +10%
37	ADC OFFSET; SYS	ADC offset for mm system leveling.	−100 - +100	0.05 dB/count
38	ADC GAIN; SYS	ADC gain for mm sys leveling.	−100 - +100	−10% - +10%
39	ADC GAIN LO	Adjusts front panel dBm display accuracy from .01 to 2.3 GHz.	−100 - +100	−10% - +10%
40	ADC GAIN HI	Adjusts front panel dBm display accuracy from 2.3 to 26.5 GHz.	−100 - +100	−10% - +10%
41	MAX SWEEP RATE	Sets the maximum sweep rate in the AUTO sweeptime mode.	1-1000	1 MHz/ms/count
42	ADC OFFSET	Adjusts front panel dBm display.	−100 - +100	0.05 dB/count

Table A-3. Calibration Constants (3 of 6)

No.	Name	Function	Range (Counts)	Significance
43	AM OFFSET	Modulation level offset for output power accuracy in AM mode.	−100 - +100	0.05 dB/count
44	LVL DAC OFF; INT	Offsets level DAC on A27 for internal leveling operation.	−100 - +100	0.05 dB/count
45	LVL DAC OFF; EXT	Offsets level DAC on A27 for external leveling operation.	−100 - +100	0.05 dB/count
46	LVL DAC GAIN; LO	Adjusts gain of level DAC for internal leveling operation in Band 0.	−100 - +100	1% of ALC power (in dBm)/count
47	LVL DAC GAIN; HI	Adjust gain of level DAC for internal leveling operation in Bands 1-4.	−100 - +100	−10.0% - +10.0%
48	LVL DAC GAIN; EXT	Adjusts gain of level DAC for external leveling operation.	−100 - +100	−10.0% - +10.0%
49	PWR SWP	Adjust gain of power sweep DAC on A27 during power sweep operation.	−100 - +100	−10.0% - +10.0%
50	YTM BX GAIN 1	Adjusts YTM slow speed tracking for sweeps which cross from Band 0 to Band 1.	0-2040	−4% - +4% YTM Frequency
51	YTM BX GAIN 2	Adjusts YTM slow speed tracking for sweeps which cross from Band 1 to Band 2.	0-2040	−2% - +2 of YTM Frequency
52	YTM BX GAIN 3	Adjusts YTM slow speed tracking for sweeps which cross from Band 2 to Band 3.	0-2040	−1.33% - +1.33% of YTM Frequency
53	YTM BX GAIN 4	Adjusts YTM slow speed tracking for sweeps which cross from Band 3 to Band 4.	0-2040	−1% - +1% of YTM Frequency
54	STOP LIMIT	Sets maximum allowable stop frequency.	11 - 26,500	1 MHz/count
55	START LIMIT	Sets minimum allowable start frequency.	10-(STOP LIMIT −1)	1 MHz/count
56	PRESET OPTION	Selects instrument's operating conditions.		
		Bits 0 through 7 - Selects power level after **[INSTR PRESET]**.	0-110	0 dBm - −110 dBm
		Bit 10 - PMI Network Analyzer retrace compatibility.	0/1024	Disabled/Enabled
		Bit 12 - CIIL compatibility (option not installed or installed)	0/4096	Not Installed/Installed
57	HB-IB ADDRESS	Selects instrument's operating conditions.		
		Bits 0 through 4 - selects HP-IB address.	00 - 30	Instrument's HP-IB Address
		Bit 5 - allows or disallows the HP-IB address to be changed after entering a **[SHIFT] [LOCAL]**	0/32	Allowed/Disallowed
		Bit 6 - allows or disallows the **[SHIFT] [SAVE]** function.	0/64	Allowed/Disallowed
		Bit 7 - allows or disallows the **[SHIFT] [RECALL]** function.	0/128	Allowed/Disallowed

Table A-3. Calibration Constants (4 of 6)

No.	Name	Function	Range (Counts)	Significance
58	RETRACE DWELL	Sets instrument dwell time after end of sweep retrace.	0-20	10 ms/count
59	ATTEN CONFIG	Selects Attenuator operating conditions.		
		Bits 0 through 9 - selects attenuator switch threshold.	0-1020	0.05 dB/5 counts
		A 0 entry sets the attenuator switch threshold at −14.95 dBm (i.e., in coupled mode, the ALC will go as low as −14.95 dBm. At −15.0 dBm, the ALC is set to −5 dBm and the attenuator switches in 10 dB of attenuation). A 500 entry sets the attenuator switch threshold at −9.95. A 1020 entry sets the attenuator switch threshold at −4.75.		
		Bit 10 - Must be set to 1. This allows attenuator to be operated over 90 dB.	1024	90 dB operation
		Bit 12 - Selects attenuator Installed or not installed.	0/4096	Installed/ Not Installed
		Bit 13 - Must be set to one.	1	—
		Bit 14 - Set to zero.	0	—
		Bit 15 - Must be set to 0. This selects how attenuator is programmed.	0	Attenuator Programming
60	CONFIGURATION	Selects instrument options		
		Bit 0 - Must be set to zero	0	
		Bit 1 - Without or With Option 001 or 005 (No attenuator option).	0/2	Without/With
		Bit 2 - Without or With Option 004 or 005 (Rear panel option).	0/4	Without/With
		Bit 13 - Without or With C75 Special.	0/8192	Without/With
61	SERIAL #	Storage location for the instrument's serial number.	—	—
62	AT10 SLP 20GZ	Slope compensation for RF power at 10 dB attenuator setting from 20 to 26.5 GHz.	0 - 255	0.01 dB/GHz/ count
63	AT20 SLP 20GZ	Slope compensation for RF power at 20 dB attenuator setting from 20.0 to 26.5 GHz.	0 - 255	0.01 dB/GHz/ count

Table A-3. Calibration Constants (5 of 6)

No.	Name	Function	Range (Counts)	Significance
64	AT30 SLP 20GZ	Slope compensation for RF power at 30 dB attenuator setting from 20.0 to 26.5 GHz.	0 - 255	0.01 dB/GHz/ count
65	AT40 SLP 20GZ	Slope compensation for RF power at 40 dB attenuator setting from 20.0 to 26.5 GHz.	0 - 255	0.01 dB/GHz/ count
66	AT50 SLP 20GZ	Slope compensation for RF power at 50 dB attenuator setting from 20.0 to 26.5 GHz.	0 - 255	0.01 dB/GHz/ count
67	AT60 SLP 20GZ	Slope compensation for RF power at 60 dB attenuator setting from 20.0 to 26.5 GHz.	0 - 255	0.01 dB/GHz/ count
68	AT70 SLP 20GZ	Slope compensation for RF power at 70 dB attenuator setting from 20.0 to 26.5 GHz.	0 - 255	0.01 dB/GHz/ count
69	AT80 SLP 20GZ	Slope compensation for RF power at 80 dB attenuator setting from 20.0 to 26.5 GHz.	0 - 255	0.01 dB/GHz/ count
70	AT90 SLP 20GZ	Slope compensation for RF power at 90 dB attenuator setting from 20.0 to 26.5 GHz.	0 - 255	0.01 dB/GHz/ count
71	YTM OFFSET 1		0 - 2048	
72	YTM OFFSET 2		0 - 2048	
73	YTM OFFSET 3		0 - 2048	
74	YTM OFFSET 4		0 - 2048	
75	YTM SGL BD RT	YTM Single Band Rise Time	−25 - +25	0.1 µsec/count
76	YTM MLT BD RT	YTM Multi Band Rise Time	0 - 1000	1 µsec/count
77	YTM BX RTA	YTM Breakpoint Rise Time A	−100 - +100	1 µsec/count
78	YTM BX RTB	YTM Breakpoint Rise Time B	−100 - +100	100 MHz/count
79	OI MODEL	Specifies instrument model number outputted when HP-IB "OI" command received.	0 - 2, 5	0=8340A 1=8341A 2=8340B 5=8341B
80	YTM TEMP COMP	SYTM tracking compensation for changes in temperature.	0 - 200	
81	LOCKWORD	Defines password required to access calibration constants.	−32,768 - +32,767	
82	LOCKWORD ENABLE	Enables lockword function which is used to allow access to calibration constants only upon input of the correct password (lockword).	0/−23,875	Disabled/ Enabled
83		UNUSED		
84		UNUSED		
85		UNUSED		

Table A-3. Calibration Constants (6 of 6)

No.	Name	Function	Range (Counts)	Significance
86		UNUSED		
87		UNUSED		
88		UNUSED		
89		UNUSED		
90		UNUSED		
91		UNUSED		
92		UNUSED		
93		UNUSED		
94		UNUSED		
95		UNUSED		
96		UNUSED		
97		UNUSED		
98	MODEL #	Instrument model number.	0 - 2, 5, 99	0=8340A 1=8341A 2=8340B 5=8341B 99=8340A-HO2
99	CHECKSUM	Serves as check point for Cal Constant Accuracy. The sum of Cal Constants 1 through 98 is calculated, the sum is complemented, and the result is stored as the CHECKSUM.	—	—

HOW TO RESTORE FACTORY-OPTIMIZED CALIBRATION CONSTANTS

A printed copy of protected data is included with each instrument. It is stored in a bracket located under the top cover, on the left side of the instrument (as viewed from the front).

If working and protected data in RAM are lost, use the information on this sheet to restore the cal constants.

When the instrument is recalibrated, the printed copy protected data should be updated and placed back in the instrument (remember to update protected data after recalibration). Figure A-3 shows an example of a calibration constant printed copy.

1. Remove the top cover of the instrument. Inside the instrument, find the printed copy of calibration constants (they are in a metal bracket on the left side of the instrument, as viewed from the front).
2. Replace the top cover.

CAUTION

This procedure affects data required for optimum instrument performance. Be careful when accessing or changing calibration data.

3. To access the calibration constants, press:

   [SHIFT] [GHz] [1] [Hz]
   [SHIFT] [MHz] [1] [2] [Hz]
   [SHIFT] [KHz] [2] [2] [Hz]

   The value of calibration constant #1 is displayed in the ENTRY display.

4. Compare the value on the ENTRY display with the value listed in the print-out. If the values do not match:

   a. Enter the value from the print-out via the DATA ENTRY keyboard.
   b. Press **[Hz]**.

5. To see the next calibration constant, press the up STEP key.
6. Repeat steps 4 and 5 until all calibration constants are the same as those shown on the print-out.
7. To store the entered calibration constants into protected memory, press:

   [SHIFT] [MHz] [1] [4] [Hz]
   [SHIFT] [KHz] [5] [3] [4] [9] [Hz]

   CALIBRATION STORED appears in the ENTRY display.

8. Press **[INSTR PRESET]**.

   The FAULT indicator should be off. If it is still on, suspect a problem with the instrument's memory.

9. Replace the print-out inside the instrument.

8340/41B CALIBRATION CONSTANTS

SERIAL NUMBER; 0000 **834041BREV 01 AUG 86**

1.	DWELL TIME	50	34.	AT90 SLOPE	−10	67.	AT60 SLP 20GZ	10
2.	YTM BX DLY 2	74	35.	LEV DAC OFF; SYS	−2	68.	AT70 SLP 20GZ	13
3.	YTM BX DLY 3	69	36.	LEV DAC GAIN; SYS	−27	69.	AT80 SLP 20GZ	15
4.	YTM BX DLY 4	100	37.	ADC OFF SYS	−1	70.	AT90 SLP 20GZ	18
5.	YTM DLY 1	80	38.	ADC GAIN SYS	−3	71.	YTM OFFSET 1	1055
6.	YTM DLY 2	101	39.	ADC GAIN LO	−40	72.	YTM OFFSET 2	1108
7.	YTM DLY 3	100	40.	ADC GAIN HI	−40	73.	YTM OFFSET 3	902
8.	YTM DLY 4	100	41.	MAX SWEEP RATE	600	74.	YTM OFFSET 4	1024
9.	YTM GAIN 1	1084	42.	ADC OFFSET	3	75.	YTM SGL BD RT	25
10.	YTM GAIN 2	964	43.	AM OFFSET	2	76.	YTM MLT BD RT	1000
11.	YTM GAIN 3	1151	44.	LVL DAC OFF; INT	−6	77.	YTM BX RTA	−25
12.	YTM GAIN 4	1024	45.	LVL DAC OFF; EXT	0	78.	YTM BX RTB	25
13.	LO SLOPE	49	46.	LVL DAC GAIN; LO	11	79.	OI MODEL	5
14.	HI SLOPE	117	47.	LVL DAC GAIN; HI	12	80.	YTM TEMP COMP	−17
15.	9GZ SLOPE	80	48.	LVL DAC GAIN; EXT	−23	81.	LOCKWORD	0
16.	20GZ SLOPE	129	49.	PWR SWP GAIN	4	82.	LOCKWORD ENABLE	0
17.	AT10 OFFSET	−5	50.	YTM BX GAIN 1	0	83.	unused	0
18.	AT20 OFFSET	−7	51.	YTM BX GAIN 2	0	84.	unused	0
19.	AT30 OFFSET	−5	52.	YTM BX GAIN 3	0	85.	unused	0
20.	AT40 OFFSET	−9	53.	YTM BX GAIN 4	0	86.	unused	0
21.	AT50 OFFSET	−10	54.	STOP LIMIT	20000	87.	unused	0
22.	AT60 OFFSET	−11	55.	START LIMIT	10	88.	unused	0
23.	AT70 OFFSET	−14	56.	PRESET OPTION	0	89.	unused	0
24.	AT80 OFFSET	−20	57.	HPIB ADDRESS	19	90.	unused	0
25.	AT90 OFFSET	−23	58.	RETRACE DWELL	0	91.	unused	0
26.	AT10 SLOPE	−1	59.	ATTEN CONFIG	9716	92.	unused	0
27.	AT20 SLOPE	−2	60.	CONFIGURATION	513	93.	unused	0
28.	AT30 SLOPE	−3	61.	SERIAL #	378	94.	unused	0
29.	AT40 SLOPE	−5	62.	AT10 SLP 20GZ	4	95.	unused	0
30.	AT50 SLOPE	−5	63.	AT20 SLP 20GZ	5	96.	unused	0
31.	AT60 SLOPE	−7	64.	AT30 SLP 20GZ	5	97.	unused	0
32.	AT70 SLOPE	−8	65.	AT40 SLP 20GZ	8	98.	MODEL #	5
33.	AT80 SLOPE	−9	66.	AT50 SLP 20GZ	9	99.	CHECKSUM	24097

Procedure for manually entering calibration data into the SOURCE:

1. Push the following sequence of KEYS:
   [Instrument Preset] [SHIFT] [MHz] [1] [2] [Hz] [SHIFT] [KHz] [2] [2] [Hz]
2. Note the Entry Display will indicate the Calibration Constant number and value.
3. Enter via the KEY BOARD or DATA KNOB the correct value for the first Calibration Constant indicated in the display.
   ≪ Terminate KEYBOARD entries with the Hz key ≫
4. Go to the next Calibration Constant by pushing the UP step key. The next constant can then be entered. Do not enter the "CHECKSUM" Constant. (This is computed automatically)
5. The Step Keys can be used to move from one Calibration Constant to another to either check them or to correct them.
6. After all entries have been made, check that all numbers are correct by using the step keys to review and verify them.
7. Allow instrument to warm up for 1/2 hour and make sure that nothing is connected to the Stop Sweep connector on the rear panel. Push SHIFT PEAK to perform an Automatic Tracking Calibration. This step may modify the "YTM GAIN n" & "YTM BX GAIN n" consts.
8. The CALIBRATION data should be permanently stored in the Non Volatile Protected Memory by pushing the following key sequence: **[SHIFT] [MHz] [1] [4] [Hz] [SHIFT] [KHz] [5] [3] [4] [9] [Hz] [PRESET]**.

Figure A-3. Sample Calibration Constants Printed Copy (Found Inside Instrument)

SELF TEST

Self test verifies:

- A60 microprocessor assembly operation
- That address and data information can be transmitted accurately over the instrument address bus and instrument data bus.

Refer to **OVERALL INSTRUMENT TROUBLESHOOTING** for details.

PHASE-LOCK INDICATION LEDS

Three green LEDs in the instrument indicate when a phase-lock condition exists for three phase-lock loops. Each LED is lit when its specific loop is phase-locked:

- A37DS1 PLL1
- A39DS1 PLL3
- A50DS1 YO

POWER SUPPLY INDICATION LEDS

Eight yellow LEDs indicate when the power supplies are at their required voltage. Each LED is lit when its specific power supply is up:

- A35DS1 +22V
- A52DS1 +5.2V
- A52DS2 +20V
- A52DS3 +12V
- A53DS1 −5.2V
- A53DS2 −40V
- A53DS3 −10V
- A56DS1 −15V

Three red LEDs indicate:

- A19DS1 Voltage is present on the A19 capacitor assembly.
- A52DS4 The instrument is in shutdown due to over-temperature.
- A62DS1 Line power is connected.

Assembly-Level Service
Front Panel Diagnostics

The SOURCE has several self-checking diagnostic routines you can activate using front panel keys.

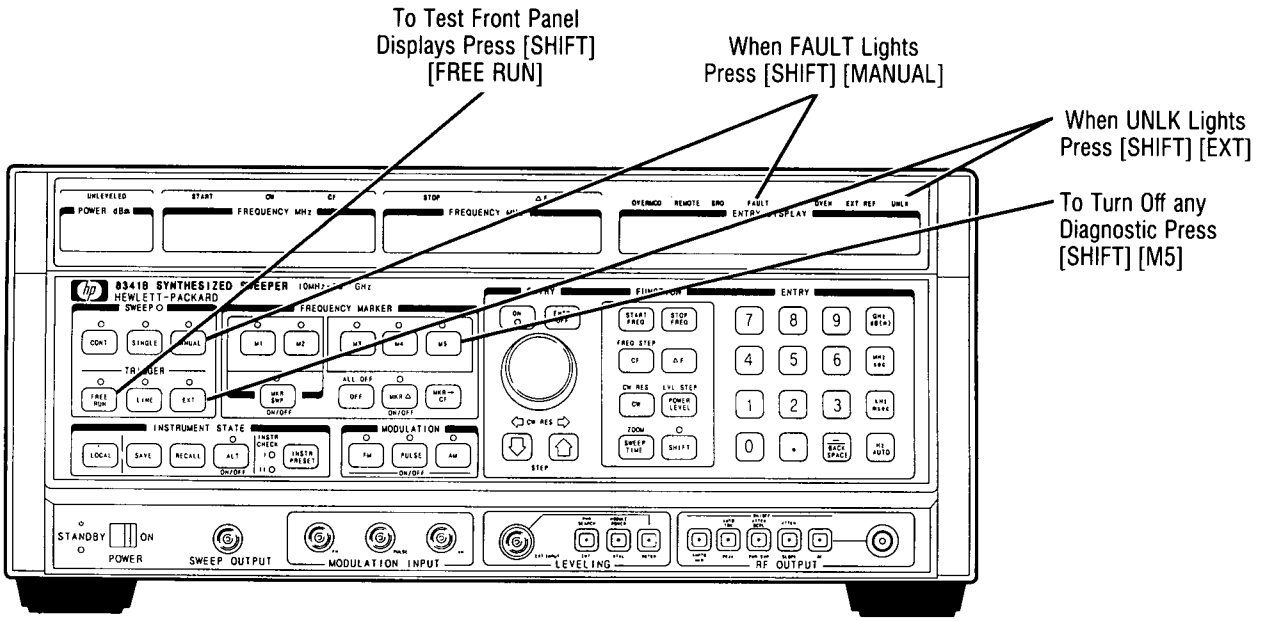


Figure A-4. Front Panel Diagnostics

NOTE: SHIFT M5 cancels all front panel diagnostic functions.

SHIFT MANUAL (HP-IB: SHS3)

If, during normal operation, the amber **FAULT** annunciator appears in the ENTRY DISPLAY:

1. Press **[SHIFT] [MANUAL]** to initiate the FAULT diagnostic routine

   FAULT CAL KICK ADC PEAK TRK appears in the ENTRY DISPLAY.

   A flashing cursor indicates the faulty instrument area:

   CAL calibration constants
   KICK kick sweep end points
   ADC analog-to-digital converter
   PEAK power peaking
   TRK tracking

   Refer to Figure A-4.

SHIFT FREE RUN (HP-IB: SHT1)

1. To activate the display self test diagnostic function, press:

   [SHIFT] [FREE RUN]

   This causes every segment of every LED in the displays to light, followed by a marching pattern of every character in the display.

SHIFT EXT (HP-IB: SHT3)

If the red UNLK annunciator appears in the ENTRY DISPLAY:

1. Press **[SHIFT] [EXT]** to activate the oscillator diagnostic function.

   OSC: REF M/N HET YO N2 N1 appears in the ENTRY DISPLAY.

   The flashing cursor indicates which oscillator circuit is causing the unlocked condition.

SHIFT M1 (HP-IB: SHM1)

This diagnostic function shows, from left to right, what the M divisor, N divisor, M/N frequency, and 20/30 loop frequency should be (see Figure A-5).

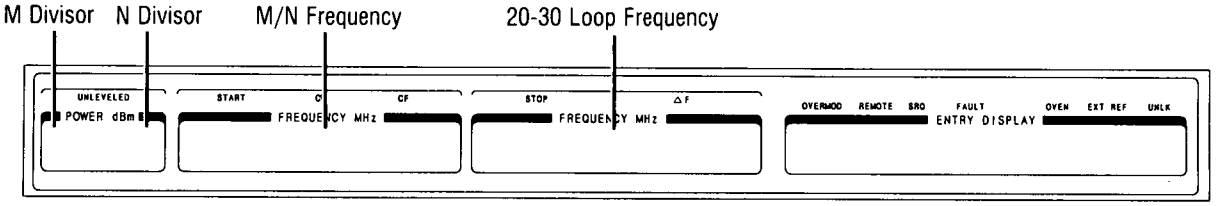


Figure A-5. M/N Diagnostics

SHIFT M2 (HP-IB: SHM2)

This diagnostic shows, from left to right, what the band number and the YIG oscillator (YO) frequency should be (see Figure A-6).

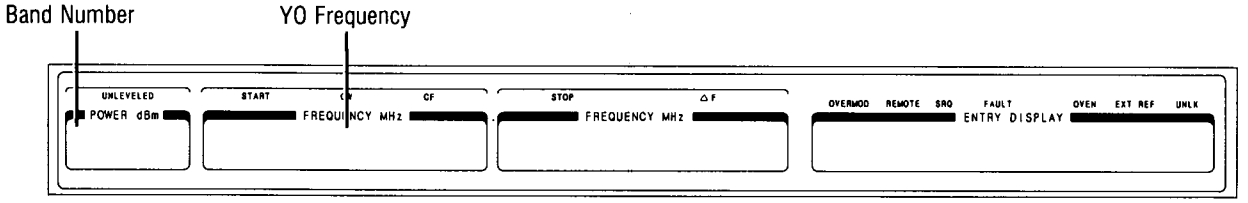


Figure A-6. YO Diagnostics

SHIFT M3 (HP-IB: SHM3)

This diagnostic shows, from left to right, what the PLL2 VCO frequency and the PLL3 upconverter frequency should be (see Figure A-7)

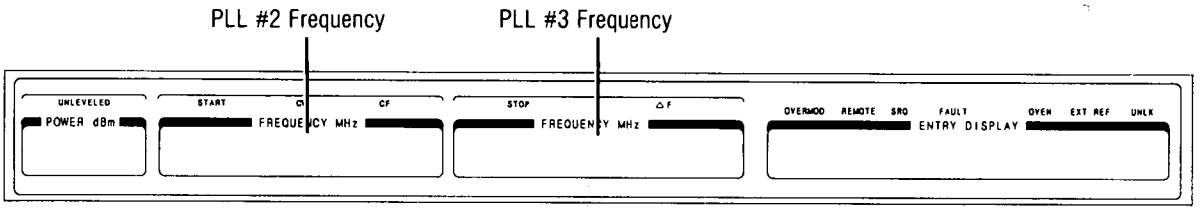


Figure A-7. 20-30 Loop Diagnostics

SHIFT M4 (HP-IB: SHM4)

SHIFT M4 activates 32 service diagnostic routines that test some of the DACs and much of the control circuits on the A27 level control, A28 SYTM driver, A57 marker bandcross, and A58 sweep generator assemblies. This diagnostic also allows the results of the self test, run at power on and after instrument preset, to be displayed in the front panel ENTRY DISPLAY.

The DAC tests are not exhaustive (a small error does not generate a failure indication), but if a test fails, the indication should direct you to a specific device or circuit path.

While the tests are running, the **DIAGNOSTIC TEST IN PROGRESS** appears in the front panel ENTRY DISPLAY. When the tests finish, **TEST:? FULL DIAGNOSTIC** and then **PASS** or **FAIL** appear. Pass indicates that **all** tests related to this diagnostic passed. Fail indicates that **one or more** tests failed.

See the controller section functional group for details on the SHIFT M4 diagnostics.

SHIFT M5 (HP-IB: SHM5)

SHIFT M5 turns off any of the above diagnostic routines, and restores the displays to their previous condition.

SHIFT RF (HP-IB: SHRF)

SHIFT RF disables the ALC (automatic leveling control) to allow direct control of the linear modulator circuit. When SHIFT RF is engaged, there is no limit on the minimum pulse repetition frequency.

1. Press **[SHIFT] [RF]**

   POWER SEARCH:X.XXdB appears in the entry display (X.XX is the last-entered value).

2. Place the instrument in CW, or in pulse modulation mode with pulses wider than 2 μs.

3. Using the step keys, the data entry keyboard, or the front panel knob, set the desired power level.

   The POWER dBm display shows the actual power when the instrument is in the CW or pulse modulation mode.

SHIFT RF can also be used as a diagnostic function of the ALC circuits.

SHIFT METER (HP-IB: SHA3)

This function bypasses the ALC to allow direct control of the linear modulator circuit. In this mode, there is no limit on the minimum pulse repetition frequency.

1. Press **[SHIFT] [METER]**.

   ATN: X-xx dB, MOD: x.x dB appears in the ENTRY DISPLAY (x is the last-entered value).

2. Place the instrument in CW, or in pulse modulation mode with pulses wider than 2 μs.

3. Use the step keys to set the 90 dB attenuator, and the data entry keyboard, or the front panel knob, set the MOD (linear modulator):

   a. Set MOD entry at 0 dBm.

   b. Increment the ATN until the POWER dBm display shows a level of 5 to 15 dB higher than the desired output power.

   c. Reduce the power to the desired level by changing the MOD value.

Because the actual power changes very little as the pulse width is narrowed, even though the POWER dBm reading drops, at very narrow pulse widths ignore this reading.

The ATN and MOD values in the ENTRY DISPLAY also have a limitation:

Although the ATN displayed value is always accurate, MOD becomes saturated in the top 10 dB (approximately) of its range. At this point no change occurs in the true power. Because of this, rely on the POWER dBm display for the true power level instead of the MOD value.

SHIFT METER can also be used as a diagnostic function of the ALC circuits.

SHIFT PEAK (HP-IB: SHRP)

This is a more extensive version of peaking. PEAK, which requires a fraction of a second to implement, aligns the output filter with a single CW frequency; SHIFT PEAK aligns all of the YTM tracking calibration constants and requires 5 to 10 seconds to implement.

Use SHIFT PEAK to enhance the power output and spectral purity of swept modes, and to improve tracking performance (especially in harsh environments having wide temperature variations).

1. Press **[SHIFT] [PEAK]**.

   AUTO TRACKING appears in the ENTRY DISPLAY for 5 to 10 seconds. When the message disappears, the instrument has completed the power peaking function and updated working calibration constants.

SHIFT PWR SWEEP (HP-IB: SHPS)

This function decouples the 90 dB step attenuator (ATN) from the automatic leveling control (ALC). To recouple the attenuator and ALC loop, press **[POWER LEVEL]**.

SHIFT SLOPE (HP-IB: SHSL)

This function allows front panel control of the 90 dB step attenuator (ATN).

1. Press **[SHIFT] [SLOPE]**.

   ATN: xdB appears in the ENTRY DISPLAY (x is the last entered value).

2. Use the **[STEP]** keys or the data entry keyboard with any termination key to change the ATN value within the range 0 dB to −90 dB in 10 dB steps.

   Keyboard entries are rounded to the nearest 10 dB. The clicking sound heard after each attenuator change is the attenuator pad mechanically switching into the RF output path.

Assembly-Level Service
Overall Instrument Troubleshooting

If an instrument fails, first verify that the calibration constants in memory are good (see **CALIBRATION CONSTANTS**).

The troubleshooting information presented here will guide you to the appropriate functional group. Figures A-8 and A-9 show the proper sequence to follow to isolate specific symptoms. The following procedures are keyed to the numbers in these diagrams.

Table A-4 provides pin I/O references for all assemblies in the eight functional groups. If, while troubleshooting a particular functional group, indications imply a power supply problem, refer to Table A-4.

NOTE: If an instrument exhibits a problem in frequency or power output, flatness, accuracy, etc, ensure the problem is not caused by a misadjustment. Refer to section five, adjustments, if you suspect this may to be the cause of the problem.

SAFETY CONSIDERATIONS

Safety Symbols

Instruction manual symbol: the apparatus will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the apparatus against damage.

Indicates dangerous voltages.

Earth terminal (sometimes used in manual to indicate circuit connected to grounded chassis).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in injury or loss of life. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the equipment. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

Operation

CAUTION

BEFORE APPLYING POWER make sure the instrument's ac input is set for the available ac line voltage, that the correct fuse is installed, and that all normal safety precautions have been taken.

Service

The information, cautions, and warnings in this manual must be followed to ensure safe operation and to keep the instrument safe. SERVICE AND ADJUSTMENTS SHOULD BE PERFORMED ONLY BY QUALIFIED SERVICE PERSONNEL.

Adjustment or repair of the opened instrument with the ac power connected should be avoided as much as possible and, when unavoidable, should be performed only by a skilled person who knows the hazard involved.

Capacitors inside the instrument may still be charged even though the instrument has been disconnected from its source of supply

Make sure only fuses of the requred current rating and type (normal blow, time delay, etc.) are used for replacement. Fuse requirements are indicated on the instrument's rear panel. Do not use repaired fuses or short-circuit fuse holders.

Whenever it is likely that the protection has been impaired, make the instrument inoperative and secure it against any unintended operation.

WARNING

If this instrument is to be energized through an auto-transformer (for voltage reduction), make sure the common terminal is connected to the earthed pole of the power source.

BEFORE SWITCHING ON THE INSTRUMENT, the protective earth terminal of the instrument must be connected to the protective conductor of the (mains) power cord. The mains plug shall only be inserted in a socket outlet provided with protective earth contact. The protection action must not be negated by using an extension cord (power cable) without a protective grounding conductor. Grounding one conductor of a two-conductor outlet is not sufficient protection.

Any interruption of the protective (grounding) conductor, inside or outside the instrument, or disconnection of the protective earth terminal is likely to make this instrument dangerous. Intentional interruption of the earth ground is prohibited. Whenever it is likely that the protection has been impaired, the instrument must be secured against any unintended operation.

Servicing this instrument often requires that you work with the instrument's protective covers removed and with ac power connected. Be careful; the energy at many points in the instrument may, if contacted, cause personal injury.

WARNING

When the A19 power-on safety indicator LED is on, there are voltages present inside the instrument that can cause personal injury or death.

When the power switch is set to STANDBY, only the A52, A53, AND A56 regulators are biased off.

Never short a capacitor with a screwdriver or similar direct short. Either let the capacitor bleed off via normal instrument loads or provide a discharge path by applying a 0.5W, 100Ω resistor (via shielded clip leads) across the capacitor terminals.

CAUTION

To protect static sensitive components, troubleshoot this instrument only at a work station equipped with an anti-static surface, and wear a grounding strap. When handling a printed circuit board, hold it by the edges; never touch the finger contacts. Use low-static solder removal tools when desoldering components. Use only soldering irons that have a grounded tip.

DO NOT use silicone based thermal compound. Silicone based oil migrates past element sockets, switch contacts, or printed circuit board edge connectors, raising contact resistance, or electrically isolating the contacts. Silicone based thermal compounds disperse into the air, depositing themselves anywhere in the instrument. Heat increases the rate of dispersion.

Use only rosin mildly activated solder when repairing a printed circuit board. Rosin activated solder can cause reliability problems.

Cleaning solder flux from a printed circuit board after replacing a component causes serious reliability problems. When you replace a component, solder flux remains on the newly soldered feedthrough pads. Solder flux contains caustic rosin activating acids. If the residual rosin is left on the board undisturbed, the activators remain encapsulated (and harmless), but cleaning the rosin off (by any means) releases the caustic rosin activators and spreads them over the printed circuit board.

The caustic chemicals get under trace edges (all printed circuit board traces have undercuts along the edges from the etching process) and can not be washed out. In time, these chemicals react with the dissimilar metals in the trace (nickel, copper, gold), slowly dissolving the trace. The chemicals also create an electrical path between traces, causing metal-ion migration, which leads to high impedance shorts and dendrite growth.

NEVER clean PC board fingers with an eraser. NEVER use tap water in the cleaning solution. Chloride contamination from tap water, from salt (skin contact), or from any other source, can cause reliability problems. Always wear a ground strap when handling any internal component or assembly.

OVERALL INSTRUMENT TROUBLESHOOTING

The following diagram indicates the proper sequence to follow to isolate specific symptoms. Each of these is described in detail in the following pages. Several categories make references to the front and rear panel items shown in Figure A-9 on the facing page.

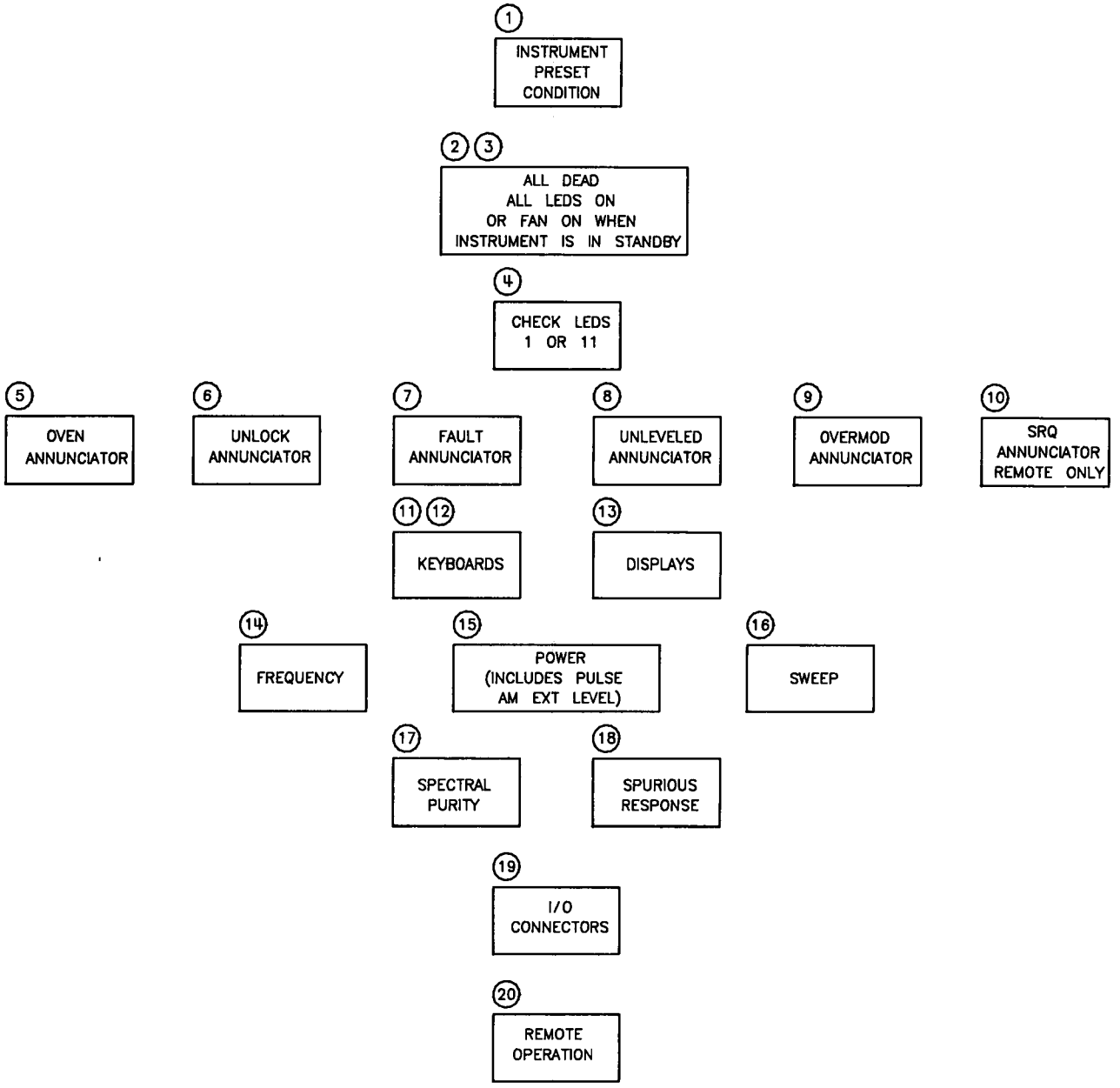


Figure A-8. Overall Instrument Troubleshooting Diagram

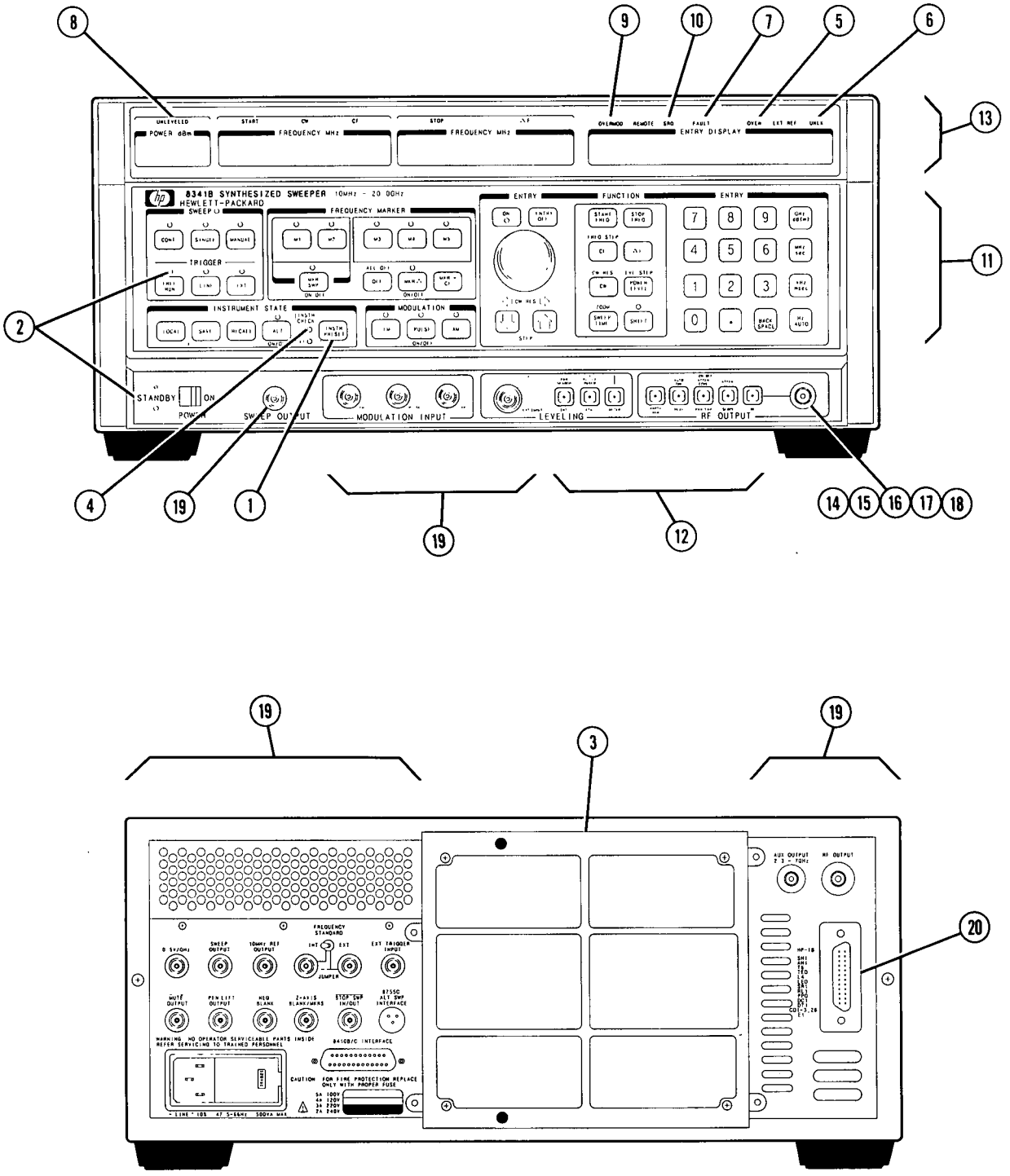


Figure A-9. Front and Rear Panel Items

INSTRUMENT PRESET CONDITIONS (1)

Press **[SHIFT] [INSTR PRESET]** and check that the following settings exist. If any instrument condition is not as shown below, the instrument requires service.

NOTE: Press **[SHIFT] [INSTR PRESET]** to eliminate any frequency multiplication factor locked into the instrument by earlier use of the SHIFT ALT function, and preset the instrument (see section three of this manual set for details.)

POWER dBm display = 0.0

Factory setting, determined by cal constant #56.

A different power level can be set by changing calibration constant #56 (see **Calibration Constant**).

FREQUENCY MHz display = 10.000000
START annunciator lit

FREQUENCY MHz display = 20.000000
STOP annunciator lit.

Factory setting. Calibration Constant #54 should always be set to a value of 20000 for the HP 8341B Option 003. If the stop frequency is wrong at instrument preset, check this calibration constant.

ENTRY DISPLAY = Blank (off)

SWEEP block = Green LED flashing

If the green LED is not flashing, the instrument is not sweeping and requires service.

CONT LED on

FREE RUN LED on

FREQUENCY MARKER block = All LEDs off

INSTRUMENT STATE block = All LEDs off

MODULATION block = All LEDs off

ENTRY block = All LEDs off

LEVELING block = **INT** LED on

RF OUTPUT block = **RF** LED on

The RF output should be a swept signal, leveled at 0 dBm. This signal should start at 10 MHz and stop at the maximum frequency of the instrument.

EXT REF annunciator = off.

If the rear panel INT or EXT REFERENCE switch is in the EXT position, the EXT REF annunciator above the ENTRY DISPLAY will be on.

All LEDs Off.

Fan is Operating. If all annunciators and LEDs are off (but the instrument's fan is operating), check that the fan is supplying proper airflow to the interior of the instrument.

Ensure that the fan filter is not blocked. If the airflow is good, suspect a failure in the instrument's power supply section.

Fan is Not Operating. Refer to the FAN section, below.

Some LEDs Off

If some LEDs that should be on are off, the front panel section is probably faulty.

All LEDs On

If all of the LEDs and annunciators are on, instrument processor, memory, or power supply is probably faulty.

Character March

If the four display windows have strings of characters marching across them, the instrument processor or memory is probably faulty.

INSTRUMENT APPEARS DEAD (2)

Fan is not Operating, LEDs Off at Power On

If all instrument LEDs are off and the fan is not operating, suspect a problem in the instrument causing complete loss of line power (line filter module, fuse, transformer, or wiring, related problems).

Check the line fuse and line filter module voltage select cam (see **POWER SUPPLIES – FAN** functional group).

FAN RUNS SLOWLY, ALL LEDS ON (But are dim)

Check that the proper voltage has been selected on the line module (see **POWER SUPPLIES – FAN** functional group).

FAN (3)

Fan Does Not Turn On

When the power switch is turned on, the instrument fan should start. If not, the fan, power supply, or K1 relay (inside the instrument, near the rear panel) is probably faulty.

If the instrument has run for some time with the fan not running, the interior temperature may have risen to the point that the A62S1 thermal switch has turned the instrument off. If so, all front panel LEDs will have gone off. The switch will reset itself when the instrument cools down.

Fan Does Not Turn Off

When the instrument is in the STANDBY mode, the fan should not run. If it is, the fan relay (K1) may be stuck, or the +22V supply has failed. The fan relay solenoid is energized when the instrument is in the STANDBY mode, turning the fan off. If the power to the relay solenoid fails (+22V supply), the solenoid de-energizes, turning the fan **on.**

INSTRUMENT CHECK LEDS REMAIN ON (4)

Instrument check LEDs I and II, located on the front panel adjacent to the **[INSTR PRESET]** key, indicate the results of self test. After switching the power on or pressing **[INSTR PRESET]**, the following occur:

1. Both LEDs turn on.
2. LED I turns off when the instrument processor determines it is operational, and has verified memory and the peripheral interface timer.
3. LED II goes off when the processor determines that the I/O address bus, I/O data bus, and the marker ram are operating.

If no failure occurs during self test, both INSTR CHECK LEDs go off after about 1 second. If either remain on, the instrument requires service. Refer to the controller section functional group for troubleshooting information.

NOTE: Instrument self test does not detect all instrument failures. If you suspect a problem and self test passes, perform the service diagnostic routine, SHIFT M4 (see **FRONT PANEL DIAGNOSTICS**).

OVEN ANNUNCIATOR (5)

The front panel OVEN light indicates the status of the internal frequency standard. When the OVEN annunciator is on, the frequency is more than 100 Hz from 10 MHz. The A51 assembly 10 MHz reference oscillator has an internal circuit that monitors the internal oven temperature. When the oven temperature is too low, the HOVC line is high (greater than +15V). When the oven temperature reaches the desired point (the frequency is within 100 Hz of 10 MHz), HOVC goes low (less than +15V). HOVC is sent to the A59 digital interface assembly where the microprocessor reads it and determines when to turn the light on or off.

The oven LED is located on the A2 display driver assembly, and is driven by the A3 display processor, annunciator latch/driver.

The LED is turned on by the instrument processor. The processor outputs the appropriate bits on the data bus, then outputs address 15:R0 to latch the data bits.

If the internal 10 MHz standard is used, the OVEN annunciator should go out within one-half hour after the instrument is connected to line power. If the annunciator stays on, the instrument requires service.

If the instrument is using an external 5 or 10 MHz standard, the OVEN annunciator indication has no effect on instrument performance.

UNLOCK ANNUNCIATOR (6)

NOTE: After performing the following procedure, use the SHIFT M4 diagnostic test to help isolate the cause of an UNLK condition.

The UNLK light indicates that that one or more of the six instrument phase lock loops is unlocked.

1. Press **[SHIFT] [EXT]**.

   OSC: REF M/N HET YO N2 N1 appears in the entry display.

   The name of the unlocked phase lock loop is flashing.

The different loops are listed below, with information about what to do if one of them is unlocked.

REF If reference loop is flashing, inspect the rear panel, one of two conditions should exist:

1. If the instrument is in internal 10 MHz mode:

   Check that the INT STANDARD BNC and the EXT STANDARD BNC are connected with a jumper cable (make sure the jumper cable is good). Ensure that the rear panel REFERENCE switch is in the INT position. If this is the case and REF is flashing, the instrument requires service. Suspect a problem in the reference loop.

2. If the instrument is in external 10 MHz mode:

   An external 10 MHz standard should be connected to the EXT STANDARD BNC with the rear panel REFERENCE switch in the EXT position. If this is the case and REF is flashing, connect the instrument as described in step 1, above. Press **[SHIFT] [EXT].**

   If REF continues to flash, the instrument requires service. Suspect a problem in the reference loop.

   If REF stops flashing, the problem is caused by the external 10 MHz reference standard.

If any of the following indicators are flashing, the instrument requires service:

M/N Suspect the M/N loop.
HET Suspect a problem in the 3.7 GHz oscillator in the RF section.
YO Suspect the YO loop.
N1 Suspect a problem in the PLL1 or PLL3 loops in the 20-30 loops.
N2 Suspect a problem in the PLL2 loop in the 20-30 loops.

Multiple Loops Unlocked

The loops relate to each other as follows:

- The REF loop generates reference signals required by all other loops.
- The YO loop uses signals generated by the M/N loop and the 20/30 loop.

The UNLK LED is located on the A2 display driver assembly, and is driven by the A3 display processor, annunciator latch/driver.

The LED is turned on by the instrument processor. The processor detects the unlock indication from the particular phase lock loop, outputs the appropriate bits on the data bus, and outputs address 15:R0 to latch the data bits.

FAULT ANNUNCIATOR (7)

NOTE: After performing the following procedure, use the SHIFT M4 diagnostic test to help isolate the cause of an FAULT condition.

The FAULT light monitors the status of the five internal functions described below.

1. If the FAULT light is on, press **[SHIFT] [MANUAL]**.

   FAULT: CAL KICK ADC PEAK TRK appears in the ENTRY DISPLAY.
   The name of the faulty function is flashing.

   CAL Refers to the calibration constants stored in memory. The calibration constants are checked only at instrument preset. If CAL is flashing, the instrument has resorted to default calibration constant data. The major effect of this condition is that RF power output flatness and accuracy are degraded.

   To remedy this situation, you must re-enter the the factory-determined calibration constants (see **HOW TO RESTORE FACTORY-OPTIMIZED CALIBRATION CONSTANTS**).

   KICK Refers to the kick pulses used to reset the YO (YIG oscillator) and SYTM (switched YIG-tuned multiplier). This fault is can be caused by a kick pulse that is too wide. suspect a problem with the kick pulse caused by the A54 YO pretune, A55 YIG oscillator driver (in the sweep generator-YO loop functional group), or the A28 SYTM driver assemblies (in the RF section functional group).

   ADC Refers to a check performed on the ADC (analog-to-digital converter) circuits on the A27 level control assembly. This check is done at instrument preset or at power on. ADC indicates that the POWER dBm display may indicate a different power than the instrument is actually producing. Also, an ADC failure does not allow the PEAK and auto tracking (SHIFT PEAK) functions to operate properly. If this annunciator is on, suspect a problem on the A27 level control assembly (see the RF section functional group).

   PEAK This refers to an instrument function that peaks the RF output power at a CW frequency by fine tuning the SYTM (which is tuned to the YO frequency). This fault can only come on if you press **[PEAK]**.

   If PEAK is flashing, something is wrong with the circuitry that peaks the SYTM. PEAK indicates that the instrument is not able to optimize its output power. While this instrument failure requires service to correct, the optimum power may not be adversely affected. Suspect the A28 SYTM driver or A27 level control assembly.

   TRK Refers to an instrument function that peaks the RF output power while the instrument is sweeping. This fault can only occur if you press **[SHIFT] [PEAK]**.

   The TRK light indicates the same things as a flashing PEAK.

The FAULT LED (located on the A2 display driver assembly) is driven by the A3 display processor, annunciator latch/driver circuit. The instrument microprocessor detects an error from the circuitry, outputs the appropriate bits to turn the LED on, and outputs address 15:R0 to latch the data bits.

UNLEVELED ANNUNCIATOR (8)

NOTE: After performing the following procedure, use the SHIFT M4 diagnostic test to help isolate the cause of an UNLEVELED condition.

The UNLEVELED light indicates the status of RF output power. If the UNLEVELED light is off, the output power is leveled; if the light is on, the power is unleveled.

1. Press **[SHIFT] [PEAK]**. This may solve the problem.
2. Make sure that the correct leveling mode is selected:

   Internal leveling = INT
   External leveling = XTAL
   Power Meter Leveling = METER

   If you are using an external millimeter-wave source module, you must press **[SHIFT] [XTAL],** and the ENTRY display should read: **EXT MODULE POWER: XX.XX dBm**.
3. Check that the power level requested is not greater than the maximum power specification at the given frequency. If the instrument is sweeping, make sure that the power requested does not exceed the maximum power specification for the entire band or bands that are swept.
4. If the output power is unleveled at all power levels and all frequencies, suspect an RF section problem (A25 ALC detector or the A26 linear modulator).
5. If the power levels at some frequencies and not others while the instrument sweeps, the SYTM may not be tracking correctly. Try the AUTO TRACKING (press **[SHIFT] [PEAK]**).
6. If the power levels at some CW frequencies and not at others, press **[PEAK]** to optimize the SYTM tracking at the frequency of interest.
7. If the power is unleveled in low band (10 MHz to 2.3 GHz) only, suspect a low band ALC or RF section problem.
8. If the power is unleveled in band 1 or above (2.3 GHz to the maximum frequency), suspect a high band ALC or RF section problem.

OVERMOD ANNUNCIATOR (9)

You can cause OVERMOD if you use FM with a modulation rate that is too high.

The other known causes of OVERMOD are internal instrument failures in the AM, pulse, or frequency modulation circuitry (refer to A26 linear modulator information in the RF section).

To determine if the instrument requires service:

1. Disconnect any cables going to the AM or FM inputs.
2. Press **[INSTR PRESET].** If the OVERMOD annunciator comes back on, the instrument requires service.

If the OVERMOD annunciator comes on only when a signal is input to the FM jack, The MODULATION INDEX (peak deviation in MHz/modulation rate in MHz) of the signal is significantly greater than the specified maximum (5).

The OVERMOD LED (located on the A2 display driver assembly) is driven by the A3 display processor, annunciator latch/driver circuit. The instrument microprocessor detects an error from the circuitry, outputs the appropriate bits to turn the LED on, and outputs address 15:R3 to latch the data bits.

SRQ ANNUNCIATOR (10)

What is a Service Request (SRQ)

An SRQ is used only when the instrument is connected to an external controller (via HP-IB). The controller programs the instrument to send an SRQ under certain conditions. When one of the programmed conditions occurs, the instrument sends out an SRQ signal and activates the SRQ annunciator. When the controller responds to the SRQ (by doing a serial poll command) the instrument turns the SRQ annunciator off. This entire process takes a fraction of a second, so the SRQ annunciator stays on only briefly.

SRQ Annunciator Stays On

If the SRQ annunciator goes on and stays on it usually indicates one of the following conditions:

If the SOURCE is Connected to an External controller. The computer controller is not able to service the SRQ interrupt. The controller is probably stuck in a loop, etc. This is usually not caused by a SOURCE fault.

If the SOURCE is Programmed by an External Controller and then Disconnected. A controller can be an external computer or HP 8756A, 8757A, or 8510 network analyzer. The SRQ annunciator stays on if a controller has programmed the SOURCE to send an SRQ, and is subsequently disconnected.

To clear this SRQ, press **[INSTR] [PRESET]** and then cycling the power switch to STANDBY and then ON.

The SRQ (located on the A2 display driver assembly) is driven by the A3 display processor, annunciator latch/driver circuit. The instrument microprocessor detects an error from the circuitry, outputs the appropriate bits to turn the LED on, and outputs address 15:R3 to latch the data bits.

UPPER KEYBOARD, LOWER KEYBOARD, DISPLAYS (11, 12, 13)

Refer to the front panel – rear panel functional group.

FREQUENCY (14)

If the UNLK annunciator is not on, and the RF output signal frequency is incorrect, refer to Section 4 Performance Test, Frequency Range and CW Mode Accuracy. This test checks all of the divider bits that program the various phase lock loops. The test indicates which phase lock loop is causing the problem and which bit or bits are incorrect. After you isolate the faulty loop, refer to the appropriate functional group troubleshooting.

POWER (15)

The RF output should meet the specifications for maximum leveled power, power accuracy, and flatness.

Maximum Leveled Power

For problems related to maximum leveled power, refer to **UNLEVELED ANNUNCIATOR**.

Flatness

NOTE: Before performing the following procedure, use the SHIFT M4 diagnostic test to help isolate the cause of an incorrect power condition.

1. The flatness adjustments in Section 5, Adjustments, improve overall flatness by varying the offset and slope correction factors. If the frequency response has large variations, the problem is probably in the associated RF path. Refer to the RF section functional group.
2. If the RF power level is low at 10 MHz and increases with frequency, suspect the RF output connector. This connector contains a series capacitor that can exhibit this symptom. To verify that the problem is the RF connector:
   a. Remove the front panel (see the front panel – rear panel functional group).
   b. Disconnect the SMA cable to the RF connector, and remove the RF connector.
   c. Measure the power level at the cable.

CAUTION

Be extremely careful when disconnecting or connecting an SMA cables from a mating 3.5 mm connector (RF attenuator). The SMA cable center conductor must align with the 3.5 mm connector center conductor. If there is any axial force on the cable when disconnecting the SMA fitting, the 3.5 mm connector center conductor can be damaged. Remove any axial force on the cable by first disconnecting the end of the cable that does not mate with the 3.5 mm connector, or by removing the mounting screws of the device having 3.5 mm connector.

Accuracy

Flatness is adjusted and tested with the RF output power at 0 dBm (RF attenuator at 0 dB and ALC at 0 dBm). The frequency response normally remains the same over the ALC range. For accuracy problems within the ALC range, refer to the ALC adjustments in Section 5, Adjustments, and to the RF section functional group if necessary.

If accuracy is within specifications over the ALC range, and out of specifications below the ALC range, the problems is probably associated with the RF attenuator. Note that the RF attenuator is outside of the ALC Loop. The instrument processor programs the RF attenuator, but there is no way for the processor to know if the attenuator actually stepped properly. If the power level is off by a factor of 10 dB, the attenuator may not be responding properly.

1. Select a CW frequency.
2. Set the power level to 0 dBM.
3. Press **[SHIFT] [PWR SWP]**.

   ATN: −00 dB, ALC: 0.00 dBm appears in the ENTRY display.
4. Using the step keys, step the RF attenuator (and RF power output) to −90 dB.

   The attenuator should click at each step, and the RF power should decrease in 10 dB steps. If the attenuator does not perform properly, refer to the RF section functional group.
5. There is an offset and slope calibration constant correction factor for each RF attenuator step from 10 to 90 dB. A printed copy of values generated at the last calibration should be located inside the instrument (see pocket along left side rail). Check the calibration constants in instrument memory against the printed copy values and restore the correct values, if necessary (see **HOW TO RESTORE FACTORY OPTIMIZED CALIBRATION CONSTANTS**).
6. If the attenuator is operating properly and the calibration constants are correct, check the RF connections from the A10 directional coupler to the RF attenuator and measure the power accuracy at the attenuator output.

SWEEP (16)

1. Make sure nothing is connected to the rear panel stop sweep connector.

NOTE: Before performing the following steps, use the SHIFT M4 diagnostic test to help isolate the cause of a sweep problem.

For sweep problems, refer to the sweep generator − YO loop functional group troubleshooting. Use the following information to further define the symptom.

The following steps assume the instrument works properly in CW mode (no UNLK indication).

2. Press **[INSTR PRESET]** and check for the following sweep indications:

   a. Check front panel SWEEP LED. The LED should be blinking.

      The sweep LED, which is turned on at start of sweep, off at each bandcross, and at end-of-sweep, is controlled by LSPLD (low sweep LED). The sweep LED is turned on when HSP (high start sweep) is low, LRSP (low reset sweep) is high, and LBX (low bandcross) is high.

   b. Check the SWEEP OUT signal.

      The sweep outputs come from the A57 marker/bandcross assembly, and are generated from the MKR RMP. For a detailed description of the SWEEP OUT or MKR RAMP waveform, refer to the sweep generator/YO loop functional group.

      If the sweep out waveform is normal, the A58 assembly ramp generator is good, the WSPTM (write sweep time) strobe is generated, and LRESET (low reset) is working.

   c. Check rear panel 0.5V/GHz waveform.

      The 0.5V/GHz signal comes from the A28 SYTM driver assembly, and is generated by the PRETUNE signal, which is generated from VSWP.

      If the rear panel 0.5V/GHz signal is normal, VSWP and PRETUNE are working.

NOTE: For sweep widths <5 MHz (20/30 sweeps), 0.5V/GHz is fixed.

SPECTRAL PURITY / HARMONICS (17, 18)

NOTE: In this section, spectral purity is considered a phase noise problem and spurious responses are considered to be discrete harmonics.

Phase Noise

This procedure assumes the instrument failed the Single Sideband Phase Noise test, in Section 4.

1. If the SOURCE failed the test at offset frequencies less than 300 Hz, the problem is most likely the 100 MHz Reference section. Refer to the reference loop – M/N loop.

   a. Replace the 400 MHz input to A31 M/N phase detector (J1) using a very stable source. Use the HP 8662A frequency standard as the SOURCE frequency standard EXT input.

   b. Repeat the failed test. If the SOURCE now passes the test, the problem is in the SOURCE's reference loop.

2. If the SOURCE failed the phase noise test at offset frequencies from 300 Hz to 50 kHz, the problem is most likely the M/N loop.

   a. You can use an external source to replace the M/N input to the YO loop, but the external source phase noise would have to be much better than the SOURCE's phase noise to eliminate the YO Loop.

   b. Replace the reference loop 400 MHz input to the M/N loop as described in step 1.

c. If the SOURCE continues to fail the phase noise test, the problem is most likely the M/N VCO.

3. If the SOURCE failed the phase noise test at offset frequencies greater than 50 KHz, the problem is most likely the YO Loop.

Spurious Response

This procedure assumes that the SOURCE failed the Spurious Response test in Section 4. Spurious responses can be divided into four categories:

Harmonics/Sub-harmonics

The SOURCE is essentially three instruments in one:

1. A heterodyning (low band) source
2. An unmodified YIG oscillator source (band 1)
3. A synthesized source (full band sweep).

In low band (10 MHz to 2.3 GHz), the 2.3 to 7.0 GHz YO output is mixed with a fixed 3.7 GHz oscillator to produce the RF frequency.

In high band, the YO output is used directly or multiplied (by the band number) to produce the RF frequency.

In high band, the SYTM is designed to pass only the RF output frequency and reject all other frequencies.

In low band, the output of the low band mixer passes directly through the SYTM.

To troubleshoot for harmonics and sub-harmonics in low band (10 MHz to 2.3 GHz), use a spectrum analyzer and troubleshoot the low band circuitry.

If the instrument does not meet its harmonic/sub-harmonic specification in high band, suspect the SYTM.

Line Related Side Bands

Line related spurs result when magnetic radiation from the power transformer is coupled into the M/N loop, the reference oscillator, or the SYTM.

The amplitude of a line related spur coupled into the M/N loop is greatest at 6.9 GHz (maximum M/N loop frequency); the amplitude of a line related spur coupled into the SYTM is greatest at 2.3 GHz (minimum SYTM drive current).

An increase in line voltage, or the line voltage selector PC can incorrectly installed can increase the radiation and, consequently, the spur amplitude.

1. Check the waveform on the unregulated power supplies.

   These supplies have full-wave bridge rectifiers. If one diode is open, the supply operates similar to a half-wave rectifier. The output of the regulated supplies can be normal, but the transformer current is unbalanced, and the magnetic radiation can increase.

Magnetic radiation coupled into the M/N Loop can sometimes be reduced by replacing A29U1 (The amplifier limiter on the reference phase detector assembly).

Squegging (≥7 GHz)

1. While changing the SOURCE output power level, observe the spurious response on a spectrum analyzer.

   If the frequency of the spur changes with power level, suspect squegging. Refer to the SRD Bias adjustments in Section 5.

Synthesized Spurs

NOTE: For proper shielding, the screws on the 20/30 and M/N section covers must be tight.

The SOURCE uses several internal oscillators to generate the desired output frequency. All the possible output frequencies can be described by the following equation:

$$Fout = k1*F1 + k2*F2 + k3*F3 .....$$

k1, k2, and k3 are integers (positive or negative) and F1, F2, and F3 are the frequencies of the internal oscillators. Because F1, F2, and F3 are phase locked to the internal reference (10 MHz standard), they are related to the reference frequency by:

$$F1 = Ref*I1/J1 \quad F2 = Ref*I2/J2 \quad F3 = Ref*I3/J3$$

The I's and J's are integers. The combination of these shows the relationship of the output frequency to the reference frequency:

$$Fout = Ref * (k1*I1/J1 + k2*I2/J2 + k3*I3/J3 ...)$$

The intended output frequency is the result of only one set of integers in the above equation. Spurs are possible at all other integer choices. These choices are normally eliminated through careful use of filtering, attention to signal levels, shielding, etc.

A Spur Family. A spur family is characterized by having the same mixing path through the instrument. For example, if the 5th harmonic of the M/N VCO is mixing with the 9th harmonic of the 20/30 output, the location of the spur can be predicted as the 20/30 frequency is changed. More spurs in this family can be hypothesized, such as the 9th 20/30 harmonic with the 6th M/N harmonic. The common thread is that the M/N VCO mixes with the 20/30 to cause a spur.

Synthesized spurs normally show up as phase modulations of the YO frequency. As the spur frequency is changed (by changing the carrier frequency), its amplitude remains constant as long as the offset from carrier remains less than the YO loop bandwidth (50 kHz). Beyond the YO loop bandwidth, the amplitude decreases until the spur is gone.

Synthesized spurs are called crossing spurs, and are possible when the harmonic frequencies of any two oscillators are equal (5th harmonic of 20 MHz = 4th harmonic of 25 MHz). A characteristic of crossing spurs is that the offset of the spur from the carrier changes as the carrier is moved. Because of this, there is a frequency at which the offset must be zero (assuming the sources of the spurs can be tuned to this frequency). This frequency is called the crossing frequency of the spur. The ratio of the change in spur offset to the change in carrier frequency is called the order.

Names can be assigned to the different spur families, such as type A, B, C1, C2, C3, etc. Each of these have a set of defining conditions to determine the crossing frequencies.

Type B, caused by the 20/30 mixing with the Ith harmonic of 10 MHz in the reference phase detector.

Type B, crossing frequency whenever:

10*Flf/10 = I or Flf = I
where Flf = 20/30 loop output frequency
ORDER of the spur = 10

Type C1 and C3 are both due to the 20/30 output and its harmonics mixing with the M/N VCO.

Given:
Fmn = M/N Output frequency = 200 − 10*M/N (MHz)
Flf = 20/30 Output Frequency = 20 to 30 (MHz)
M, N are the divider numbers for the M/N Loop
I, J, K are integers

Type C1, crossing frequency when:
Fmn/Flf = I/2 or Flf = 20 * (20-M/N)/I
ORDER of spur = I/2

This type of spur can be caused by several factors, such as the A48 sampler assembly 70 MHz low pass filter, or the A46 low pass filter assembly.

Type C3, crossing frequency when:
Fmn/Flf = 20*I ± J/(2*K)
or
Flf = 20 * K * (20-M/N)/20*I ± J
ORDER of spur = 20*I ± J/(2*K)

This type is caused by the Ith harmonic of the PLL1 VCO sampled by the Kth harmonic of the M/N VCO.

For any CW frequency, selecting the appropriate SHIFT functions displays the M/N frequency, 20/30 frequency, and YO frequency. A synthesized spurious response must be a function of these signals. Any coupling from one signal path into another can result in a spurious response (i.e., loose connectors, poor shielding, cable routing, etc.).

Low band spurs are caused by mixing products in the low band mixer. Because these are not crossing spurs (they are not YO loop sidebands), they are added to the output as part of the down-conversion process. The YO output should mix with the 3.7 GHz oscillator output and produce a single mixer output at F_{yo} − 3.7 GHz, but, harmonics of both oscillators are present, or are generated in the mixer. These mix to form spurs on the output.

Troubleshooting synthesized spurs.

1. To eliminate various RF paths, determine the YO frequency at which the spur occurs and select a CW frequency in both low band and band 1 that uses that YO frequency.

   If the spur occurs only in low band, troubleshoot the low band RF path. If the spur occurs only in band 1, troubleshoot the high band RF path.

2. Using the equations above, change the CW frequency so that the M/N output remains constant and only the 20/30 output changes.

3. Determine the order of the spur (i.e. ratio of YO frequency change to spur frequency change).

   If the spur is a crossing spur, at some point the spur will be on top of the YO frequency and at some point (50 kHz away from the YO frequency) the spur amplitude will decrease. If the spur is a crossing spur, refer to the appropriate spur family type above.

4. To determine which internal frequency source(s) is generating the spur:

   a. Change the CW frequency while monitoring the SHIFT function diagnostics, looking for a sudden change in spur frequency and/or amplitude. For example, press **[SHIFT] [M1]**, then change the CW frequency. Look for a correlation between any sudden change in spur frequency and/or amplitude with a change in M/N output frequency or 20/30 output frequency.

      If a sudden change in the spur occurs at the same time the M/N or 20/30 makes a large change, the internal frequency source that changed is probably one of the signals generating the spur.

   b. If you suspect the 20/30, press **[SHIFT] [M3]** to display the PLL2 VCO frequency and PLL3 up converter frequency and repeat the above test.

NOTE: For more information on the diagnostic modes, refer to the Frequency Range and CW Mode Accuracy test in Section 4, Performance Tests.

I/O CONNECTORS (19)

To determine source or destination of input or output connector signals, and for troubleshooting information, refer to the front panel — rear panel functional group.

REMOTE OPERATION (20)

Section 4, Performance Tests, contains an HP-IB Operation Verification Program Listing. This program verifies the ability of the instrument to respond to a remote input (complete HP-IB handshake). The program tests each data bit and reads the instrument status bytes.

If the instrument exhibits a problem while running this test, refer to the controller section functional group.

If you do not see a problem while running this program, and the instrument does not respond properly to other remote commands, refer to the computer documentation to read the computer HP-IB I/O card status. By outputting the I/O card status, the source of the problem can be determined.

Assembly-Level Service Repair Procedures

HOW TO CLEAN PRINTED CIRCUIT BOARD FINGERS

1. Mix one part de-ionized (or de-chlorinated) water with two parts isopropyl alcohol.
2. Apply this solution to a clean, lint free, cloth (HP Part Number 9310-0039 CD3).
3. Rub the PC board fingers carefully, then dry them with a clean part of the cloth.

MODULE EXCHANGE PROGRAM

The module exchange programs lets you exchange specified microcircuits for fully tested and guaranteed restored-exchange modules at a reduced price (contingent on the return of the defective microcircuit).

For detailed information on the module exchange service and how to use it, see the RF section functional group (replaceable parts).

Assembly-Level Service
After Service Safety Checks

VISUAL INSPECTION

Visually Inspect the interior of the instrument for any signs of abnormal internally generated heat, such as discolored printed circuit boards or components, damaged insulation, or evidence of arcing. If you find any signs of abnormal heat, determine and remedy the cause.

CHECK LINE CORD GROUND

Using a suitable ohmmeter, check the resistance from the instrument enclosure to the ground pin on the power cord plug. The reading must be less than 1Ω. Flex the power cord while making this measurement to determine whether intermittent discontinuities exist.

If the resistance is greater than 1Ω, replace the faulty line cord.

CHECK THE LINE/NEUTRAL

With the instrument disconnected from line power, and the line switch on, check the resistance from the instrument enclosure to the line and neutral (tied together). The resistance must be at least 2 MΩ.

If the resistance is less than 2 MΩ, **DO NOT CONNECT THE INSTRUMENT TO LINE POWER!** Troubleshoot the source of the problem.

CHECK THE LINE FUSE

Verify that a correctly rated fuse is installed, and the line module voltage selector cam is set properly.

AIR FILTER REPLACEMENT

CAUTION

To retain the instrument safety features, periodically perform the following procedure.

The air filter (HP Part Number 08340-00018 for a package of 10), attached to the rear panel cooling fan assembly requires periodic replacement. The time between filter replacements varies because of the variety of environmental conditions in which they operate. These filters are inexpensive, and cannot be cleaned. Replace as follows:

1. Disconnect the line power cord.
2. Remove four screws holding the air filter housing to the rear panel.
3. Replace the filter and reassembly.

A62J1 Pin	Mnemonic	A62W1P1	A62W1P2	Levels
1 2	GND PLANE +12V	PIN 1 PIN 2	PIN 1 PIN 2	0V +12V
3 4	DB0 DB1	PIN 3 PIN 4	PIN 3 PIN 4	TTL TTL
5 6	DB2 DB3	PIN 5 PIN 6	PIN 5 PIN 6	TTL TTL
7 8	DB4 DB5	PIN 7 PIN 8	PIN 7 PIN 8	TTL TTL
9 10	DB6 DB7	PIN 9 PIN 10	PIN 9 PIN 10	TTL TTL
11 12	DB8 DB9	PIN 11 PIN 12	PIN 11 TTL	TTL
13 14	DB10 DB11	PIN 13 PIN 14	PIN 13 PIN 14	TTL TTL
15 16	DB12 DB13	PIN 15 PIN 16	PIN 15 PIN 16	TTL TTL
17 18	DB14 DB15	PIN 17 PIN 18	PIN 17 PIN 18	TTL TTL
19 20	LIPS LSBY	PIN 19 NOT USED	PIN 19 PIN 20	TTL (LOW TRUE) 0V TO +22V
21 22	GND PLANE HPUP	NOT USED NOT USED	PIN 21 NOT USED	0V TTL (HIGH TRUE)
23 24	ADR0 ADR1	PIN 23 PIN 24	PIN 23 PIN 24	TTL TTL
25 26	ADR2 ADR3	PIN 25 PIN 26	PIN 25 PIN 26	TTL TTL
27 28	ADR4 LSTEPUP	PIN 27 NOT USED	PIN 27 PIN 28	TTL TTL (LOW TRUE)
29 30	GND PLANE +22V	PIN 29 NOT USED	PIN 29 PIN 30	0V +22V
31 32	+5.2V +5.2V	PIN 31 PIN 32	PIN 31 PIN 32	+5.2V +5.2V
33 34	+5.2V +5.2V	PIN 33 PIN 34	PIN 33 PIN 34	+5.2V +5.2V
35 36	+5.2V +5.2V	PIN 35 PIN 36	PIN 35 PIN 36	+5.2V +5.2V
37 38	+5.2V GND PLANE	NOT USED NOT USED	PIN 37 PLIN 38	+5.2V 0V
39 40	GND PLANE GND PLANE	PIN 39 NOT USED	PIN 39 PIN 40	0V 0V
41 42	GND PLANE −5.2V	NOT USED PIN 42	PIN 41 PIN 42	0V −5.2V
43 44	LSTP LSPLD	NOT USED NOT USED	NOT USED PIN 44	TTL (LOW TRUE) TTL
45 46	LSRQ GND PLANE	NOT USED NOT USED	PIN 45 PIN 46	TTL (LOW TRUE) 0V
47 48	SIOB GND PLANE	NOT USED PIN 48	PIN 47 PIN 48	TTL (LOW TRUE) 0V
49 50	ISOA GND PLANE	PIN 49 PIN 50	NOT USED PIN 50	TTL (LOW TRUE) 0V

Note: Refer to A62 motherboard wiring list for signal source and destination information.

A12 Pin I/O

Pin	Mnemonic	A12W1P1	Levels
1	THERM 2	PIN 1	−10V
2	LDETBW	PIN 2	TTL (LOW TRUE)
3	THERM 1	PIN 3	1V TO −8V

Note: Refer to RF Section Schematic Diagram and A62 motherboard wiring list for signal source and destination information.

A13 Pin I/O

Pin	Mnemonic	A13A1J1	Levels
1			
2	SRD BIAS	PIN 2	−10V/THRU 2000 OHMS TO +5V
3			
4	SYTM COIL −	PIN 4	−40V TO −25V
5	SYTM TEMP	PIN 5	+100 mV/°C
6	+20V	NOT USED	+20V
7	−10V	NOT USED	−10V
8	+20V	PIN 8	+20V
9	−10V	PIN 9	−10V
10	PINBIAS	PIN 10	−4V TO +12V
11			
12	STYM COIL −	PIN 12	−40V
13	SYTM GND	NOT USED	0V
14	SYTM GND	PIN 14	0V
15	SYTM GND	PIN 15	0V
16			

Note: Refer to RF Section Schematic Diagram and A62 motherboard wiring list for signal source and destination information.

A16/A20 Pin I/O

A62J19 Pin	Mnemonic	A62W31P2 Pin	A62W31P3 Pin	A16A1J1 Pin	A20J1	Levels
1	GND PLANE	1	1	1	1	0V
2	+20V	2	NOT USED	NOT USED	2	+20V
3	+5.2V	3	3	3	3	+5.2V
4	−5.2V	4	4	4	4	−5.2V
5	−10V	5	NOT USED	NOT USED	5	−10V
6	−40V/−40V SENSE (−)	6	NOT USED	NOT USED	6	−40V
7	LHET	7	NOT USED	NOT USED	7	TTL (LOW TRUE)
8	LHET	8	NOT USED	NOT USED	8	TTL (LOW TRUE)
9	GND PLANE	9	9	9	9	0V
10	+20V	10	NOT USED	NOT USED	10	+20V
11	+5.2V	11	11	11	11	+5.2V
12	−5.2V	12	12	12	12	−5.2V
13	−10V	13	NOT USED	NOT USED	13	−10V
14	−.25V/GHZ	NOT USED	NOT USED	NOT USED	NOT USED	
15	LHIBND	NOT USED	15	15	NOT USED	
16	HULH	16	NOT USED	NOT USED	16	TTL (HIGH TRUE)

Note: Refer to RF Section Schematic Diagram and A62 motherboard wiring list for signal source and destination information.

A19 Pin I/O

Pin	Mnemonic	Levels	Source	Destination
1	+20V AC1	+20 VAC	A62 LUG (2)	*A
13	+20V AC1	+20 VAC	A62 LUG (2)	*A
2	+20V AC2	+20 VAC	A62 LUG (2)	*A
14	+20V AC2	+20 VAC	A62 LUG (2)	*A
3	−10V AC1	−10 VAC	A62 LUG (6)	*B
15	−10V AC1	−10 VAC	A62 LUG (6)	*B
4	−10V AC1	−10 VAC	A62 LUG (6)	*B
16	−10V AC1	−10 VAC	A62 LUG (6)	*B
5	−10V AC2	−10 VAC	A62 LUG (6)	*6
17	−10V AC2	−10 VAC	A62 LUG (6)	*B
6	−10V AC2	−10 VAC	A62 LUG (6)	*B
18	−10V AC2	−10 VAC	A62 LUG (6)	*B
7	−10V RETURN	+6.4V AT 13.3 GHZ	XA53P1-2, 20	B C
19	−10V RETURN	+6.4V AT 13.3 GHZ	XA53P1-2, 20	B C
8	−10V RETURN	+6.4V AT 13.3 GHZ	XA53P1-2, 20	B C
20	−10V RETURN	+6.4V AT 13.3 GHZ	XA53P1-2, 20	B C
9	+20V UNREG	+31.2V	XA35P1-7, 25	*A
21	+20V UNREG	+31.2V	XA35P1-7, 25	*A
10	GND	0V	A62 STAR GND	*A
22	GND	0V	A62 STAR GND	*A
11	−10V UNREG	−10V	B C	XA53P1-27, 28
23	−10V UNREG	−10V	B C	XA53P1-27, 28
12	−10V UNREG	−10V	B C	XA53P1-27, 28
24	−10V UNREG	−10V	B C	XA53P1-27, 28

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A62 motherboard wiring list for a complete representation of signal sources and destinations.

A20 Pin I/O

A62J19 Pin	Mnemonic	A62W31P2 Pin	A62W31P3 Pin	A16A1J1 Pin	A20J1	Levels
1	GND PLANE	1	1	1	1	0V
2	+20V	2	NOT USED	NOT USED	2	+20V
3	+5.2V	3	3	3	3	+5.2V
4	−5.2V	4	4	4	4	−5.2V
5	−10V	5	NOT USED	NOT USED	5	−10V
6	−40V/−40V SENSE (−)	6	NOT USED	NOT USED	6	−40V
7	LHET	7	NOT USED	NOT USED	7	TTL (LOW TRUE)
8	LHET	8	NOT USED	NOT USED	8	TTL (LOW TRUE)
9	GND PLANE	9	9	9	9	0V
10	+20V	10	NOT USED	NOT USED	10	+20V
11	+5.2V	11	11	11	11	+5.2V
12	−5.2V	12	12	12	12	−5.2V
13	−10V	13	NOT USED	NOT USED	13	−10V
14	−.25V/GHZ	NOT USED	NOT USED	NOT USED	NOT USED	
15	LHIBND	NOT USED	15	15	NOT USED	
16	HULH	16	NOT USED	NOT USED	16	TTL (HIGH TRUE)

Note: Refer to RF Section Schematic Diagram and A62 motherboard wiring list for signal source and destination information.

Pin	Mnemonic	Levels	Source	Destination
1 19	HADCEN BIAS S/H PULSE	TTL (HIGH TRUE) TTL	D A	XA27P1-8 XA22P1-8
2 20	LMODHLD	TTL	E	XA26P1-1
3 21	DET S/H + DET S/H −	+4.5V/+3.5V +3.5V/+4.5V	F F	XA25P1-2 XA25P1-24
4 22 5 23	+20V +20V +5.2V +5.2V	+20V +20V +5.2V +5.2V	XA52P1-16, 40 XA52P1-16, 40 XA52P1-17, 18, 41, 42 XA52P1-17, 18, 41, 42	*G *G *G *G
6 24	HLBW	TTL (HIGH TRUE)	XA26P1-33	XA26P1-33
7 25	−10V −10V	−10V −10V	XA53P1-12, 13, 31, 32 XA53P1-12, 13, 31, 32	*G *G
8 26	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*G *G
9 27	HPLSEN HRFON	TTL (HIGH TRUE) TTL (HIGH TRUE)	XA26P1-2 XA57P1-105	*A *A C
10 28				
11 29	LHET	TTL (LOW TRUE)	XA27P1-20	*C
12 30				
13 31				
14 32				
15 33				
16 34	LOPMOD DRV	CURRENT SOURCE	C	A62J10-SMC CENTER
17 35	PLS IN RTN PMOD RTN	0V PV	* B	*A *A
18 36	PLS IN HIPMOD DRV	TTL CURRENT TO PIN DIODE	A62J26-SMC CENTER C	A A62J25-SMC CENTER

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A62 motherboard wiring list for a complete representation of signal sources and destinations.

Pin	Mnemonic	Levels	Source	Destination
1 19	+20V +20V	+20V +20V	XA52P1-16,40 XA52P1-16,40	*F *F
2 20	+5.2V +5.2V	+5.2V +5.2V	XA52P1-17,18,41,42 XA52P1-17,18,41,42	*F *F
3 21				
4 22	−10V −10V	−10V −10V	XA53P1-12,13,31,32 XA53P1-12,13,31,32	*F *F
5 23	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*F *F
6 24	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*F *F
7 25	SYTM TEMP HLB0	+100 mV/ °C TTL (HIGH TRUE)	A13J1-5 XA27P1-46	E D
8 26	BIAS S/H PULSE HLB1	TTL TTL (HIGH TRUE)	XA21P1-19 XA27P1-16	B D
9 27	HLB2	TTL (HIGH TRUE)	XA27P1-47	NOT USED
10 28				
11 29	VIDEO DET VIDEO DET RTN	ANALOG 0V	A14J21-SMC CENTER A14J21-SMC SHIELD	C C
12 30	LHET +1.4V/GHz	TTL (LOW TRUE) 1.4V/GHz	XA27P1-20 XA28P1-7	E D
13 31	SRD BIAS	−10V TO +5V (THROUGH 2K)	E	A62J18-10
14 32				
15 33				
16 34	MODHI	CURRENT SOURCE	A	A62J13-SMC CENTER
17 35	HRFON SYTM GND	TTL (HIGH TRUE) 0V	XA57P-105 A62J18-13,14,15	*A *E
18 36	REFGND	0V	A62 STAR GND	*F

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A62 motherboard wiring list for a complete representation of signal sources and destinations.

Pin	Mnemonic	Levels	Source	Destination
1 19	+20V +20V	+20V +20V	XA52P1-16, 40 XA52P1-16, 40	*G *G
2 20				
3 21	+5.2V +5.2V	+5.2V +5.2V	XA52P1-17, 18, 41, 42 XA52P1-17, 18, 41, 42	*G *G
4 22	LOMD	TTL (LOW TRUE)	*F	XA27P1-48
5 23	−10V −10V	−10V −10V	XA53P1-12, 13, 31, 32 XA53P1-12, 13, 31, 32	*G *G
6 24	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*G *G
7 25	−40V	−40V	XA53P1-11, 30	*G
8 26				
9 27	DB0 DB1	TTL TTL	XA60P1-20 XA60P1-76	E E
10 28	DB2 DB3	TTL TTL	XA60P1-21 XA60P1-77	E E
11 29	DB4 DB5	TTL TTL	XA60P1-22 XA60P1-78	E E
12 30	DB6 DB7	TTL TTL	XA60P1-23 XA60P1-79	E E
13 31				
14 32				
15 33	W11R2	TTL (LOW TRUE)	XA27P1-15	E
16 34	FMDRVR OUT FMDRVR SHIELD	ANALOG 0V	D GND2 G	A44A1J3
17 35	FM SHIELD	0V	GND1 G	J22 SHIELD
18 36	FM INPUT	−8V TO +8V	J22	A

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A62 motherboard wiring list for a complete representation of signal sources and destinations.

A24 Pin I/O

Pin	Mnemonic	Levels	Source	Destination
1 19	+20V +20V	+20V +20V	XA52P1-16, 40 XA52P1-16, 40	*L *A13J1-8
2 20	−10V HLB0	−10V TTL (HIGH TRUE)	XA53P1-12, 13, 31, 32 XA27P1-46	*A13J1-9 *C
3 21	+5.2V HLB1	+5.2V TTL (HIGH TRUE)	XA52P1-17, 18, 41, 42 XA27P1-16	*L *C
4 22	STAT10 HLB2	TTL (LOW TRUE) TTL (HIGH TRUE)	XA23P1-22 XA27P1-47	H *C
5 23	−10V RSTAT	−10V TTL (LOW TRUE)	XA53P1-12, 13, 31, 32 XA27P1-45	*L *H
6 24	PIN BIAS	−4V TO +12V	G	A62J18 PIN 10
7 25	ATN COIL +	+5V	L	A62J20 PIN 6
8 26	GND GND PLANE	0V 0V	A62 STAR GND INSTRUMENT GND	*L *L
9 27	ATNTH4 ATNAT4	OPEN COLLECTOR OPEN COLLECTOR	J J	A62J20 PIN 4 A62J20 PIN 20
10 28	ATNTH3 ATNAT3	OPEN COLLECTOR OPEN COLLECTOR	J J	A62J20 PIN 11 A62J20 PIN 5
11 29	ATNTH2 ATNAT2	OPEN COLLECTOR OPEN COLLECTOR	J J	A62J20 PIN 3 A62J20 PIN 9
12 30	ATNTH1 ATNAT1	OPEN COLLECTOR OPEN COLLECTOR	J J	A62J20 PIN 13 A62J20 PIN 2
13 31	HENDKICK	TTL (HIGH TRUE)	XA28P1-18	H
14 32	DB9 DB11	TTL TTL	*H *H	* *I
15 33	DB10 WLEVEL	TTL TTL (LOW TRUE)	*H XA27P1-12	*I I
16 34	DB12 DB13	TTL TTL	*H *H	*I *I
17 35				
18 36				

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A62 motherboard wiring list for a complete representation of signal sources and destinations.

A25 Pin I/O

Pin	Mnemonic	Levels	Source	Destination
1 23				
2 24	DET S/H + DET S/H −	+4.5/+3.5V +3.5/+4.5V	XA21P1-3 XA21P1-21	C C
3 25	HPLSEN	TTL (HIGH TRUE)	XA26P1-2	*NOT USED
4 26	THERM 1 THERM 2	−1V TO −8V −10V	A62J34-3 A62J34-1	A A
5 27	+20V +20V	+20V +20V	XA52P1-16, 40 XA52P1-16, 40	*H *H
6 28	+5.2V +5.2V	+5.2V +5.2V	XA52P1-17, 18, 41, 42 XA52P1-17, 18, 41, 42	*NOT USED *NOT USED
7 29	−10V −10V	−10V −10V	XA53P1-12, 13, 31, 32 XA53P1-12, 13, 31, 32	*H *H
8 30				
9 31	GND GND	0V 0V	A62 STAR GND A62 STAR GND	* *
10 32	GND DETOUT	0V −30mV/dB, 0V = 0dBm	A62 STAR GND F	* XA26P1-10
11 33	DETLVL	−200mV/dB, 0v = 0dBm	D	XA27P1-29
12 34	RGND RGND	0V 0V	STAR GND POINT STAR GND POINT	*H *H
13 35	LVLREF TCREF	0.2V/dB, 0V = 0dBm −200mV/dB, 0V = 0dBm	XA27P1-30 G	G XA26P1-12
14 36	LVLCOR HMTR	+1.25dB/VOLT, 0V = 0dB TTL (HIGH TRUE)	B XA26P1-13	XA27P1-62 A F
15 37	LHET	TTL (LOW TRUE)	XA27P1-20	*A
16 38				
17 39	LDETBW	TTL (LOW TRUE)	XA26P1-9	*NOT USED
18 40				
19 41				
20 42	HINT	TTL (HIGH TRUE)	XA26P1-42	F
21 43	EXDETR	0V	*	E
22 44	EXDET	0.5mV − 2V	A26J16 SMC CENTER	E

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A62 motherboard wiring list for a complete representation of signal sources and destinations.

A26 Pin I/O

Pin	Mnemonic	Levels	Source	Destination
1 23	LMODHLD LHIBND	TTL TTL (LOW TRUE)	XA21P1-2 D	B A62J19 PIN 15
2 24	HPLSEN HRFON	TTL (HIGH TRUE) TTL (HIGH TRUE)	E XA57P1-105	* *B
3 25	+20V +20V	+20V +20V	XA52P1-16, 40 XA52P1-16, 40	*H *H
4 26	+5.2V +5.2V	XA52P1-17, 18, 41, 42 +5.2V	*H XA52P1-17, 18, 41, 42	 *H
5 27	−10V −10V	−10V −10V	XA53P1-12, 13, 31, 32 XA53P1-12, 13, 31, 32	*H *H
6 28	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
7 29	HSP HLB0	TTL (HIGH TRUE) TTL (HIGH TRUE)	XA57P1-13 XA27P1-46	* *F
8 30	LOMD HLB1	TTL (LOW TRUE) TTL (HIGH TRUE)	C XA27P1-16	XA27P1-48 *F
9 31	LDETBW HLB2	TTL (LOW TRUE) TTL (HIGH TRUE)	E XA27P1-47	*XA25P1-39 *F
10 32	DETOUT MODLVL	−30mV/dB, 0V = 0dBm 0V TO −3V (LEVELED)	XA25P1-32 B	B XA27P1-61
11 33	RGND HLBW	0V TTL (HIGH TRUE)	STAR GND POINT E	*H XA21P1-6
12 34	TCREF RGND	−200mV/dB, 0V= 0dBm 0V	XA25P1-35 STAR GND POINT	B *H
13 35	HMTR DB11	TTL (HIGH TRUE) TTL	E *	XA25P1-36 *E.
14 36	LHET LUNLVL	TTL (LOW TRUE) TTL (LOW TRUE)	XA27P1-20 C	*NOT USED XA27P1-52
15 37	DB0 DB1	TTL TTL	XA60P1-20 XA60P1-76	*E *E
16 38	DB2 DB3	TTL TTL	XA60P1-21 XA60P1-77	*E *E
17 39	DB4 DB6	TTL TTL	XA60P1-22 XA60P1-78	*E *E
18 40	SRD BIAS CONT DB7	0 TO −5V (LEVELED) TTL	G XA60P1-79	XA24P1-13 *E
19 41	AM IN AM RTN	±1V MAXIMUM 0V	A62J15-SMC CENTER *	A A
20 42	MODHI HINT	CURRENT SOURCE TTL (HIGH TRUE)	D E	A62J13-SMC CENTER XA25P1-42
21 43	MOD RTN HMRKR	0V TTL (HIGH TRUE)	D XA57P1-2, 12	A62J13-SMC SHIELD B
22 44	MODLO WMOD	CURRENT SOURCE TTL (LOW TRUE)	D XA27P1-59	A62J14-SMC CENTER *E

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A62 motherboard wiring List for a complete representation of signal sources and destinations.

A27 Pin I/O (1 of 2)

Pin	Mnemonic	Levels	Source	Destination
1 32	−5.2V −5.2V	−5.2V −5.2V	XA53P1-18, 36 XA53P1-18, 36	*S *S
2 33	+20V +20V	+20V +20V	XA52P1-16, 40 XA52P1-16, 40	*S *S
3 34	+5.2V +5.2V	+5.2V +5.2V	XA52P1-17, 18, 41, 42 XA52P1-17, 18, 41, 42	*S *S
4 35	−10V −10V	−10V −10V	XA53P1-12, 13, 31, 32 XA53P1-12, 13, 31, 32	*S *S
5 36	−15V −15V	−15V −15V	XA56P1-15, 30 XA56P1-15, 30	*S *S
6 37	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*S *S
7 38	GND PLANE GND PLANE	0V 0V	IN GROUND IN GROUND	*S *S
8 39	HADCEN LATTN	TTL (HIGH TRUE) TTL (LOW TRUE)	XA21P1-1 A62J20-14	M 0
9 40	ADR0 ADR1	TTL TTL	XA60P1-17 XA60P1-73	*B *B
10 41	ADR2 ADR3	TTL TTL	XA60P1-18 XA60P1-74	*B *B
11 42	ADR4 SIOA	TTL TTL (LOW TRUE)	XA60P1-19 XA60P1-15	*B *B
12 43	WLEVEL WBAND	TTL (LOW TRUE) TTL (LOW TRUE)	B B	XA24P1-33 XA28P1-29
13 44	SYTM TEMP WYTMSLP	100 mV/°C TTL (LOW TRUE)	A13J1-5 B	XA22P1-7 XA28P1-30
14 45	WYTMCTL RSTAT	TTL (LOW TRUE) TTL (LOW TRUE)	B B	XA28P1-8 *
15 46	W11R2 HLB0	TTL (LOW TRUE) TTL (HIGH TRUE)	B A	XA23P1-15 *
16 47	HLB1 HLB2	TTL (HIGH TRUE) TTL (HIGH TRUE)	A A	* *

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A62 motherboard wiring list for a complete representation of signal sources and destinations.

A27 Control Pin I/O (2 of 2)

Pin	Mnemonic	Levels	Source	Destination
17 48	RFSWP LOMD	10V/SWEEP TTL (LOW TRUE)	XA57P1-42 XA26P1-8	I Q R
18 49	RGND RGND	0V 0V	STAR GND POINT STAR GND POINT	*S *S
19 50	GND PLANE GND PLANE	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*S *S
20 51	LHET −.25V/GHZ	TTL (LOW TRUE) −.25V/GHZ	A XA28P1-40	* *
21 52	LCHNG LUNLVL	TTL (LOW TRUE) TTL (LOW TRUE)	* XA26P1-36	Q Q R
22 53	DB0 DB1	TTL TTL	*XA60P1-20 *XA60P1-76	*L *L
23 54	DB2 DB3	TTL TTL	*XA60P1-21 *XA60P1-77	*L *L
24 55	DB4 DB5	TTL TTL	*XA60P1-22 *XA60P1-78	*L *L
25 56	DB6 DB7	TTL TTL	*XA60P1-23 *XA60P1-79	*L *L
26 57	DB8 DB9	TTL TTL	*XA60P1-24 *XA60P1-80	*L *L
27 58	DB10 DB11	TTL TTL	*XA60P1-25 *XA60P1-81	*L *L
28 59	RGND WMOD	0V TTL (LOW TRUE)	STAR GND POINT B	*S *
29 60	DETVL RGND	−0.2V/dB, 0V=0dB 0V	XA25P1-33 STAR GND POINT	N *S
30 61	LVLREF MODLVL	0.2V/dB, 0V=0dB 0 TO −3V LEVELED	T XA26P1-32	XA25P1-13 N
31 62	BVSWP LVLCOR	10V SWEEP 1.25 dB/V, 0V=0dB	XA58P1-40 G	N XA25P1-14

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A62 motherboard wiring list for a complete representation of signal sources and destinations.

A28 P1 Pin I/O

Pin	Mnemonic	Levels	Source	Destination
1 23	+20V +20V	+20V +20V	XA52P1-16, 40 XA52P1-16, 40	*L *L
2 24	+5.2V +5.2V	+5.2V +5.2V	XA52P1-17, 18, 41, 42 XA52P1-17, 18, 41, 42	*L *L
3 25	−10V −10V	−10V −10V	XA53P1-12, 13, 31, 32 XA53P1-12, 13, 31, 32	*L *L
4 26	−15V HSP	−15V TTL (HIGH TRUE)	XA56P1-15, 30 XA57P1-13	*L *I
5 27	SYTM COIL −/−40V SYTM COIL −/−40V	−40V/−40V −40V/−40V	A62J18-12/XA53P1-11, 30 A62J18-12/XA53P1-11, 30	H H
6 28	GMD GND	0V 0V	A62 STAR GND A62 STAR GND	*L *L
7 29	1.4V/GHz WBAND	1.4V/GHz TTL (LOW TRUE)	C XA27P1-43	XA22P1-30 B
8 30	WYTMCTL WYTMSLP	TTL (LOW TRUE) TTL (LOW TRUE)	XA27P1-14 XA27P1-44	I C
9 31	HLB0	TTL (HIGH TRUE)	XA27P1-46	*I
10 32	RSTAT HLB1	TTL (LOW TRUE) TTL (HIGH TRUE)	XA27P1-45 XA27P1-16	NOT USED *I
11 33	DB0 HLB2	TTL TTL (HIGH TRUE)	*XA60P1-20 XA27P1-47	*NOT USED *I
12 34	DB2 DB1	TTL TTL	*XA60P1-21 *XA60P1-76	*NOT USED *NOT USED
13 35	DB4 DB3	TTL TTL	*XA60P1-22 *XA60P1-77	*B C I *B C I
14 36	DB6 DB5	TTL TTL	*XA60P1-23 *XA60P1-78	*B C *B C I
15 37	DB8 DB7	TTL TTL	*XA60P1-24 *XA60P1-79	*B C *B C
16 DB10 38	TTL DB9	*XA60P1-25 TTL	*B C *XA60P1-80	 *B C
17 39	+1.0V/GHZ +1.0V/GHZ RTN	1.0V/GHZ 0V	F F	A62J31-27 A62J31-13
18 40	HENDKICK −.25V/GHZ	TTL (HIGH TRUE) −.25V/GHZ	I E	XA24P1-31 *B C F H
19 41	SYTMDB YOKICK	−22V TO −39V TTL (HIGH TRUE)	H XA54P1-21	A62J32-2 I
20 42	SYTMDC SYTM COIL +	−.6V TO −6V −40V TO −25V	H H	A62J32-4 *
21 43	RGND RGND	0V 0V	STAR GND POINT STAR GND POINT	*L *L
22 44	PRETUNE SYTMRES	−2.5V/GHZ 0V≅2 GHZ −.9V LOW BAND CW	XA54P1-24 H	*C D E J A62J32-5

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A62 motherboard wiring list for a complete representation of signal sources and destinations.

A29 Pin I/O

Pin	Mnemonic	Levels	Source	Destination
1	−10V	−10V	XA34P2-8, 9	*K
2	−40V	−40V	XA34P2-6, 7	*K
3	GND	0V	INSTRUMENT GROUND	*K
4	GND	0V	INSTRUMENT GROUND	*K
5	+20V	+20V	XA34P2-2, 3	*K
6	GND	0V	INSTRUMENT GROUND	*K
7	HULR	TTL (HIGH TRUE)	J	XA34PX-14
8	GND	0V	INSTRUMENT GROUND	*K
9	−5.2V	−5.2V	XA34P2-12, 13	*K
10	GND	0V	INSTRUMENT GROUND	*K
11	GND	0V	INSTRUMENT GROUND	*K
12	TUNE GROUND	0V	E	XA30P1-12
13	TUNE VOLTAGE		E	XA30P1-14
14	GND	0V	INSTRUMENT GROUND	*K
15	GND	0V	INSTRUMENT GROUND	*K

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A34 Reference Loop - M/N Motherboard Schematic Diagram for a complete representation of signal sources and destinations.

A30 Pin I/O

Pin	Mnemonic	Levels	Source	Destination
1 2	−10V	−10V	XA34P2-8,9	*E
3 4	−40V	+40V	XA34P2-6,7	*A
5 6	+20V GND	+20V 0V	XA34P2-2, 3 INSTRUMENT GROUND	*E *E
7 8	GND GND	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*E *E
9 10	GND GND	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*E *E
11 12	GND TUNE GROUND	0V 0V	INSTRUMENT GROUND XA29P1-12	*E A
13 14	TUNE VOLTAGE		XA29P1-13	A
15	GND	0V	INSTRUMENT GROUND	*E

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A34 Reference Loop - M/N Motherboard Schematic Diagram for a complete representation of signal sources and destinations.

A31 Pin I/O

Pin	Mnemonic	Levels	Source	Destination
1 16	−10V −10V	−10V −10V	XA34P2-8, 9 XA34P2-8, 9	*I *I
2 17	+20V +20V	+20V +20V	XA34P2-2,3 XA34P2-2, 3	*I *I
3 18	−5.2V −5.2V	−5.2V −5.2V	XA34P2-12, 13 XA34P2-13, 13	*I *I
4 19	GND GND	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*I *I
5 20	GND GND	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*I *I
6 21	VCO TUNE (−) VCO TUNE (+)		G G	* *
7 22	GND GND	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*I *I
8 23	N1 N2	TTL TTL	XA34P1-15 XA34P1-14	A A
9 24	N5 N6	TTL TTL	XA34P1-11 XA34P1-10	A A
10 25	N3 N4	TTL TTL	XA34P1-13 XA34P1-12	A A
11 26	GND HULM	0V TTL (HIGH TRUE)	INSTRUMENT GROUND H	*I XA34P1-8
12 27	GND GND	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*I *I
13 28	M1 M2	TTL (HIGH TRUE) TTL (HIGH TRUE)	XA34P1-5 XA34P1-6	A A
14 29	M3 M4	TTL (HIGH TRUE) TTL (HIGH TRUE)	XA34P1-3 XA34P1-4	A A
15 30	M5 LMNE	TTL HIGH TRUE TTL (LOW TRUE)	XA34P1-1 XA34P1-2	A NOT USED

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A34 Reference Loop – M/N Motherboard Schematic Diagram for a complete representation of signal sources and destinations.

A33 Pin I/O

Pin	Mnemonic	Levels	Source	Destination
1	VCO TUNE (+)		XA31P1-21	A
2	GND	0V	INSTRUMENT GROUND	*F
3	VCO TUNE (−)		XA31P1-6	A
4	GND	0V	INSTRUMENT GROUND	*F
5	−10V	−10V	XA34P2-8, 9	*F
6	GND	0V	INSTRUMENT GROUND	*F
7	−5.2V	−5.2V	XA34P2-12, 13	*F
8	GND	0V	INSTRUMENT GROUND	*F
9	GND	0V	INSTRUMENT GROUND	*F
10	GND	0V	INSTRUMENT GROUND	*F
11	GND	0V	XA34P2-6, 7	*F
12	−40V	−40V	INSTRUMENT GROUND	*F
13	GND	0V		*F
14	LMNE	TTL (LOW TRUE)	INSTRUMENT GROUND	D
15	GND	0V		*F

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A34 Reference Loop – M/N Motherboard Schematic Diagram for a complete representation of signal sources and destinations.

A34 P1 Pin I/O

Pin	Mnemonic	Levels	Source	Destination
1	M5	TTL (HIGH TRUE)	XA59P1-31	XA31P1-15
2	LMNE	TTL (LOW TRUE)	XA59P1-86	*
3	M3	TTL (HIGH TRUE)	XA59P1-32	XA31P1-14
4	M4	TTL (HIGH TRUE)	XA59P1-87	XA31P1-29
5	M1	TTL (HIGH TRUE)	XA59P1-33	XA31P1-13
6	M2	TTL (HIGH TRUE)	XA59P1-88	XA31P1-28
7				
8	HULM	TTL (HIGH TRUE)	XA31P1-26	XA31P1-26
9				
10	N6	TTL	XA59P1-101	XA31P1-24
11	N5	TTL	XA59P1-46	XA31P1-9
12	N4	TTL	XA59P1-102	XA31P1-25
13	N3	TTL	XA59P1-47	XA31P1-10
14	N2	TTL	XA59P1-103	XA31P1-23
15	N1	TTL	XA59P1-48	XA31P1-8

A34 P2 Pin I/O

Pin	Mnemonic	Levels	Source	Destination
1				
2	+20V	+20V	XA52P1-16, 40	*
3	+20V	+20V	XA52P1-16, 40	*
4	+5.2V	+5.2V	XA52P1-17, 18, 41, 42	*
5	+5.2V	+5.2V	XA52P1-17, 18, 41, 42	*
6	−40V	−40V	XA53P1-11, 30	*
7	−40V	−40V	XA53P1-11, 30	*
8	−10V	−10V	XA53P1-12, 13, 31, 32	*
9	−10V	−10V	XA53P1-12, 13, 31, 32	*
10	GND	0V	A62 STAR GND	*
11	GND	0V	A62 STAR GND	*
12	−5.2V	−5.2V	XA53P1-18, 36	*
13	−5.2V	−5.2V	XA53P1-18, 36	*
14	HULR	TTL (HIGH TRUE)	XA29P1-7	XA29P1-7
15				

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A34 Reference Loop - M/N Motherboard Schematic Diagram for a complete representation of signal sources and destinations.

A35 Pin I/O

Pin	Mnemonic	Levels	Source	Destination
1 19	+5V UNREG +5V UNREG	+7 TO +9V +7 TO +9V	C C	* *
2 20	+5V UNREG +5V UNREG	+7 TO +9V +7 TO +9V	C C	* *
3 21	+5V UNREG +5V UNREG	+7 TO +9V +7 TO +9V	C C	* *
4 22	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*C *C
5 23				
6 24	−40V UNREG −40V UNREG	−40V −40V	A B A B	* *
7 25	+20V UNREG +20V UNREG	+31.2V +31.2V	D D	* *
8 26	+5V AC1 +5V AC1	7V AC 7V AC	A62 LUG (5) A62 LUG (5)	*C *C
9 27	+5V AC1 +5V AC1	7V AC 7V AC	A62 LUG (5) A62 LUG (5)	*C *C
10 28	+5V AC1 +5V AC1	7V AC 7V AC	A62 LUG (5) A62 LUG (5)	*C *C
11 29				
12 30	+5V AC2 +5V AC2	7V AC 7V AC	A62 LUG (5) A62 LUG (5)	*C *C
13 31	+5V AC2 +5V AC2	7V AC 7V AC	A62 LUG (5) A62 LUG (5)	*C *C
14 32	+5V AC2 +5V AC2	7V AC 7V AC	A62 LUG (5) A62 LUG (5)A	*C *C
15 33	−40V AC1 −40V AC1	−40V AC −40V AC	A62 LUG (4) A62 LUG (4)	*A *A
16 34	−40V AC2 −40V AC2	−40V AC −40V AC	A62 LUG (4) A62 LUG (4)	*A *A
17 35				
18 36	+22V +22V	22V 22V	D E D E	* *

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A62 motherboard wiring list for a complete representation of signal sources and destinations.

Pin	Mnemonic	Levels	Source	Destination
1 16	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*G *G
2 17	DB8 DB9	TTL TTL	* *	*THRU A62R7 TO B *THRU A62R8 TO B
3 18	DB10 DB11	TTL TTL	* *	*THRU A62R9 TO B *THRU A62R10 TO B
4 19	LCK4 GND	TTL (LOW TRUE) 0V	XA59P1-52 A62 STAR GND	*THRU A62R11 TO B *G
5 20	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*G *G
6 21	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*G *G
7 22	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*G *G
8 23	GND SW1	0V TTL	A62 STAR GND XA42P1-32	*G *E
9 24	PH1	0 TO +5V	A6R12	A
10 25	GND PH2	0V 0 TO +5V	A62 STAR GND A62R13	*G A
11 26	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*G *G
12 27	−10V −10V	−10V −10V	XA53P1-12,13,31,32 XA53P1-12. 13. 31. 32	*THRU A62L8 TO G *THRU A62L8 TO G
13 28	+12V U1 ADJ +12V U1 ADJ	+10.5V +10.5V	XA5P1-10 XA52P1-10	*THRU A62L2 TO G *THRU A62L2 TO G
14 29	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*G *G
15 30	+5.2V +5.2V	+5.2V +5.2V	XA52P1-17, 18,41,42 XA52P1-17, 18, 41, 42	*THRU A62L1 TO G *THRU A62L1 TO G

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A62 motherboard wiring list for a complete representation of signal sources and destinations.

A37 Pin I/O

Pin	Mnemonic	Levels	Source	Destination
1	DB0	TTL	XA60P1-20	*B
19	DB1	TTL	XA60P1-76	*B
2	DB2	TTL	XA60P1-21	*B
20	DB3	TTL	XA60P1-77	*B
3	DB4	TTL	XA60P1-22	*B
21	DB5	TTL	XA60P1-78	*B
4	DB6	TTL	XA60P1-23	*B
22	DB7	TTL	XA60P1-79	*B
5	DB8	TT;	*	*B
23	DB9	TTL	*	*B
6	GND	0V	A62 STAR GND	*H
24	GND	0V	A62 STAR GND	*H
7	DB10	TTL	*	*B
25	DB11	TTL	*	*B
8	LCK4	TTL (LOW TRUE)	XA59P1-52	*B
26	HULI	TTL (HIGH TRUE)	*G	XA59P1-106
9	GND	0V	A62 STAR GND	*H
27	GND	0V	A62 STAR GND	*H
10	GND	0V	A62 STAR GND	*H
28	GND	0V	A62 STAR GND	*H
11	PH1	0 TO +5V	E	XA36P1-24
29	GND	0V	A62 STAR GND	*H
12	PH2	0 TO +5V	E	XA36P1-25
30	GND	0V	A62 STAR GND	*H
13	GND	0V	A62 STAR GND	*H
31	GND	0V	A62 STAR GND	*H
14	GND	0V	A62 STAR GND	*H
32	GND	0V	A62 STAR GND	*H
15	GND	0V	A62 STAR GND	*H
33	GND	0V	A62 STAR GND	*H
16	GND	0V	A62 STAR GND	*H
34	GND	0V	A62 STAR GND	*H
17	GND	0V	A62 STAR GND	*H
32	GND	0V	A62 STAR GND	*H
18	+5.2V	+5.2V	XA5201-17, 18, 41, 42	*THRU A62L3 TO H
36	+5.2V	+5.2V	XA52P1-17, 18, 41, 42	*THRU A62L3 TO H

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A62 motherboard wiring list for a complete representation of signal sources and destinations.

Pin	Mnemonic	Levels	Source	Destination
1	GND	0V	A62 STAR GND	*F
16	GND	0V	A62 STAR GND	*F
2	GND	0V	A62 STAR GND	*F
17	GND	0V	A62 STAR GND	*F
3	GND	0V	A62 STAR GND	*F
18	GND	0V	A62 STAR GND	*F
4	GND	0V	A62 STAR GND	*F
19	GND	0V	A62 STAR GND	*F
5	GND	0V	A62 STAR GND	*F
20	GND	0V	A62 STAR GND	*F
6	GND	0V	A62 STAR GND	*F
21	GND	0V	A62 STAR GND	*F
7	GND	0V	A62 STAR GND	*F
22	GND	0V	A62 STAR GND	*F
8	GND	0V	A62 STAR GND	*F
23	GND	0V	A62 STAR GND	*F
9	GND	0V	A62 STAR GND	*F
24	GND	0V	A62 STAR GND	*F
10	GND	0V	A62 STAR GND	*F
25	GND	0V	A62 STAR GND	*F
11	GND	0V	A62 STAR GND	*F
26	GND	0V	A62 STAR GND	*F
12	−10V	−10V	XA53P1-12, 13, 31, 32	*THRU A62L8 TO F
27	−10V	−10V	XA53P1-12, 13, 31, 32	*THRU A62L8 TO F
13	+12V U1 ADJ	+10.5V	XA52P1-10	*THRU A62LF TO F
28	+12V UI ADJ	+10.5V	XA52P1-10	*THRU A62LF TO F
14	GND	0V	A62 STAR GND	*F
29	GND	0V	A62 STAR GND	*F
15	GND	0V	A62 STAR GND	*F
30	GND	0V	A62 STAR GND	*F

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A62 motherboard wiring list for a complete representation of signal sources and destinations.

Pin	Mnemonic	Levels	Source	Destination
1 16	HUL1 HUL1	TTL (HIGH TRUE) TTL (HIGH TRUE)	*G *G	XA59P1-106 XA59P1-106
2 17	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
3 18	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
4 19	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
5 20	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
6 21	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
7 22	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
8 23	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
9 24	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
10 25	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
11 26	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
12 27	−10V −10V	−10V −10V	XA53P1-12, 13, 31, 32 XA53P1-12, 13, 31, 32	*THRU A62L4 TO H *THRU A62L4 TO H
13 28	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
14 29	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
15 30	+5.2V +5.2V	+5.2V +5.2V	XA52P1-17, 18, 41, 42 XA52P1-17, 18, 41, 42	*THRU A62L3 TO H *THRU A62L3 TO H

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A62 motherboard wiring list for a complete representation of signal sources and destinations.

Pin	Mnemonic	Levels	Source	Destination
1 16				
2 17	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*G *G
3 3 18	GND	0V	A62 STAR GND A62 STAR GND	*G
4 19	GND	0V	A62 STAR GND A62 STAR GND	*G
5 20	GND	0V	A62 STAR GND A62 STAR GND	*G
6 21	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*G *G
7 22	SW2	TTL	XA42P1-14	E
8 23				
9 24	SW1	TTL	XA42P1-32	*F
10 25	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*G *G
11 26	−40V/−40V SENSE (−) −40V/−40V SENSE (−)	−40V −40V	XA5301-11,30/XA53P1-23 XA53P1-11, 30/XA53P1-23	*A *A
12 27	−10V −10V	−10V −10V	XA53P1-12, 13, 31, 32 XA53P1-12, 13, 31, 32	*G *G
13 28	+20V +20V	+20V +20V	XA52P1-16, 40 XA52P1-16, 40	*G *G
14 29	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*G *G
15 30	+5.2V +5.2V	+5.2V +5.2V	XA52P1-17,18,41,42 XA52P1-17, 18, 41, 42	*G *G

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A62 motherboard wiring list for a complete representation of signal sources and destinations.

Pin	Mnemonic	Levels	Source	Destination
1 16	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*F *F
2 17	HLE2	TTL (HIGH TRUE)	XA59P1-53	*A B C
3 18	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*F *F
4 19	HUL2 DIV N2	TTL (HIGH TRUE) TTL (LOW TRUE)	E XA42P1-27	XA59P1-107 A
5 20	500 KHZ REF	TTL	XA42P1-9	A
6 21	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*F *F
7 22	−7 REF GND	−7V 0V	XA43P1-9 A62 STAR GND	F *F
8 23	N2 TUNE RTN N2 TUNE	0V 0 TO +7 VOLTS	F D	XA43P1-10 XA43P1-28
9 24				
10 25	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*F *F
11 26	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*F *F
12 27	−10V −10V	−V −10V	XA53P1-12, 13, 31, 32 XA53P1-12, 13, 31, 32	*F *F
13 28	+20V +20V	+20V +20V	XA52P1-16, 40 XA52P1-16, 40	*F *F
14 29	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*F *F
15 30	+5.2V +5.2V	+5.2V +5.2V	XA52P1-17, 18, 41, 42 XA52P1-17, 18, 41, 42	*F *F

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A62 motherboard wiring list for a complete representation of signal sources and destinations.

A42 Pin I/O

Pin	Mnemonic	Levels	Source	Destination
1 19	LCK2 LCK1	TTL (LOW TRUE) TTL (LOW TRUE)	XA59P1-109 XA59P1-54	A A
2 20	HLE2 GND	TTL (HIGH TRUE) 0V	XA59P1-53 A62 STAR GND	*C D *H
3 21	DB1 DB0	TTL TTL	XA60P1-76 XA60P1-20	*A *A
4 22	DB3 DB2	TTL TTL	XA60P1-77 XA60P1-21	*A *A
5 23	DB5 DB4	TTL TTL	XA60P1-78 XA60P1-22	*A *A
6 24	DB7 DB6	TTL TTL	XA60P1-79 XA60P1-23	*A *A
7 25	DB9 DB8	TTL TTL	* *	*A *A
8 26	DB11 DB10	TTL TTL	* *	*A *A
9 27	500 KHZ REF DIV N2	TTL TTL (LOW TRUE)	D B	XA41P1-20 *C
10 28	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
11 29				
12 30				
13 31				
14 32	SW2 SW1	TTL TTL	A A	XA40P1-22 *
15 33	−10V −10V	−10V −10V	XA53P1-12, 13, 31, 32 XA53P1-12, 13, 31, 32	*NOT USED *NOT USED
16 34	+20V +20V	+20V +20V	XA5201-16, 40 XA52P1-16, 40	*NOT USED *NOT USED
17 35	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
18 36	+5.2V +5.2V	+5.2V +5.2V	XA52P1-17, 18, 41, 42 XA5201-17, 18, 41, 42	*H *H

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A62 motherboard wiring list for a complete representation of signal sources and destinations.

A43 Pin I/O

Pin	Mnemonic	Levels	Source	Destination
1 19	20/30 LCK3	0 TO +10V TTL (LOW TRUE)	XA58P1-41 XA59P1-108	E D
2 20	HLE2 RGND	TTL (HIGH TRUE) 0V	XA59P1-53 A62 STAR GND	*NOT USED *H
3 21	DB1 DB0	TTL (LOW TRUE) TTL (LOW TRUE)	XA60P1-76 XA60P1-20	*D *D
4 22	DB3 DB2	TTL (LOW TRUE) TTL (LOW TRUE)	XA60 1-77 XA60P1-21	*D *D
5 23	DB5 DB4	TTL (LOW TRUE) TTL (LOW TRUE)	XA60P1-78 XA60P1-22	*D *D
6 24	DB7 DB6	TTL (LOW TRUE) TTL (LOW TRUE)	XA60P1-79 XA60P1-23	*D *D
7 25	DB9 DB8	TTL (LOW TRUE) TTL (LOW TRUE)	* *	*D *D
8 26	DB11 DB10	TTL (LOW TRUE) TTL (LOW TRUE)	* *	*D *D
9 27	−7V REF GND	−7V 0V	C A62 STAR GND	XA41P1-7 *H
10 28	N2 TUNE RTN N2 TUNE	0V 0 TO +7V	XA41P1-8 XA41P1-23	C B G
11 29	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
12 30	GND	0V	A62 STAR GND	*H
13 31	GND	0V	A62 STAR GND	*H
14 32	GND	0V	A62 STAR GND	*H
15 33	−10V −10V	−10V −10V	XA53P1-12, 13, 31, 32 XA53P1-12, 13, 31, 32	*H *H
16 34	+20V +20V	+20V +20V	XA52P1-16, 40 XA52P1-16, 40	*H *H
17 35	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
18 36	+5.2V +5.2V	+5.2V +5.2V	XA52P1-17, 18, 41, 42 XA52P1-17, 18, 41, 42	*H *H

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A62 motherboard wiring list for a complete representation of signal sources and destinations.

A47W1 Pin I/O

Pin	Mnemonic	A47W1P1	Levels
1	RGND	PIN 1	0V
2	SR FBK	PIN 2	−5V TO −17V
3	SR PWR	PIN 3	−5V TO −17V
4	YOXISTB	PIN B	−30V TO −39V
5	YO COIL +	PIN 5	−40V TO −20V

Note: Refer to A55 YO Driver Schematic Diagram and A62 motherboard wiring list for signal source and destination information.

A47W2 Pin I/O

Pin	Mnemonic	A47W2P1	Levels
1	RGND	PIN 1	0V
2	SYTMDB	PIN 2	−22V TO −39V
3	SYTM COIL +	PIN 3	−40V TO −25V
4	SYTMDC	PIN 4	−.6V TO −6V
5	SYTMRES	PIN 5	−.9V LOW BAND CW

Note: Refer to A28 SYTM Driver Schematic Diagram and A62 motherboard wiring list for signal source and destination information.

A50 Pin I/O

Pin	Mnemonic	A50W1P2	Levels
1 2	−5.2V GND	PIN 1 PIN 2	−5.2V 0V
3 4	HLEY +5.2V	PIN 3 PIN 4	TTL (HIGH TRUE) +5.2V
5 6	HFILYO YO COIL +	PIN 5 PIN 6	TTL (HIGH TRUE) −40V TO −20V
7 8	LOMD YO COIL −/−40V	PIN 7 PIN 8	TTL (LOW TRUE) −40V
9 10	+20V −10V	PIN 9 PIN 10	+20V −10V
11 12	−10V +20V	PIN 11 PIN 12	−10V +20V
13 14	YO COIL −/−40V	PIN 13	−40V
15 16	YO COIL+ HULY	PIN 15 PIN 16	−40V TO −20V TTL (HIGH TRUE)
17 18	+5.2V	PIN 17	+5.2V
19 20	GND −5.2V	PIN 19 PIN 20	0V −5.2V

Note: Refer to A50 YO Loop Interconnect Schematic Diagram and A62 motherboard wiring list for signal source and destination information.

A54 Pin I/O

Pin	Mnemonic	Levels	Source	Destination
1 19	+20V LKICK	+20V TTL	XA52P1-16, 40 G	*H XA55P1-1
2 20	+5.2V +5.2V	+5.2V +5.2V	XA52P1-17, 18, 41, 42 XA52P1-17, 18, 41, 42	*H *H
3 21	−40V/−40V SENSE (−) YOKICK	−40V TTL (HIGH TRUE)	XA53P1-11,30/XA53P1-23 G	*H/H *
4 22	−10V −10V	−10V −10V	XA53P1-12, 13, 31, 32 XA53P1-12, 13, 31, 32	*H *H
5 23	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*H *H
6 24	WYOKW PRETUNE	TTL (LOW TRUE) −2.5V/GHZ, 0V = 2.3 GHZ	XA59P1-99 C	G *
7 25	RGND RGND	0V 0V	STAR GND POINT STAR GND POINT	*H *H
8 26	−15V VSWP	−15V 0 TO 10V SWEEP	XA56P1-15, 30 XA58P1-97	*H *C F
9 27	LVSX VCOMP	TTL (LOW TRUE) −26 MHZ/VOLT	XA58P1-68 F	E XA55P1-9
10 28	DB1 WCDAC	TTL TTL (LOW TRUE)	XA60P1-76 XA59P1-30	*A G F
11 29	DB3 DB2	TTL TTL	XA60P1-77 XA60P1-21	*A G *A G
12 30	DB5 DB4	TTL TTL	XA60P1-78 XA60P1-22	*A G *A G
13 31	DB7 DB6	TTL TTL	XA60P1-79 XA60P1-23	*A G *A G
14 32	DB9 DB8	TTL TTL	* *	*A F *A F G
15 33	DB11 DB10	TTL TTL	* *	*A F *A F
16 34	DB13 DB12	TTL TTL	XA60P1-82 *	*F *A F
17 35	DB15 DB14	TTL TTL	XA60P1-83 XA60P1-27	*F *F
18 36	TYOKP WPDAC	TTL (LOW TRUE) TTL (LOW TRUE)	XA59P1-100 XA59P1-68	*G A

A circled letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A62 motherboard wiring list for a complete listing of signal destinations.

A55 Pin I/O

Pin	Mnemonic	Levels	Source	Destination
1 16	+20V +20V	+20V +20V	XA52P1-16, 40 XA52P1-16, 40	*G *G
2 17	+5.2V +5.2V	+5.2V +5.2V	XA52P1-17, 18, 41, 42 XA52P1-17, 18, 41, 42	*G *G
3 18	−40V/−40V SENSE (−) −40V/−40V SENSE (−)	−40V XA53P1-11, 30/XA53P1-23	XA53P1-11, 30/XA53P1-23 *G/NOT USED	*G/NOT USED
4 19	−10V −10V	−10V −10V	XA53P1-12, 13, 31, 32 XA53P1-12, 13, 31, 32	*G *G
5 20	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*G *G
6 21	GND GND	0V 0V	A62 STAR GND A62 STAR GND	*G *G
7 22	LYSP HSP	TTL (LOW TRUE) TTL (HIGH TRUE)	XA59P1-11 XA57P1-13	C D *C
8 23	PRETUNE PRETUNE	−25V/GHZ, 0V = 2.3 GHZ −25V/GHZ, 0V = 2.3 GHZ	XA54P1-24 XA54P1-24	*A *A
9 24	VCOMP YO TUNE	−26 MHZ/VOLT 0V ± 6V	XA54P1-27 E	F A62J6-SMC CENTER
10 25	RGND RGND	0V 0V	STAR GND POINT STAR GND POINT	*H *H
11 26	RGND RGND	0V 0V	STAR GND POINT STAR GND POINT	*H *H
12 27	SR FBK SR FBK	−5V TO −17V −5V TO −17V	A A	A62J29-2 A62J29-2
13 28	SR PWR SR PWR	−5V TO −17V −5V TO −17V	B B	A62J29-3 A62J29-3
14 29	HCEN YOXISTB	TTL (HIGH TRUE) −30V TO −39V	XA59P1-67 B	XA55P1-14 A62J29 PIN 4
15 30	YO COIL + YO COIL +	−40V TO −20V −40V TO −20V	B B	* *

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A62 motherboard wiring list for a complete representation of signal sources and destinations.

A57 Pin I/O (1 of 3)

Pin	Mnemonic	Levels	Source	Destination
1 56	GND PLANE 0V GND PLANE	INSTRUMENT GROUND 0V	*0 INSTRUMENT GROUND	 *0
2 57	HMRKR LINE TRIG	TTL (HIGH TRUE) LINE FREQ 7 TO 10V	J A62-CR1 CATHODE/A62R1	XA26P1-43 L
3 58	LRETRACE	TTL (LOW TRUE)	J	F A62J31-11, 25
4 59	LALTSEL	TTL (LOW TRUE)	J	A62J31-10, 24
5 60	LALTEN	TTL (LOW TRUE)	J	A62J31-9, 23
6 61	MUTE	TTL (HIGH TRUE)	J	A62J31-8, 22
7 62	8410 TRIG	TTL	J	A62J31-7
8 63				
9 64				
10 65				
11 66				
12 67	HMRKR	TTL (HIGH TRUE)	J	XA26P1-43
13 68	HSP LINE TRIG	TTL (HIGH TRUE) LINE FREQ 7 TO 10V	M A62-CR1 CATHODE/A62R1	*I N L
14 69	LIPS LBX	TTL (LOW TRUE) TTL (LOW TRUE)	XA52P1-36/A62J1-19 *F	*NOT USED M XA59-69
15 70	SIOA GND PLANE	TTL (LOW TRUE) 0V	XA60P1-15 INSTRUMENT GROUND	*K *0
16 71	SIOB GND PLANE	TTL (LOW TRUE) 0V	XA60P1-16 INSTRUMENT GROUND	*NOT USED *0
17 72	ADR0 GND PLANE	TTL 0V	XA60P1-17 INSTRUMENT GROUND	*K *0
18 73	ADR2 ADR1	TTL TTL	XA60P1-18 XA60P1-73	*K *K
19 74	ADR4 ADR3	TTL TTL	XA60P1-19 XA60P1-74	*K *K

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A62 motherboard wiring list for a complete representation of signal sources and destinations.

A57 Pin I/O (2 of 3)

Pin	Mnemonic	Levels	Source	Destination
20 75	DB0 GND PLANE	TTL 0V	*C XA60P1-20 INSTRUMENT GROUND	*A C G J *0
21 76	DB2 DB1	TTL TTL	*C XA60P1-21 *C XA60P1-76	*A C G J *A C G J
22 77	DB4 DB3	TTL TTL	*C XA60P1-22 *C XA60P1-77	*A C G J *A C G J
23 78	DB6 DB5	TTL TTL	*C XA60P1-23 *C XA60P1-78	*A C G J *A C G J
24 79	DB8 DB7	TTL TTL	*C XA60P1-24 *C XA60P1-79	*C G *C G J
25 80	DB10 DB9	TTL TTL	*C I XA60P1-25 *C XA60 1-80	*C L *C G
26 81	DB12 DB11	TTL TTL	*C I XA60P1-26 *C I XA60P1-81	*C L *C L
27 82	DB14 DB13	TTL TTL	*C I XA60P1-27 *C I XA60P1-82	*C L *C L
28 83	DB15	TTL	*C I XA60P1-83	*C L
29 84	GND PLANE GND PLANE	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*0 *0
30 85	GND PLANE GND PLANE	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*0 *0
31 86	GND PLANE GND PLANE	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*0 *0
32 87				
33 88				
34 89	GND PLANE GND PLANE	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*0 *0
35 90	+20V +20V	+20V +20V	XA52P1-16, 40 XA52P1-16, 40	*0 *0
36 91	+5.2V +12V	+5.2V +12V	XA52P1-17, 18, 41, 42 XA52P1-9, 33	*0 *NOT USED
37 92	+5.2V +5.2V	+5.2V +5.2V	XA52P1-17, 18, 41, 42 XA52P1-17, 18, 41, 42	*0 *0

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A62 motherboard wiring list for a complete representation of signal sources and destinations.

A57 Pin I/O (3 of 3)

Pin	Mnemonic	Levels	Source	Destination
38 93	−15V −5.2V	−15V −5.2V	XA56P1-15, 30 XA53P1-18, 36	*O *O
39 94	−10V −10V	−10V −10V	XA53P1-12, 13, 31, 32 XA53P1-12, 13, 31, 32	*NOT USED *NOT USED
40 95	GND PLANE	0V	INSTRUMENT GROUND	*O
41 96	NEG BLANK MKR RMP	0, +5V 0 TO 10V SWEEP	N XA58P1-96	A62J31-1, 15 D G
42 97	RFSWP Z-AXIS BLANK	10V/SWEEP +5V/−5V	H N	XA27P1-17 A62J31-2, 16
43 98	FPNLSWP	10V/SWEEP	H	A62J9-SMC CENTER
44 99	RPNLSWP FPNLSWP RTN	10V/SWEEP 0V	H H	A62J8-SMC CENTER
45 100	RGND RPNLSWP RTN	0V 0V	STAR GND POINT H	*O *
46 101	RGND RGND	0V 0V	STAR GND POINT STAR GND POINT	*O *O
47 102				
48 103				
49 104	HULH	TTL (HIGH TRUE)	A62J19-16	*NOT USED
50 105	HRFON	TTL (HIGH TRUE)	J	*
51 106	EXT TRIG	EXTERNAL SOURCE LEVEL	A62J31-4, 18	L A62J31-4, 18
52 107	LSSP	TTL (LOW TRUE)	M	A62J31-5, 19
53 108	PEN LIFT	CLAMP AT 56V	J	A62J31-6, 20
54 109	LSRQ PEN LIFT RTN	TTL (LOW TRUE) 0V	* J	*NOT USED A62J31-21
55 110	GND PLANE GND PLANE	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*O *O

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A62 motherboard wiring list for a complete representation of signal sources and destinations.

A58 Pin I/O (1 of 3)

Pin	Mnemonic	Levels	Source	Destination
1 56	GND PLANE 0V GND PLANE	INSTRUMENT GROUND 0V	*V INSTRUMENT GROUND	 *V
2 57				
3 58				
4 59				
5 60				
6 61				
7 62				
8 63				
9 64				
10 65				
11 66				
12 67				
13 68	HSP LVSZ	TTL (HIGH TRUE) TTL (LOW TRUE)	XA57P1-13 E	*P XA54P1-9 F
14 69	LIPS LBX	TTL (LOW TRUE) TTL (LOW TRUE)	* *U	*NOT USED XA59P1-69 P
15 70	SIOA GND PLANE	TTL (LOW TRUE) 0V	XA60P1-15 INSTRUMENT GROUND	*NOT USED *V
16 71	SIOB GND PLANE	TTL (LOW TRUE) 0V	XA60P1-16 INSTRUMENT GROUND	*NOT USED *V
17 72	ADR0 HFILY0	TTL TTL (HIGH TRUE)	XA60P1-17 XA59P1-72	*NOT USED *NOT USED
18 73	ADR2 ADR1	TTL TTL	XA60P1-18 XA60P1-73	*NOT USED *NOT USED
19 74	ADR4 ADR3	TTL TTL	XA60P1-19 XA60 1-74	*NOT USED *NOT USED

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A62 motherboard wiring list for a complete representation of signal sources and destinations.

A58 Pin I/O (2 of 3)

Pin	Mnemonic	Levels	Source	Destination
20 75	DB0 GND PLANE	TTL 0V	XA60P1-20 INSTRUMENT GROUND	*A B E *V
21 76	DB2 DB1	TTL TTL	XA60P1-21 XA60 1-76	*A B E *A B E
22 77	DB4 DB3	TTL TTL	XA60P1-22 XA60P1-77	*A B E *A B E
23 78	DB6 DB5	TTL TTL	XA60P1-23 XA60P1-78	*A B E *A B E
24 79	DB8 DB7	TTL TTL	XA60P1-24 XA60P1-79	*A B E *A B E
25 80	DB10 DB9	TTL TTL	XA60P1-25 XA60P1-80	*A E *A B E
26 81	DB12 DB11	TTL TTL	XA60P1-26 XA60P1-81	*A E *A E
27 82	DB14 DB13	TTL TTL	XA60P1-27 XA60P1-82	*A E *A E
28 83	WSPTM DB15	TTL (LOW TRUE) TTL	XA59P1-28 XA60P1-83	A *NOT USED
29 84	WRDAC WSPAT	TTL (LOW TRUE) TTL (LOW TRUE)	XA59P1-29 XA59P1-84	B S E
30 85	TYDKP LRSP	TTL (LOW TRUE) TTL (LOW TRUE)	XA59P1-100 XA59P1-85	*NOT USED P
31 86				
32 87				
33 88				
34 89	GND PLANE GND PLANE	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*V *V
35 90	+20V +20V	+20V +20V	XA52P1-16, 40 XA52P1-16, 40	*V *V
36 91	+5.2V +12V	+5.2V +12V	XA52P1-17, 18, 41, 42 XA52P1-9, 33	*V *NOT USED
37 92	+5.2V +5.2V	+5.2V +5.2V	XA52P1-17, 18, 41, 42 XA52P1-17, 18, 41, 42	*V *V

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A62 motherboard wiring list for a complete representation of signal sources and destinations.

A58 Pin I/O (3 of 3)

Pin	Mnemonic	Levels	Source	Destination
38 93	−15V −5.2V	−15V −5.2V	XA56P1-15,30 XA53P1-18, 36	*V *NOT USED
39 94	−10V −10V	−10V −10V	XA53P1-12, 13, 31, 32 XA53P1-12, 13, 31, 32	*V *V
40 95	BVSWP	10V SWEEP	0	XA27P1-31
41 96	20/30 SWP MKR RMP	0V TO +10V 0 TO 10V SWEEP	M K	XA43P1-1 N XA57P1-96 R L
42 97	RGND VSWP	0V 0 TO 10V SWEEP	STAR GND POINT N	*V *F 0
43 98	RGND RGND	0V 0V	STAR GND POINT STAR GND POINT	*V *V
44 99	GND PLANE GND PLANE	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*V *V
45 100	GND PLANE LCHNG	0V TTL (LOW TRUE)	INSTRUMENT GROUND *	*V *NOT USED
46 101	GND PLANE GND PLANE	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*V *V
47 102	HFILYO	TTL (HIGH TRUE)	XA59P1-72	*NOT USED
48 102				
49 104				
50 105				
51 106				
52 107				
53 108	HXREF	TTL (HIGH TRUE)	A62J31-17	*NOT USED
54 109	LSRQ	TTL (LOW TRUE)	*	*NOT USED
55 110	GND PLANE GND PLANE	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*V *V

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A62 motherboard wiring list for a complete representation of signal sources and destinations.

A59 Pin I/O (1 of 3)

Pin	Mnemonic	Levels	Source	Destination
1 56	GND PLANE GND PLANE	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*J *J
2 57				
3 58				
4 59				
5 60				
6 61				
7 62				
8 63				
9 64				
10 65	HOVC LSTP	+3 VOLTS - OVEN WARM TTL (LOW TRUE)	A62J3-3 I	C XA6101-85 *
11 66	LYSP HSTD	TTL (LOW TRUE) TTL (HIGH TRUE)	G G	XA55P1-7 XA52P1-21
12 67	HCEN	TTL (HIGH TRUE)	G	XA55P1-14
13 68	HSP WPDAC	TTL (HIGH TRUE) TTL (LOW TRUE)	XA57P1-13 A	*B XA54P1-36
14 69	LIPS LBX	TTL (LOW TRUE) TTL (LOW TRUE)	XA52P1-36/A62J7-19 *	*I I
15 70	SIOA	TTL (LOW TRUE)	XA60P1-15	*NOT USED
16 71	SIOB	TTL (LOW TRUE)	XA60P1-16	*A
17 72	ADR0 HFILY0	TTL TTL	XA60P1-17 G	*A *XA58P1-47, 72
18 73	ADR2 ADR1	TTL TTL	XA60P1-18 XA60P1-73	*A *A
19 74	ADR4 ADR3	TTL TTL	XA60P1-19 XA60P1-74	*A *A

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A62 motherboard wiring list for a complete representation of signal sources and destinations.

A59 Pin I/O (2 of 3)

Pin	Mnemonic	Levels	Source	Destination
20 75	DB0 GND PLANE	TTL 0V	*D XA60P1-20 INSTRUMENT GROUND	*D E G *J
21 76	DB2 DB1	TTL TTL	*D XA60P1-21 *D XA60P1-76	*D E G *D E G
22 77	DB4 DB3	TTL TTL	*D F XA60P1-22 *D XA60P1-77	*D E G *D E G
23 78	DB6 DB5	TTL TTL	*D F XA60P1-23 *D F XA60P1-78	*D G *D E G
24 79	DB8 DB7	TTL TTL	*XA60P1-24 *D F XA60P1-79	*B D I *D G
25 80	DB10 DB9	TTL TTL	*XA60P1-25 *XA60P1-80	*B E I *B I
26 81	DB12 DB11	TTL TTL	*XA60P1-26 *XA60P1-81	*B E I *B E I
27 82	DB14 DB13	TTL TTL	*XA60P1-27 *XA60P1-82	*B E I *B E I
28 83	WSPTM DB15	TTL (LOW TRUE) TTL	A *XA60P1-83	XA58P1-28 *B E I
29 84	WRDAC WSPAT	TTL (LOW TRUE) TTL (LOW TRUE)	A A	XA58P1-29 XA58P1-84
30 85	WCDAC LRSP	TTL (LOW TRUE) TTL (LOW TRUE)	A G	XA54P1-28 XA58P1-85
31 86	M5 LMNE	TTL (HIGH TRUE) TTL (LOW TRUE)	E E	XA34P1-1 XA34P1-2
32 87	M3 M4	TTL (HIGH TRUE) TTL (HIGH TRUE)	E E	XAE4P1-3 XA34P1-4
33 88	M1 M2	TTL (HIGH TRUE) TTL (HIGH TRUE)	E E	XA34P1-5 XA34P1-6
34 89	5 MHZ CLK LSRQ	TTL TTL (LOW TRUE)	XA60P1-34 *I	D *
35 90	+20V +20V	+20V +20V	XA52P1-16, 40 XA52P1-16, 40	*NOT USED *NOT USED
36 91	+5.2V +12V	+5.2V +12V	XA52P1-17, 18, 41, 42 XA52P1-9, 33	*J *NOT USED
37 92	+5.2V +5.2V	+5.2V +5.2V	XA52P1-17, 18, 41, 42 XA52P1-17, 18, 41, 42	*J *J

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A62 motherboard wiring list for a complete representation of signal sources and destinations.

A59 Pin I/O (3 of 3)

Pin	Mnemonic	Levels	Source	Destination
38 93	−15V −5.2V	−15V −5.2V	XA56P1-15, 30 XA53P1-18, 36	*NOT USED *NOT USED
39 94	−10V −10V	−10V −10V	XA53P1-12, 13, 31, 32 XA53P1-12, 13, 31, 32	*NOT USED *NOT USED
40 95	GND PLANE HPUP	0V TTL (HIGH TRUE)	INSTRUMENT GROUND XA52P1-46	*J *D I
41 96	GND PLANE GND PLANE	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*J *J
42 97	GND PLANE GND PLANE	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*J *J
43 98	GND PLANE HXREF	0V TTL (HIGH TRUE)	INSTRUMENT GROUND A62J31-17	*J *C
44 99	GND PLANE WYOKW	0V TTL (LOW TRUE)	INSTRUMENT GROUND A	*J XA54P1-6
45 100	LCHNG TYOKP	TTL (LOW TRUE) TTL (LOW TRUE)	* A	C *
46 101	N5 N6	TTL TTL	E E	XA34P1-11 XA34P1-10
47 102	N3 N4	TTL TTL	E E	XA34P1-13 XA34P1-12
48 103	N1 N2	TTL TTL	E E	XA34P1-15 XA34P1-14
49 104	HULR HULM	TTL (HIGH TRUE) TTL (HIGH TRUE)	XA34P2-14 XA34P1-8	B B
50 105	HULY HULH	TTL (HIGH TRUE) TTL (HIGH TRUE)	A62J2-16 A62J19-16	B *B
51 106	HLEY HUL1	TTL (HIGH TRUE) TTL (HIGH TRUE)	B XA37P1-26; XA39P1-1, 16	A62J2-3 B
52 107	LCK4 HUL2	TTL (LOW TRUE) TTL (HIGH TRUE)	A XA41P1-4	* B
53 108	HLE2 LCK3	TTL (HIGH TRUE) TTL (LOW TRUE)	B A	* XA43P1-19
54 109	LCK1 LCK2	TTL (LOW TRUE) TTL (LOW TRUE)	A A	XA42P1-19 XA42P1-1
55 110	GND PLANE GND PLANE	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*J *J

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A62 motherboard wiring list for a complete representation of signal sources and destinations.

A60 Pin I/O (1 of 3)

Pin	Mnemonic	Levels	Source	Destination
1 56	GND PLANE GND PLANE	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*L *L
2 57	REN DIO1	TTL (LOW TRUE) TTL	A62J7-10 D	D A62J7-1
3 58	IFC DIO2	TTL (LOW TRUE) TTL	A62J7-17 D	D A62J7-3
4 59	NDAC DIO3	TTL TTL	D D	A62J7-15 A62J7-5
5 60	NRFD DIO4	TTL TTL	D D	A62J7-13 A62J7-7
6 61	DAV DIO5	TTL TTL	D D	A62J7-11 A62J7-2
7 62	EOI DIO6	TTL TTL	D D	A62J7-9 A62J7-4
8 63	ATN DIO7	TTL TTL	D D	A62J7-21 A62J7-6
9 64	SRQ DIO8	TTL TTL	A62J7-19 D	D A62J7-8
10 65	LSTP	TTL (LOW TRUE)	XA59P1-65	D A62J1-43
11 66				
12 67				
13 68				
14 69	LIPS	TTL (LOW TRUE)	XA52P1-36/A62J1-19	*E
15 70	SIOA GND PLANE	TTL (LOW TRUE) 0V	*G INSTRUMENT GROUND	*J *L
16 71	SIOB GND PLANE	TTL (LOW TRUE) 0V	*G INSTRUMENT GROUND	*J *L
17 72	ADR0 GND PLANE	TTL 0V	*G INSTRUMENT GROUND	*J *L
18 73	ADR2 ADR1	TTL TTL	*G *G	*J *J
19 74	ADR4 ADR3	TTL TTL	*G *G	*J *J

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A62 motherboard wiring list for a complete representation of signal sources and destinations.

A60 Pin I/O (2 of 3)

Pin	Mnemonic	Levels	Source	Destination
20 75	DB0 GND PLANE	TTL 0V	*J K I INSTRUMENT GROUND	*I K *L
21 76	DB2 DB1	TTL TTL	*I K *I K	*I K *I K
22 77	DB4 DB3	TTL TTL	*I K *I K	*I K *I K
23 78	DB6 DB5	TTL TTL	*I K *I K	*I K *I K
24 79	DB8 DB7	TTL TTL	*J K I *I K	*I K *I K
25 80	DB10 DB9	TTL TTL	*J K I *J K L	*I K *I K
26 81	DB12 DB11	TTL TTL	*J K I *J K I	*I K *I K
27 82	DB14 DB13	TTL TTL	*J K L *J K I	*I K *I K
28 83	DB15	TTL	*J K I	*I K
29 84				
39 85				
31 86				
32 87				
33 88				
34 89	5 MHZ CLK LSRQ	TTL TTL (LOW TRUE)	B *	C F XA59P1-34 *I
35 90	+20V +20V	+20V +20V	XA52P1-16, 40 XA52P1-16, 40	*NOT USED *NOT USED
36 91	+5.2V +12V	+5.2V +12V	XA52P1-17, 18, 41, 42 XA52P1-9, 33	*L *L
37 92	+5.2V +5.2V	+5.2V +5.2V	XA52P1-17, 18, 41, 42 XA52P1-17, 18, 41, 42	*L *L

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A62 motherboard wiring list for a complete representation of signal sources and destinations.

A60 Pin I/O (3 of 3)

Pin	Mnemonic	Levels	Source	Destination
38 93	−15V −5.2V	−15V −5.2V	XA56P1-15, 30 XA53P1-18, 36	*NOT USED *L
39 94	−10V −10V	−10V −10V	XA53P1-12, 13, 31, 32 XA53P1-12, 13, 31, 32	*NOT USED *NOT USED
40 95	GND PLANE HPUP	0V TTL (HIGH TRUE)	INSTRUMENT GROUND XA52P1-46	*L *NOT USED
41 96	GND PLANE GND PLANE	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*L *L
42 97	GND PLANE GND PLANE	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*L *L
43 98	GND PLANE GND PLANE	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*L *L
44 99	GND PLANE GND PLANE	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*L *L
45 100	HSTM GND PLANE	TTL (HIGH TRUE) 0V	H INSTRUMENT GROUND	XA61P1-45 *L
46 101	LSOB LWRT	TTL (LOW TRUE) TTL (LOW TRUE)	H H	XA61P1-46 XA61P1-101
47 102	LIDA14 LIDA15	TTL (LOW TRUE) TTL (LOW TRUE)	I I	XA61P1-47 XA61P1-102
48 103	LIDA12 LIDA13	TTL (LOW TRUE) TTL (LOW TRUE)	I I	XA61P1-48 XA61P1-103
49 104	LIDA10 LIDA11	TTL (LOW TRUE) TTL (LOW TRUE)	I I	XA61P1-49 XA61P1-104
50 105	LIDA8 LIDA9	TTL (LOW TRUE) TTL (LOW TRUE)	I I	XA6P1-50 XA61P1-105
51 106	LIDA6 LIDA7	TTL (LOW TRUE) TTL (LOW TRUE)	I I	XA61P1-51 XA61P1-106
52 107	LIDA4 LIDA5	TTL (LOW TRUE) TTL (LOW TRUE)	I I	XA61P1-52 XA61P1-107
53 108	LIDA2 LIDA3	TTL (LOW TRUE) TTL (LOW TRUE)	I I	XA61P1-53 XA6P1-108
54 109	LIDA0 LIDA1	TTL (LOW TRUE) TTL (LOW TRUE)	I I	XA61P1-54 XA61P1-109
55 110	GND PLANE GND PLANE	0V 0V	INSTRUMENT GROUND INSTRUMENT GROUND	*L *L

A single letter in the source or destination column refers to a function block on this assembly schematic.

An asterisk (*) denotes multiple sources or destinations; refer to the A62 motherboard wiring list for a complete representation of signal sources and destinations.

A63 Pin I/O

Pin	Mnemonic	A13A1J1	Levels
1			
2	ATNAT1	PIN 2	OPEN COLLECTOR
3	ATNTH2	PIN 3	OPEN COLLECTOR
4	ATNTH4	PIN 4	OPEN COLLECTOR
5	ATNAT3	PIN 5	OPEN COLLECTOR
6	ATN COIL +	PIN 6	+5V
7			
8			
9	ATNAT2	PIN 9	OPEN COLLECTOR
10	ATNAT4	PIN 10	OPEN COLLECTOR
11	ATNTH3	PIN 11	OPEN COLLECTOR
12			
13	ATNTH1	PIN 13	OPEN COLLECTOR
14	LATTN	PIN 14	TTL (LOW TRUE)

Note: Refer to RF Section Schematic Diagram and A62 motherboard wiring list for signal source and destination information.

Reference Loop – M/N Loop Assembly-Level Service

CONTENTS

CONTENTS (Cont'd)

Reference Loop – M/N Loop Introduction

ASSEMBLIES

Reference Loop

The reference loop produces all of the reference signals that are used in the other phase-locked loops.

The reference loop consists of the following assemblies:

- A29 reference phase detector assembly
- A30 100 MHz VCXO (voltage-controlled crystal oscillator) assembly
- A34 reference loop – M/N loop motherboard
- A51 10 MHz standard

M/N Loop

The M/N loop generates the 177-197 MHz signal that drives the A48 sampler in the YO loop.

The M/N Loop consists of the following assemblies:

- A31 M/N phase detector assembly
- A32 M/N VCO (voltage-controlled oscillator) assembly
- A33 M/N output assembly
- A34 reference loop – M/N loop motherboard

Reference Loop Theory of Operation

The reference loop produces all of the reference signals that are used in instrument phase-locked loops. Each of these signals are referenced to either the internal A51 10 MHz standard or an external 5 or 10 MHz source connected to the EXT REF BNC connector on the rear panel. The frequency stability of the instrument is directly related to the stability of the reference.

The reference loop consists of four assemblies, shown in functional order:

- A30 100 MHz VCXO assembly
- A29 reference phase detector assembly
- A34 reference loop – M/N loop motherboard
- A51 10 MHz standard

A30 100 MHz VOLTAGE CONTROLLED CRYSTAL OSCILLATOR ASSEMBLY

The A30 VCXO assembly is a crystal-stabilized voltage controlled oscillator with a ±1 kHz tuning range. It provides a 100 MHz reference signal for four instrument circuits:

- 20-30 phase lock loops (PLL3)
- 3.7 GHz oscillator (in the RF section)
- M/N phase lock loop (after being multiplied by four)
- A29 reference phase detector for phase-locking to the 10 MHz standard

The A30 VCXO is phase-locked to the A51 frequency standard by the A29 reference phase detector assembly.

A29 REFERENCE PHASE DETECTOR ASSEMBLY

The reference phase detector phase-locks the A30 VCXO to the A51 10 MHz reference standard.

This assembly also divides the output of the A30 VCXO and distributes it to the following circuits:

- M/N phase lock loop
- 20-30 phase lock loops (PLL1, PLL2)
- 10 MHz OUT on the rear panel

The 100 MHz VCXO output is divided by ten, providing a 10 MHz input to the reference phase detector. The 10 MHz (internal or external) frequency standard is the second input to the reference phase detector. The VCXO tuning voltage output is proportional to the error in the 100 MHz VCXO.

This assembly also divides the 100 MHz VCXO output frequency by five and ten, providing 20 MHz and 10 MHz respectively. The 20 MHz signal is output to the M/N phase lock loops. 10 MHz is output to the 20-30 phase lock loops and to the rear panel 10 MHz REFERENCE OUTPUT connector.

A34 REFERENCE LOOP – M/N LOOP MOTHERBOARD

This assembly is attached to a metal casting that forms an enclosed housing for the following reference – M/N loop assemblies:

- A29 reference phase detector assembly
- A30 100 MHz VCXO assembly
- A31 M/N phase detector assembly
- A33 M/N output assembly

Each of these assemblies has a sheet metal plate attached to it, that completes the reference – M/N enclosure. The enclosure provides RFI (radio frequency interference) shielding.

A51 10 MHz FREQUENCY STANDARD

This is a self-contained, oven-stabilized, precision reference oscillator. The output of the A51 frequency standard is sent to the A29 reference phase detector assembly through the rear panel jumper.

M/N Loop
Theory of Operation

The M/N loop generates the 177-197 MHz signal that drives the A48 sampler in the YIG oscillator (YO) phase lock feedback loop. The M/N loop uses the 20 and 400 MHz reference signals from the reference loop.

The A48 sampler down-converts the output of the YIG oscillator so the YO can be phase locked to the output of the 20-30 loop.

The M/N loop consists of four assemblies, shown in functional order below:

- A32 M/N VCO assembly
- A33 M/N output assembly
- A31 M/N phase detector assembly
- A34 reference loop – M/N loop motherboard

The YO loop sampler drive output of the M/N loop (after being divided by 2) can be related to the M and N numbers by the following equation:

$$f_{M/N} = 200 - 10 \times (M/N) \text{ MHz}$$

A harmonic of this signal is used in the A48 YO loop sampler to down-convert the 2.3 to 7.0 GHz YO output to 20 to 30 MHz. For every increment in M number, the YO output decreases by 10 MHz, and for every increment in N number, the YO output increases by 200 MHz. This relationship is given in the following equation where $f_{20,30}$ is the output of the 20 to 30 Loop:

$$f_{YO} = 200 \times N - 10 \times M - f_{20,30} \text{ MHz}$$

A32 M/N VCO ASSEMBLY

The M/N VCO is a cavity resonator that is varactor tuned from 355 to 395 MHz. The VCO output goes to the A33 M/N output assembly

A33 OUTPUT ASSEMBLY

The VCO output is split by the A33 output assembly and sent to two circuits:

- The A48 YIG oscillator sampler assembly. This is the output of the entire M/N loop, and is divided by two before going to the YO sampler.
- The A31 phase detector, where the VCO output is phase-locked to the 400 MHz reference loop output.

The M/N VCO assembly is mounted to the A33 M/N output assembly.

A31 M/N PHASE DETECTOR

The M/N phase detector assembly contains a phase detector, a mixer, and two programmable frequency dividers (refer to Figure B-1). The mixer down converts the 355 to 395 MHz M/N VCO output to 5 to 45 MHz by mixing it with the 400 MHz reference signal from A30 100 MHz VCXO.

This 5 to 45 MHz IF signal is frequency divided by the M divider, which is programmed to divide by an integer ranging from 8 to 27. The output of the M divider is phase/frequency compared with the output of the N divider:

The N divider divides the 20 MHz reference loop signal by an integer ranging from 13 to 36. The N and M divider outputs are phase/frequency compared and the resultant error signal tunes the A32 M/N VCO. This keeps the M/N loop phase-locked to the reference loop.

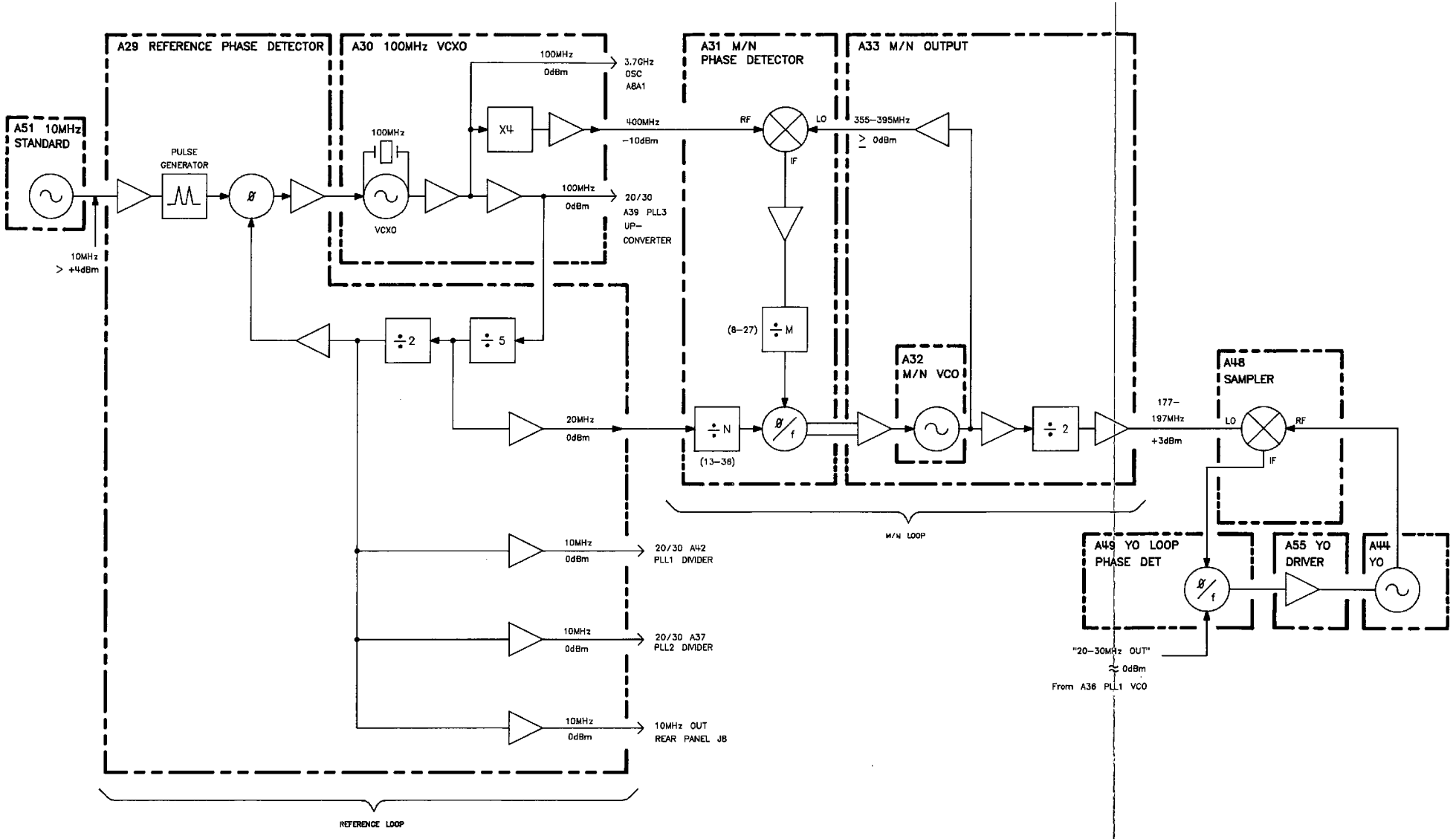


Figure B-1. Reference M/N Simplified Block Diagram

Reference Loop Assembly-Level Troubleshooting

The following troubleshooting procedure provides information for isolating a reference loop failure to the assembly level. The assemblies which are covered in this procedure are:

- A29 reference phase detector
- A30 100 MHz VCXO
- A34 reference loop − M/N loop motherboard
- A59 digital interface assembly.

During troubleshooting, refer to Figure B-21, Reference Loop Troubleshooting Block Diagram. When an output signal level is not mentioned in the troubleshooting procedure, refer to Figure B-21 for the required level. Also provided in this section are the spectrum analyzer plots of the reference loop output signals (Figures B-2 through B-11).

NOTE: In the following procedure, the acronym DUT (device under test) is used to describe the instrument you are troubleshooting.

1. Ensure that the rear panel INT/EXT FREQUENCY STANDARD switch is in the INT position and that a BNC cable is connected between the INT and EXT BNCs (the front panel's EXT REF annunciator should be off).

   If the instrument had been connected to an external frequency standard and the REFERENCE UNLOCK condition now goes away, the problem is with the external frequency standard.

2. Disconnect the BNC cable from the rear panel INT BNC and verify that there is a 10 MHz, $>$ 0 dBm signal present. If this signal is not present or is low in power, go to step 3.

   If the frequency is incorrect, perform the 10 MHz frequency standard adjustment in Section V of the *Calibration Manual* before troubleshooting further.

   If the signal level and frequency are good, reconnect the BNC jumper cable and go to step 5.

3. Remove the YO Loop from the instrument (the YO Loop disassembly procedure is provided in the Sweep Generator − YO Loop functional group). Disconnect A51W1 from the main motherboard connector A62J3 and measure the voltages at A62J3 pins 1 and 5 (refer to Figure B-12). If the proper voltages are not present, troubleshoot the power supplies. If the voltages are present, proceed with step 4.

4. Remove A51 and reconnect A51W1 to A62J3. Measure the frequency and power directly out of A51. If the signal is not present or incorrect, replace A51. If the signal is good, replace J9W1.

5. Disconnect J10W10 from A29J1 and measure the signal directly out of J10W10. The signal should look identical to the one measured in step 2. If the signal is not present, there is a problem with either the rear panel BNC jumper cable or J10W10. If the signal is good, reconnect J10W10 to A29J1 and proceed with step 6.

6. Measure the voltage at TP1, TUNE, on the top cover of the A30 assembly. This test point should be approximately −8V when the reference loop is locked (TP1 is approximately −1V or approximately −25V when the reference loop is unlocked). If the voltage at TP1 is not −8V, proceed with step 7. If the voltage is −8V, proceed with step 13.

7. Adjust A30C4 for −8V at TP1. If TP1 was off by more than ±3 volts and A30C4 is able to bring it back to −8V, it is likely that the 100 MHz VCXO is drifting and A30 should be replaced. If TP1 is still not −8V, proceed with step 8. If TP1 is now −8V, proceed with step 13.

NOTE: When making frequency measurements in steps 8 through 11, connect the FREQ STD OUT from the frequency counter to the DUT's EXT FREQUENCY STANDARD input. If the instruments are not connected in this way, a frequency measurement error may occur. This error is caused by the different 10 MHz references used by the DUT and the frequency counter.

8. Connect the frequency counter to A30J1. Connect a DVM and a low voltage power supply (set to −0.5V) to TP1 (you are applying a voltage between −0.5V to −8V to TP1).

9. Slowly change the power supply voltage until TP1 measures approximately −8V. While you are changing the power supply voltage, you should also see the frequency counter reading approach 100 MHz. If you are unable to change the voltage at TP1, replace the A30 assembly.

10. Slowly adjust the power supply for a 100 MHz frequency counter reading. Slowly increase and decrease the power supply voltage. You should be able to change the frequency counter reading above and below 100 MHz.

    If you can change the frequency counter as described, proceed to step 11.

    If you can't change the frequency counter reading above and below 100 MHz, remove the A30 assembly and measure the power supply voltages at the edge connector. If the power supply voltages are incorrect, troubleshoot the reference loop − M/N loop motherboard and the power supplies. If they are correct, replace the A30 assembly.

11. Turn the DUT to STANDBY and remove the A29 assembly from the instrument. Install an extender board onto the A29 edge connector. Measure the resistance between TP1 (TUNE) and A29P1 pin 13. The resistance should be approximately 370Ω. If the resistance is correct, proceed with step 12. If the resistance is incorrect, remove the A30 assembly and measure the resistance between A29P1 pin 13 to A30P1 pin 14 and from A29P1 pin 12 to A30P1 pin 12. In both cases you should measure approximately 0Ω. If either test fails, check the solder connections and replace the wires connecting the two edge connectors, if necessary. If both measure correctly, replace the A30 assembly.

12. Switch the DUT ON and measure the power supply voltages at the A29 edge connector. If the power supplies are correct, replace the A29 assembly. If the supply voltages are incorrect, troubleshoot the reference − M/N motherboard and the power supplies.

13. Measure the frequency and power output from A30J2, A30J3, and A30W1. If any of these are at the incorrect frequency or power level, proceed to step 14. If the output signals from the above connectors are correct, proceed to step 15.

14. Remove the A30 assembly and install an extender board. Measure the power supply voltages at the A30 edge connector. If the supply voltages are correct, replace the A30 assembly. If the supply voltages are incorrect, troubleshoot the reference − M/N motherboard and the power supplies.

15. Measure the frequency and power output from A29J2, A29J3, A29J4, and A29J5. If any of these are at the incorrect frequency or power level, proceed to step 16. If the output signals from the above connectors are correct, proceed to step 17.

16. Remove the A29 assembly and install an extender board. Measure the power supply voltages at the A29 edge connector. If the supply voltages are correct, replace the A29 assembly. If the supply voltages are incorrect, troubleshoot the reference − M/N motherboard and the power supplies.

17. Press **[SHIFT] [EXT]**. If **REF** is flashing, the DUT is incorrectly indicating a REF unlock, proceed to step 18. If **REF** is not flashing, the reference loop is operating properly.

18. Switch the DUT to STANDBY and install the A29 assembly on an extender board. Remove the A59 digital interface assembly from the DUT and connect the frequency counter's FREQ STD OUT to the DUT's INT FREQUENCY STANDARD input. Switch the DUT ON and measure the voltage at A29P1 pin 7. The voltage should be approximately −0.7V (note: if the voltage is 0V, the feedthrough capacitor on the reference loop − M/N motherboard may be shorted). If the voltage is incorrect, replace A29. If the voltage is correct proceed to step 19.

19. Switch the DUT to STANDBY and reinstall the A59 digital interface assembly. Switch the DUT on and measure the voltage at A29P1 pin 7. If the voltage is no longer approximately −0.7V, remove the A59 digital interface and check the motherboard connector, A62XA59, for bent pins. If none of the pins are bent, replace A59. If the voltage at A31P1 pin 26 is still approximately −0.7V, troubleshoot the A59 assembly for a false unlock indication.

INTERNAL FREQUENCY STANDARD OUTPUT CHECK

Test Setup

ON THE DUT:

Press **[INSTR PRESET].** Connect the rear panel INT FREQUENCY STANDARD BNC directly to the input on the spectrum analyzer. The DUT's **UNLOCK** annunciator will come on, this will not affect the test. Place the FREQUENCY STANDARD switch into the INT position.

ON THE SPECTRUM ANALYZER:

Refer to the figure below for appropriate front panel settings. Set the rear panel FREQ REFERENCE switch to INT.

Proper Waveform Parameters

As shown in the figure below, and within the following parameters:

Frequency = 10 MHz
Power ≥ 0 dBm
Harmonics ≤ −40 dBc

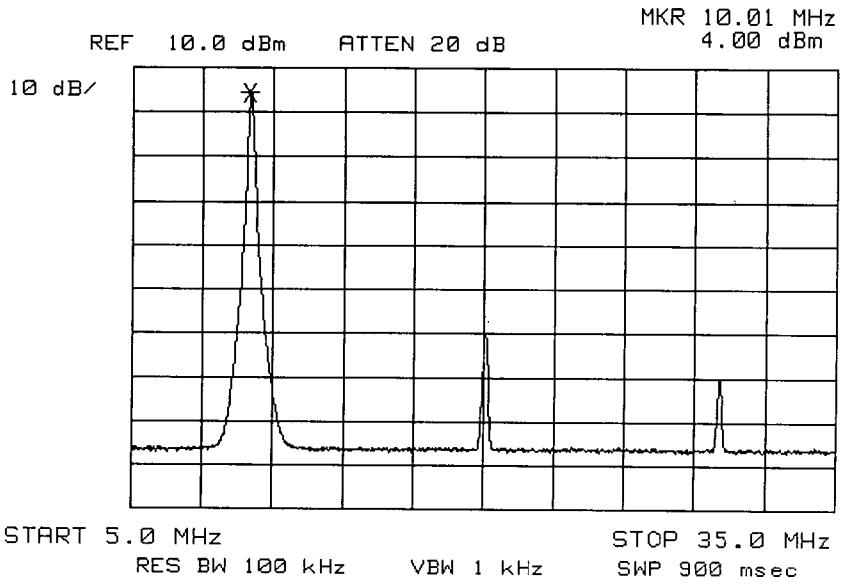


Figure B-2. Internal Frequency Standard Output

10 MHZ REFERENCE OUTPUT CHECK

Test Setup

ON THE DUT:

Press **[INSTR PRESET]**. The DUT requires a jumper cable connected between its INT and EXT FREQUENCY STANDARD BNC's, and the FREQUENCY STANDARD switch must be placed in the INT position.

ON THE SPECTRUM ANALYZER:

Refer to the figure below for appropriate front panel settings. Set the rear panel FREQ REFERENCE switch to INT.

Proper Waveform Parameters

As shown in the figure below, and within the following parameters:

Frequency = 10 MHz
Power = approximately 0 dBm ± 3 dB
Harmonics = ≤ −15 dBc

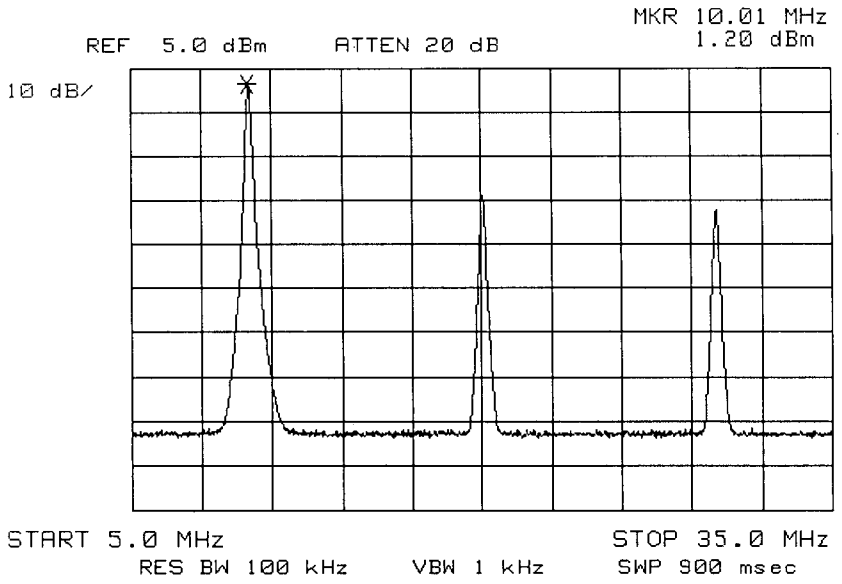


Figure B-3. 10 MHz Reference Output

A30J1 OUTPUT CHECK

Test Setup

ON THE DUT:

Press **[INSTR PRESET]**. The DUT requires a jumper cable connected between its INT and EXT FREQUENCY STANDARD BNC's, and the FREQUENCY STANDARD switch must be placed in the INT position.

ON THE SPECTRUM ANALYZER:

Refer to the figure below for appropriate front panel settings. Connect the DUT's 10 MHz REFERENCE OUTPUT to the spectrum analyzer's FREQ REFERENCE input and set the frequency reference switch to EXT.

OTHER EQUIPMENT:

CAUTION

Do not apply a positive voltage to A30TP1.

Set the HP 6294A power supply to −0.5V and connect a jumper from the positive terminal and ground. Plug in a dual banana to alligator clip test lead. Connect the ground side to instrument ground and the negative side to A30TP1 (TUNE). Also connect the DVM across these two points. Connect the spectrum analyzer's input to A30J1. Slowly adjust the power supply until TP1 reads approximately −8.0 volts.

Proper Waveform Parameters

As shown in figure below, and within the following parameters:

Frequency = approximately 100 MHz
Power = approximately 0 dBm ± 3 dB
Harmonics = ≤ −20 dBc

After verifying this waveform, disconnect the power supply and DVM from A30TP1.

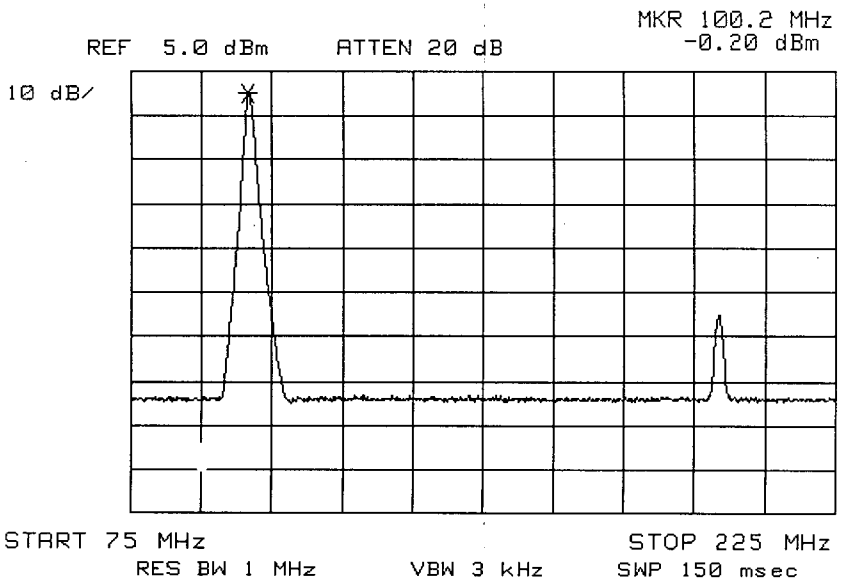


Figure B-4. A30J1 Output With −8.0V Applied to A30TP1 (TUNE)

A30J2 OUTPUT CHECK

Test Setup

Make sure the power supply has been disconnected from A30TP1 (TUNE).

Proper Waveform Parameters

As shown in the figure below, and within the following parameters:

Frequency = 100 MHz
Power = approximately 0 dBm ± 3 dB
Harmonics = ≤ −15 dBc

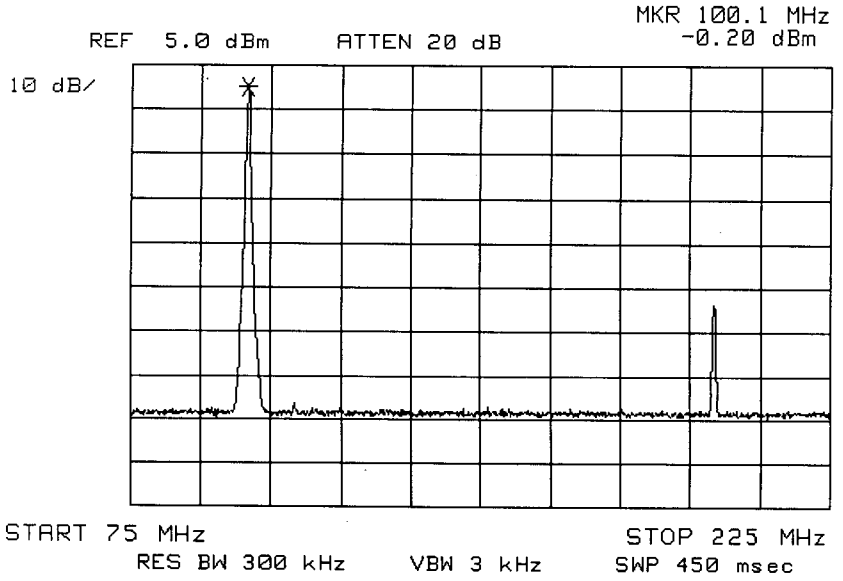


Figure B-5. A30J2 Output

A30J3 OUTPUT CHECK

Proper Waveform Parameters

As shown in the figure below, and within the following parameters:

Frequency = 100 MHz
Power = approximately 0 dBm ± 3 dB
Harmonics = ≤ −15 dBc

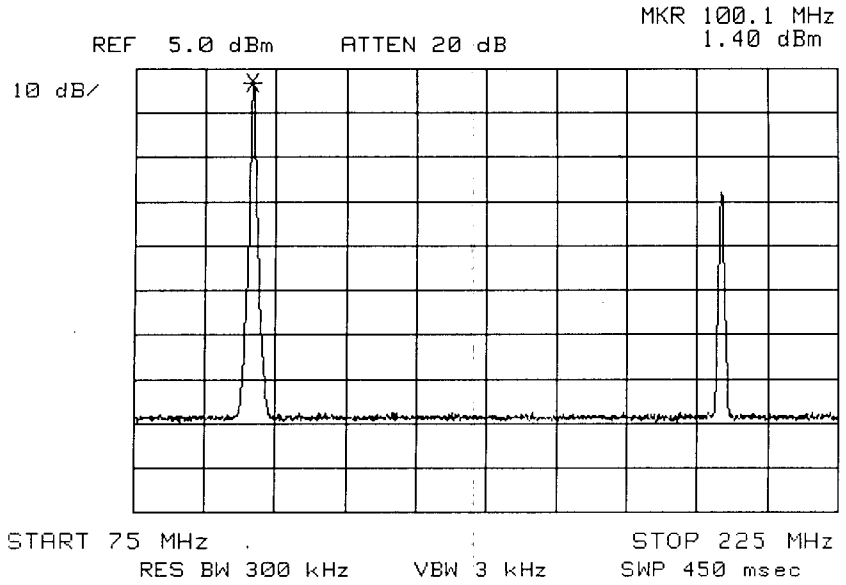


Figure B-6. A30J3 Output

A30W1 OUTPUT CHECK

Proper Waveform Parameters

As shown in the figure below, and within the following parameters:

Frequency = approximately 400 MHz
Power = approximately −10 dBm ± 3 dB
Harmonics 800 MHz: ≤ −10 dBc
200 MHz: ≤ −20 dBc
Others: ≤ −30 dBc

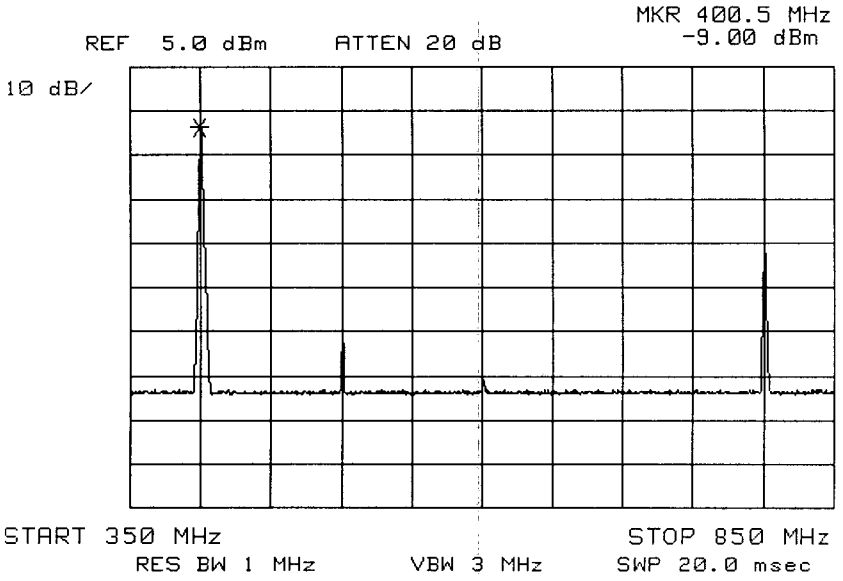


Figure B-7. A30W1 Output

A29J2 OUTPUT CHECK

Proper Waveform Parameters

As shown in the figure below, and within the following parameters:

Frequency = 20 MHz
Power = approximately 0 dBm ± 3 dB
Harmonics = ≤ −10 dBc

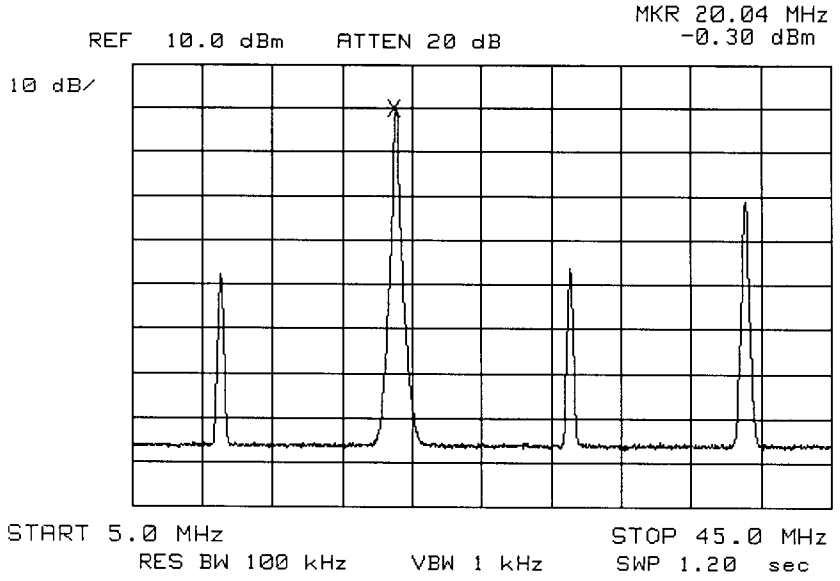


Figure B-8. A29J2 Output

A29J3 OUTPUT CHECK

Proper Waveform Parameters

As shown in the figure below, and within the following parameters:

Frequency = 10 MHz
Power = approximately 0 dBm ± 3 dB
Harmonics = ≤ −15 dBc

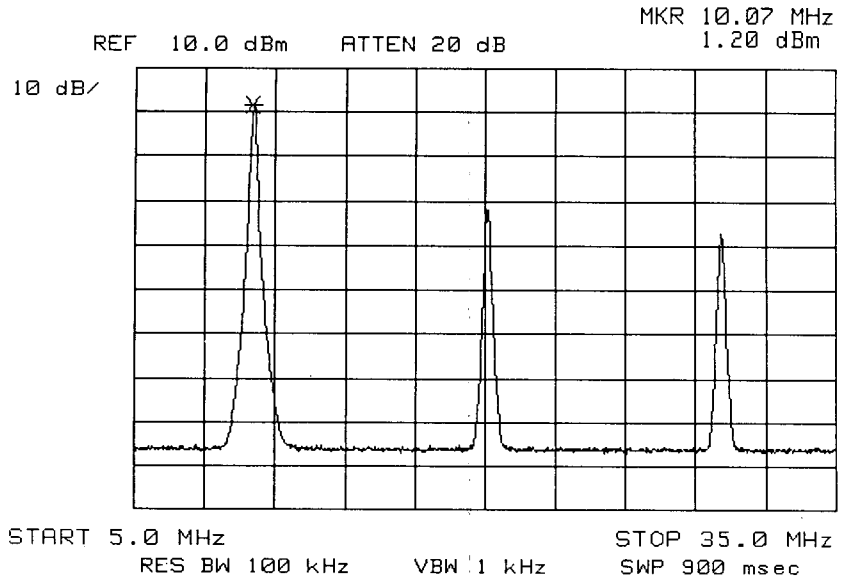


Figure B-9. A29J3 Output

A29J4 OUTPUT CHECK

Proper Waveform Parameters

As shown in the figure below, and within the following parameters:

Frequency = 10 MHz
Power = approximately 0 dBm ± 3 dB
Harmonics = ≤ −15 dBc

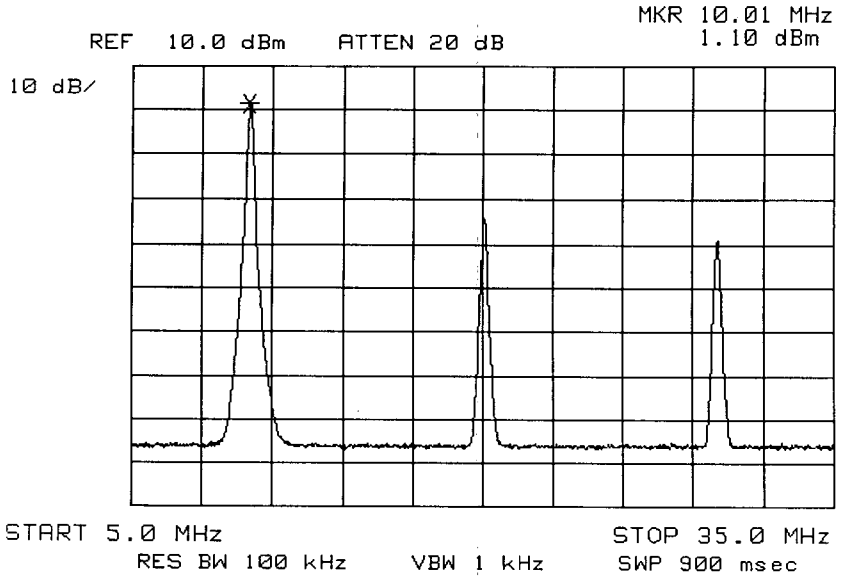


Figure B-10. A29J4 Output

A29J5 OUTPUT CHECK

Proper Waveform Parameters

As shown in the figure below, and within the following parameters:

Frequency = 10 MHz
Power = approximately 0 dBm ± 3 dB
Harmonics = ≤ −15 dBc

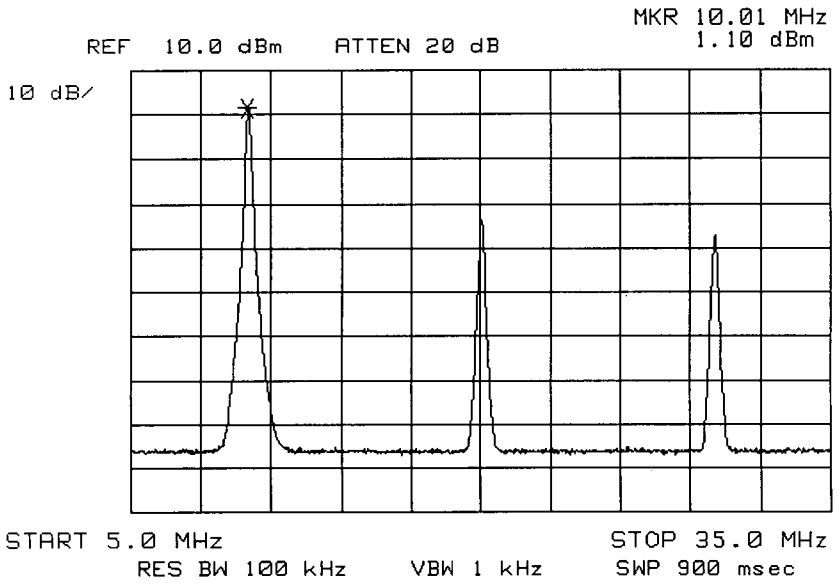
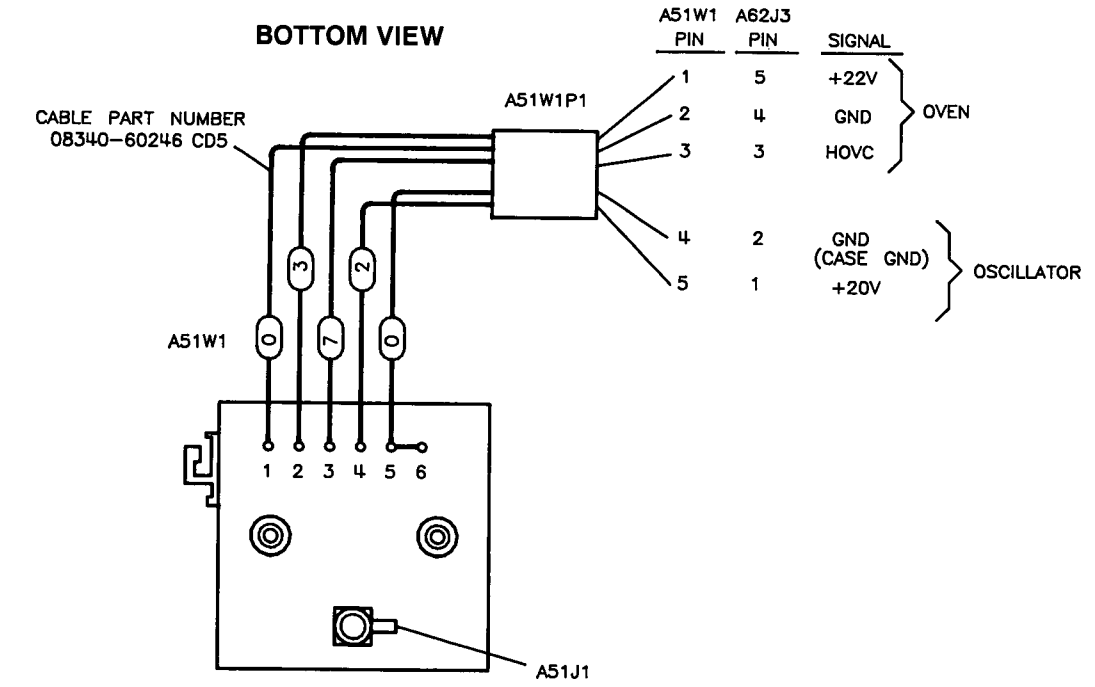
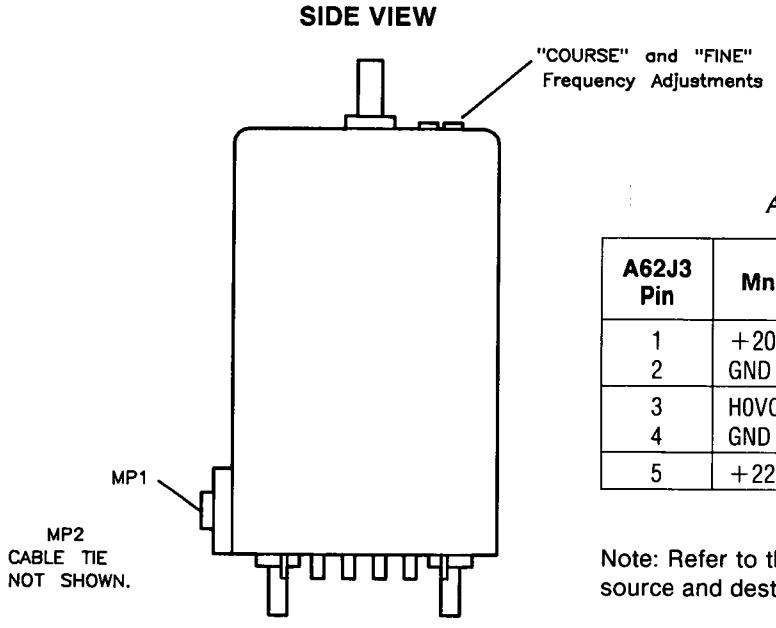


Figure B-11. A29J5 Output

REFERENCE OSCILLATOR
A51 10 MHz

HP Part Number: 08340-60183





A62J3 TO A51W1P1, Pin I/O

A62J3 Pin	Mnemonic	A51W1P1	Levels
1	+20 REF OSC	PIN 5	0V/+20V
2	GND	PIN 4	0V
3	HOVC	PIN 3	+3V/OVEN WARM
4	GND	PIN 2	0V
5	+22V	PIN 1	+22V

Note: Refer to the A62 Motherboard Wiring List for signal source and destination information.

Figure B-12. A51 Reference Oscillator, Wiring Diagram, Part Number

M/N Loop
Assembly-Level Troubleshooting

The following troubleshooting procedure provides information for isolating an M/N loop failure to the assembly level. The assemblies which are covered in this procedure are:

- A31 M/N phase detector assembly
- A32 M/N VCO assembly
- A33 M/N output assembly
- A34 reference loop — M/N loop motherboard
- A59 digital interface assembly

During troubleshooting, refer to Figure B-21, M/N Loop Troubleshooting Block Diagram. When an output signal level is not mentioned in the troubleshooting procedure, refer to Figure B-21 for the required level. Also provided in this section are the spectrum analyzer plots of the M/N Loop output signals (Figures B-13 through B-20).

M/N VERIFICATION AND LOW OUTPUT POWER TROUBLESHOOTING

NOTE: Before replacing A31, A32, or A33, remove the assembly from the instrument and verify that the appropriate power supply voltages are present at the assembly's input. Refer to the end of the Service Introduction in this manual. For the A31 and A33 assemblies, a missing power supply is due to either a failure on the A34 reference loop — M/N loop motherboard or a failure in the power supplies. In the case of A32, a missing power supply can also be due to a failure on the A33 assembly.

This verification is to determine if the M/N Loop outputs the correct M/N OUT signal (frequency and power level) over the entire range of its internal dividers. If you have already determined a CW frequency that generates an incorrect M/N output frequency, you don't need to perform this verification. Proceed to step 1 of the M/N Output Frequency Incorrect troubleshooting, below. If you are not sure which CW frequency causes the incorrect M/N OUT signal, proceed with step 1 of the verification.

NOTE: Pressing **[SHIFT] [M1]** displays, from left to right:

M Divide Number	N Divide Number	M/N OUTput Frequency (MHz)	20/30 OUTput Frequency (MHz)

NOTE: In the following procedure, the acronym DUT (device under test) is used to describe the instrument you are troubleshooting.

1. Connect the frequency counter's FREQ STD OUT to the DUT's rear panel EXT FREQUENCY STANDARD input. Switch the DUT's FREQUENCY STANDARD switch to the EXT position (the EXT REF annunciator should be on).

2. Disconnect the SMB cable from A33J2 and connect the frequency counter's 10 Hz — 500 MHz input to A33J2.

3. Check the M divider frequencies as follows:

   a. On the DUT, press **[INSTR PRESET] [CW] [2] [4] [9] [0] [MHz]**. Select a step size of 10 MHz by pressing **[SHIFT] [CF] [1] [0] [MHz]**. Press **[SHIFT] [M1]** to display, from left to right, the M divide number, the N divide number, the M/N loop output frequency (M/N OUT), and the 20/30 loop output frequency. Press **[CW]** to display the CW frequency in the **ENTRY DISPLAY**.

   b. Press **[▼]** and step the DUT down to 2300.000000 MHz. Check the counter indication at each step. The counter should indicate the M/N loop output frequency ±2 Hz. If, at any point, the frequency counter does not indicate the M/N loop output frequency displayed on the DUT, record the DUT's CW frequency and proceed to step 1 of the M/N Output Frequency Incorrect troubleshooting below.

4. Check the N divider frequencies as follows:

   a. Select a step size of 200 MHz by pressing **[SHIFT] [CF] [2] [0] [0] [MHz]**. Press **[CW]** to display the CW frequency in the ENTRY DISPLAY. The CW frequency should be 2300.000000 MHz.

   b. Press **[▲]** and step the DUT up to 6900.000000 MHz. Check the counter indication at each step. The counter should indicate the M/N loop output frequency ±2 Hz. If, at any point, the frequency counter does not indicate the M/N loop output frequency displayed on the DUT, record the DUT's CW frequency and proceed to step 1 of the M/N Output Frequency Incorrect troubleshooting procedure, below.

5. If steps 3 and 4 both passed, the M/N loop is phase-locked. Press **[SHIFT] [EXT]**. The following phase lock loop diagnostic should be displayed in the ENTRY DISPLAY:

   OSC: REF M/N HET YO N2 N1

   If M/N is flashing, the M/N loop is unlocked. Proceed to step 8. If M/N is not flashing, proceed to step 6.

6. Connect a power meter or spectrum analyzer to A33J2. Repeat steps 3 and 4. The power level indication at each step should be 3 dBm ±3 dB. If the output power is low at any point, perform the M/N Loop adjustment procedure in Section 5, Adjustments, in the *Calibration Manual*. If you are unable to adjust A32C5 (PWR) for 0 dBm ±2 dB out of A32A1W1 (355 − 395 MHz output) replace A32. If the power out of A32A1W1 is good, replace A33.

7. If steps 3 through 6 pass, the M/N loop is operating properly.

8. Switch the DUT to STANDBY. Place the A31 assembly on an extender board and reconnect any A31 SMB cables. Remove the A59 digital interface assembly from the instrument and switch the DUT ON.

9. Measure the voltage at A31P1 pin 26. The voltage at A31P1 pin 26 should be approximately −0.7V (note: if the voltage is 0V, the feedthrough capacitor on the reference loop − M/N motherboard may be shorted). If the voltage is incorrect, replace A31. If the voltage is correct, proceed to step 10.

10. Switch the DUT to STANDBY and reinstall the A59 digital interface assembly. Switch the DUT ON and again measure the voltage at A31P1 pin 26. If the voltage is no longer approximately −0.7V, remove the A59 digital interface and check the motherboard connector, A62XA59, for bent pins. If none of the pins are bent, replace A59. If the voltage at A31P1 pin 26 is still approximately −0.7V, troubleshoot the A59 assembly for a false unlock indication.

M/N OUTPUT FREQUENCY INCORRECT

NOTE: Before replacing A31, A32, or A33, remove the assembly from the instrument and verify that the appropriate power supply voltages are present at the assembly's input. Refer to the end of the Service Introduction in this manual power supply input information. For the A31 and A33 assemblies, a missing power supply will be caused either by a failure on the A34 reference loop – M/N loop motherboard or a failure in the power supplies. In the case of A32, a missing power supply could also be due to a failure on A33.

1. ON the DUT, press **[INSTR PRESET] [CW]**. Either set the DUT to a CW frequency that causes and incorrect M/N Loop output frequency (M/N OUT), or to a CW frequency that causes the front panel UNLK annunciator to light.

2. Press **[SHIFT] [EXT].** The following phase lock loop diagnostic should be displayed in the ENTRY DISPLAY:

   OSC: REF M/N HET YO N2 N1

   If REF is flashing, troubleshoot the reference loop. The reference loop must be phase-locked before the M/N loop can phase-lock.

3. Connect the frequency counter's FREQ STD OUT to the DUT's rear panel EXT FREQUENCY STANDARD input. Switch the DUT's FREQUENCY STANDARD switch to the EXT position (the EXT REF annunciator should be on).

4. Verify that the output frequency from A29J2 is 20 MHz ±2 Hz and that its output power is 0 dBm ±3 dB. If the signal's frequency or power level is incorrect, troubleshoot the reference loop.

5. Verify that the output frequency from A30W1 is 400 MHz ±2 Hz and that its output power is approximately −10 dBm ±3dB. If the signal's frequency or power is incorrect troubleshoot the reference loop.

6. On the DUT, press **[SHIFT] [M1]**. The DUT will display, from left to right, the following information:

M Divide Number	N Divide Number	M/N OUTput Frequency (MHz)	20/30 OUTput Frequency (MHz)

   Verify that the signal out of A33J2 is at the displayed M/N output frequency ±2 Hz and that its power level is 3 dBm ±3 dB. If the output frequency is incorrect, proceed to step 7. If the output frequency is correct but the output power is low, perform the M/N Divider Verification and Low Output Power Troubleshooting above.

7. Remove the SMB cable, A31W2, from A33J1 and install an SMB tee onto A31W2. Connect the second port of the tee to A33J1 (you will need to use an SMB jumper cable) and connect the third port to the frequency counter's 10 Hz – 500 MHz input.

8. Multiply the displayed M/N output frequency by two and verify that the counter indicates this frequency ±2 Hz. If the output frequency is correct, replace A33. If the frequency is incorrect, proceed to step 9.

9. Switch the DUT to STANDBY. Remove the A31 assembly from the instrument and place it on an extender board. Switch the DUT ON. The M and N divide numbers should still be displayed in the POWER dBm display.

10. Measure and record the voltages at:

    A31P1 pin 13 (M1)
    pin 28 (M2)
    pin 14 (M3)
    pin 29 (M4)
    pin 15 (M5)

    Compare the recorded voltages with the voltage levels provided in Table B-1 (use the M divide number shown in the POWER dBm display to determine which voltage levels to use in the table). If the voltages are correct, proceed with step 12. If any of the voltages are incorrect, proceed with step 11.

11. Remove the A31 assembly and repeat step 10. If the voltages are still incorrect, the failure is due to a shorted or open trace on the A34 reference loop – M/N loop Motherboard or an A59 digital interface assembly failure. If the voltages for the M1 through M5 inputs are now correct, replace A31.

12. Measure and record the voltages at:

    A31P1 pin 8 (N1)
    pin 23 (N2)
    pin 10 (N3)
    pin 25 (N4)
    pin 9 (N5)
    pin 24 (N6)

    Compare the recorded voltages with the voltage levels provided in Table B-1 (use the N divide number shown in the POWER dBm display to determine which voltage levels to use in the table). If the voltages are correct, proceed with step 14. If any of the voltages are incorrect, proceed with step 13.

13. Remove the A31 assembly and repeat step 12. If the voltages are still incorrect, the failure is due to a shorted or open trace on the A34 reference loop – M/N loop motherboard or an A59 digital interface assembly failure. If the voltages for the M1 through M5 inputs are now correct, replace A31.

Table B-1. M and N Divide Numbers and Voltage Levels[1]

M Divide Number	M1	M2	M3	M4	M5	N Divide Number	N1	N2	N3	N4	N5	N6
08	0	0	0	1	0	13	1	0	1	1	0	0
09	1	0	0	1	0	14	0	1	1	1	0	0
10	0	1	0	1	0	15	1	1	1	1	0	0
11	1	1	0	1	0	16	0	0	0	0	1	0
12	0	0	1	1	0	17	1	0	0	0	1	0
13	1	0	1	1	0	18	0	1	0	0	1	0
14	0	1	1	1	0	19	1	1	0	0	1	0
15	1	1	1	1	0	20	0	0	1	0	1	0
16	0	0	0	0	1	21	1	0	1	0	1	0
17	1	0	0	0	1	22	0	1	1	0	1	0
18	0	1	0	0	1	23	1	1	1	0	1	0
19	1	1	0	0	1	24	0	0	0	1	1	0
20	0	0	1	0	1	25	1	0	0	1	1	0
21	1	0	1	0	1	26	0	1	0	1	1	0
22	0	1	1	0	1	27	1	1	0	1	1	0
23	1	1	1	0	1	28	0	0	1	1	1	0
24	0	0	0	1	1	29	1	0	1	1	1	0
25	1	0	0	1	1	30	0	1	1	1	1	0
26	0	1	0	1	1	31	1	1	1	1	1	0
27	1	1	0	1	1	32	0	0	0	0	0	1
						33	1	0	0	0	0	1
						34	0	1	0	0	0	1
						35	1	1	0	0	0	1
						36	0	0	1	0	0	1

[1] A 0 entry corresponds to < 0.5V.
A 1 entry corresponds to > 3.0V.

NOTE: To accurately measure the frequency at A31TP1 and A31TP2 in steps 14 and 17, the measurement should be made with a spectrum analyzer and an active probe.

14. Install the A31 assembly on the extender board and press **[CW] [4] [5] [3] [0] [MHz].** Connect Channel 1 of an oscilloscope to A31TP1 and set the scope as follows: 100 ns/div, 200 mV/div, and DC coupled. The waveform displayed on the scope should be similar to the one shown in Figure B-13. The frequency at the test point should be 3.333333 MHz. If the signal at A31TP1 is incorrect, replace A31.

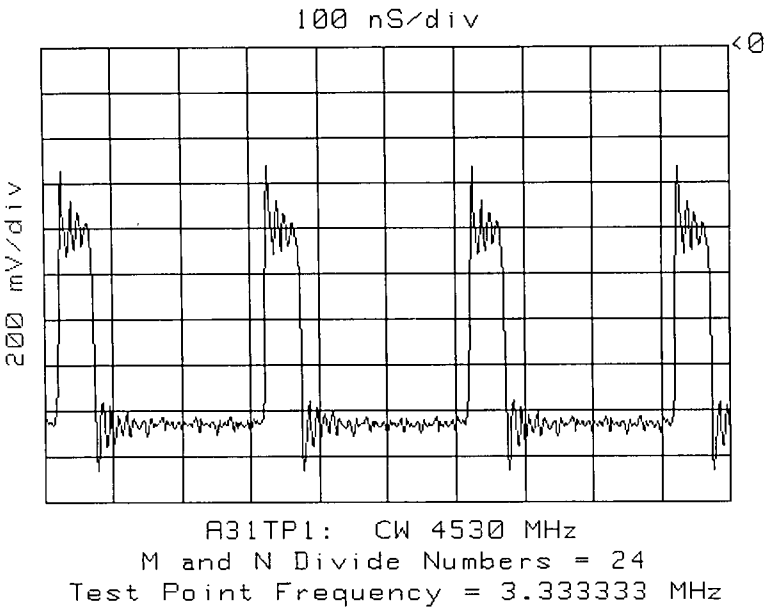


Figure B-13. Signal at A31TP1

15. Measure the frequency at A33J1 (the counter should still be connected in the configuration described in step 7). If the frequency is unstable, proceed to step 18. If the frequency is stable, proceed to step 16.

NOTE: If the frequency out of A33J1 is unstable, it is still possible to check the operation of the M Divider on the A31 assembly. To do this, you will need a synthesized source (LO) which can produce a 376.000000 MHz CW signal (for example, an HP 8340A, 8341A, 8340B or 8341B). Set the LO for 376.000000 MHz, power level 3 dBm, and connect the DUT's 10 MHz REF OUTPUT to the LO's EXTERNAL FREQUENCY STANDARD input. Disconnect A31W2 from A33J1 and connect the source to A31W2. With this input signal, A31TP2 should measure 4 MHz (with an M Divide number of 24) and the its amplitude should be similar to A31TP1.

16. Using the frequency measured in step 15 and the following formula, calculate the frequency which should appear at A31TP2 (Note: the divisor of 6 in the following formula will only work when the M Divide Number is 24):

$$F_{A31TP1} = (400\ MHz - F_{Step\ 15})/6$$

17. Connect Channel 1 of the oscilloscope to A31TP2 and set the oscilloscope's TIME/DIV as appropriate for the frequency you calculated in step 16. Determine if TP2 is at the frequency calculated in step 16 and the amplitude is similar to A31TP1. If the signal at TP2 is bad, replace A31.

CAUTION

In the M/N Loop adjustment procedure, you will be connecting a DC power supply to TP1 (TUNE), located on the cover of the A33 M/N output assembly. It is critical that you do not apply a positive voltage to this test point. Application of a positive voltage may damage the tuning diodes on the A32 VCO. Ensure that you only apply a negative voltage to TP1.

18. Perform the M/N Loop adjustment in Section 5, Adjustments, of the *Calibration Manual*. If, during the procedure, you are unable to adjust the VCO for the correct frequency and power (measured at A32A1W1), replace the A32 assembly. At step 17 of the M/N Loop adjustment procedure, record the frequency at A32A1W2 when the TP1 (TUNE) is set to −2.8V and −35V. After this, reconnect A32A1W1 and measure the frequency and power out of A33J1 and A33J2 when TP1 is set to −2.8V and −35V. A33J1 should be at the same frequency as A32A1W1 and A33J2 should be one half the frequency of A32A1W1. If either output is incorrect, replace A33.

19. If, upon completion of the M/N Loop adjustment procedure, the M/N loop is still not operating properly, switch the DUT to STANDBY and remove the A31 assembly from the instrument (an extender board should still be installed). Connect a jumper cable from A31P1 pin 6 (VCO TUNE −) to pin 5 (GND). Set the power supply to −1V and then connect the DVM to TP1 (TUNE). Connect the positive lead of the power supply to pin 5 (GND) and the negative lead to pin 21 (VCO TUNE +). Switch the DUT on and verify that TP1 is approximately −38V (A33 input loop amplifier railed negative). If this test fails, replace the A33 assembly.

NOTE: "Railed" refers to the condition in which an amplifier is at the positive or negative operational limit determined by its power supplies and biasing circuitry.

20. Switch the DUT to STANDBY and disconnect the power supply. Remove the jumper from A31P1 pin 6 (VCO TUNE −) and reconnect it to pin 21 (VCO TUNE +). Connect the positive lead of the power supply to pin 5 (GND) and the negative lead to pin 6 (VCO TUNE −). Switch the DUT ON and verify that TP1 (TUNE) measures approximately −0.5V (A33 input loop amplifier railed positive). If this test fails, replace A33. If steps 19 and 20 both pass, replace A31.

A33J1 OUTPUT CHECK (WITH PHASE LOCK LOOP CLOSED)

Test Setup

ON THE DUT:

Press **[INSTR PRESET] [CW] [4] [5] [3] [0] [MHz]** (M and N divide numbers = 24). Connect the 10 MHz REF output to the spectrum analyzer's FREQ REFERENCE input. Connect an SMB(f) to SMB(f) cable to A31J1. Split A31J1's output signal with a SMB Tee. Connect A31W2 to one output of the tee and the other output to the spectrum analyzer's input.

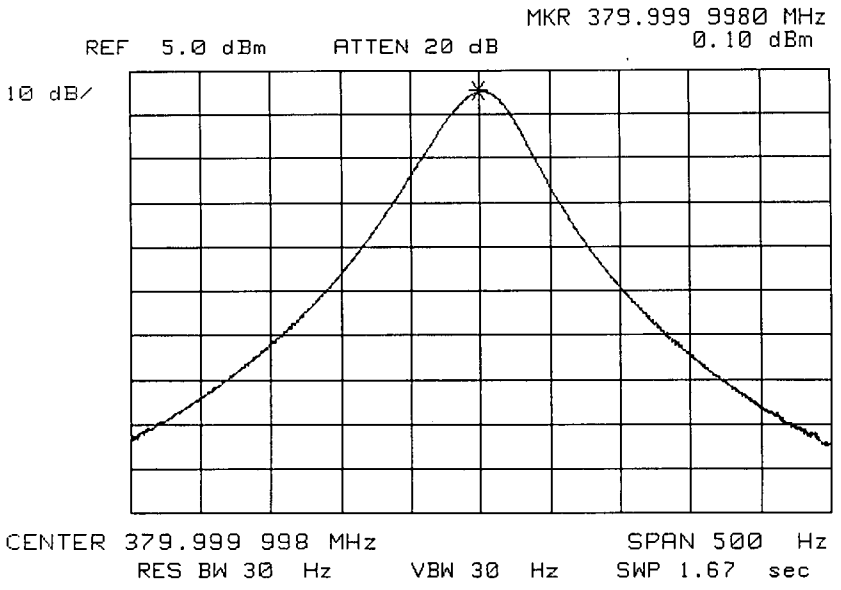
ON THE SPECTRUM ANALYZER

As shown in the figures on the following page.

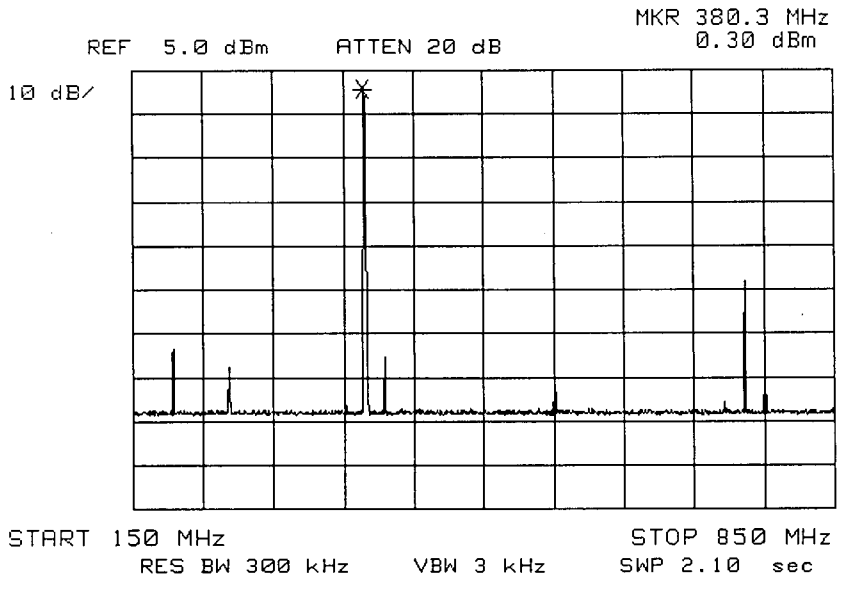
Proper Waveform Parameters

As shown in views A and B, below, and within the following parameters:

Frequency = 380 MHz
Power = ≥ −6 dBm (assumes 6 dB loss due to SMB Tee)
Harmonics = ≤ −20 dBc



VIEW A



VIEW B

Figure B-14. A33J1 Output with Phase Lock Loop Closed

A33J1 OUTPUT CHECK (WITH PHASE LOCK LOOP OPEN)

Test Setup

ON THE DUT:

The DUT should still be set to a CW frequency of 4530 MHz with its 10 MHz REF connected to the spectrum analyzer's FREQ REFERENCE input. Disconnect A31W2, remove the SMB Tee, and connect the output of A33J1 directly to the input of the spectrum analyzer.

ON THE SPECTRUM ANALYZER:

As shown in the figures on the following page:

OTHER EQUIPMENT:

CAUTION

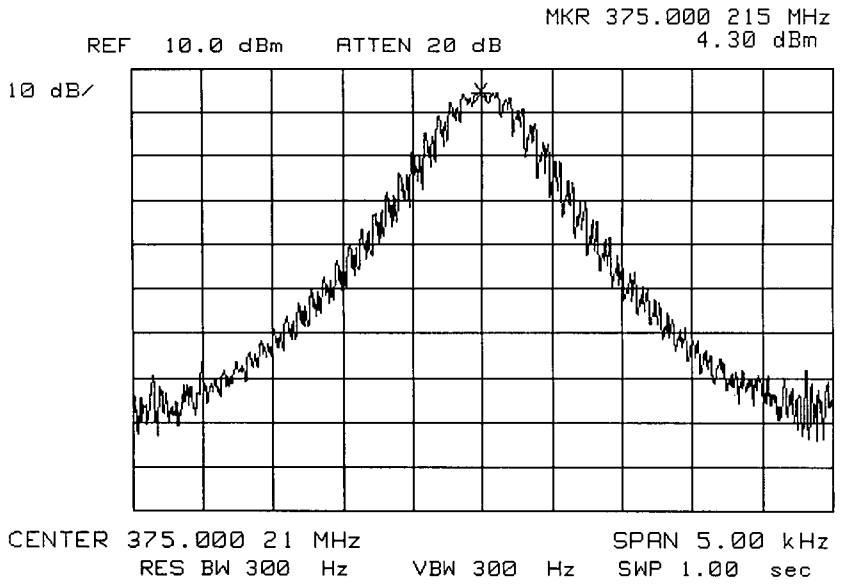
Do not apply a positive voltage to A30TP1.

Set the HP 6294A power supply to about −0.5V. Plug in a dual banana to BNC connector across the ground and negative outputs. To this connect a BNC cable with a BNC to clip lead adapter on the other end. Measure the output of the power supply with a digital voltmeter to determine which output lead is ground and which is negative. Connect the ground side to ground (A31P1-pin 5) and the negative side to A33TP1 (TUNE). Slowly adjust the power supply until the output of the VCO is approximately 375 MHz (TUNE voltage approximately −11V).

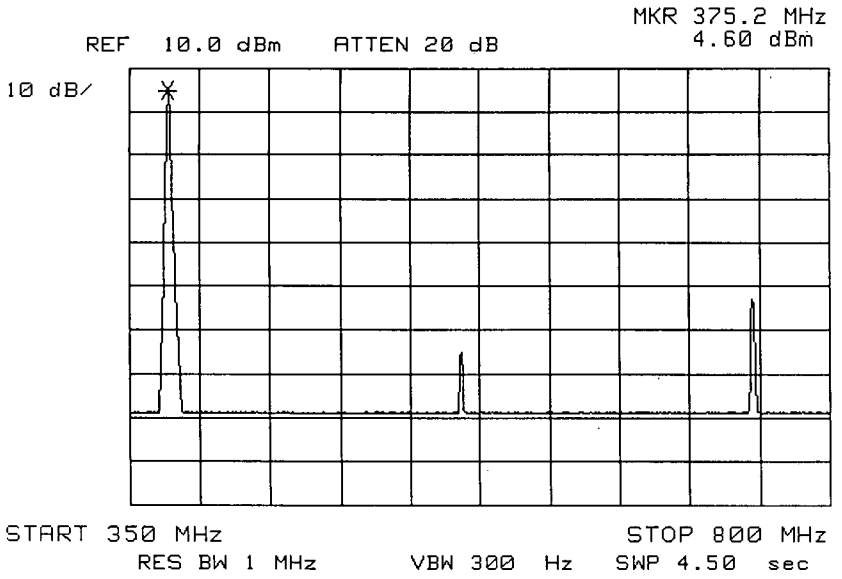
Proper Waveform Parameters

As shown in views A and B, on the following page, and within the following parameters:

Frequency = approximately 375 MHz
Power = approximately 0 dBm ± 3 dBm
Harmonics = ≤ −20 dBc



VIEW A



VIEW B

Figure B-15. A33J1 Output with Phase Lock Loop Open

A33J2 OUTPUT CHECK

Test Setup

ON THE DUT:

The DUT should still be set to a CW frequency of 4530 MHz with its 10 MHz REF connected to the spectrum analyzer's FREQ REFERENCE input. Disconnect the power supply from A33TP1 (TUNE). Connect A33J2 directly to the spectrum analyzer's input.

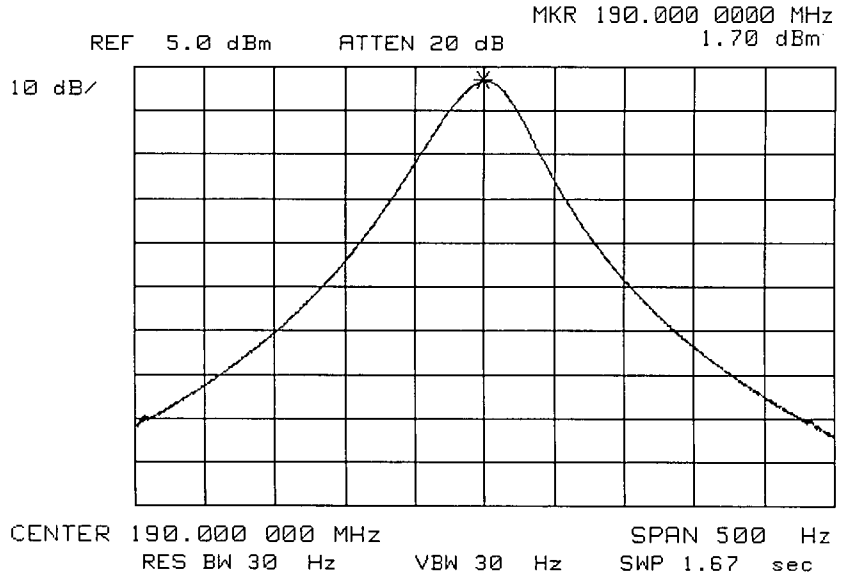
ON THE SPECTRUM ANALYZER:

As shown in figures on the following page.

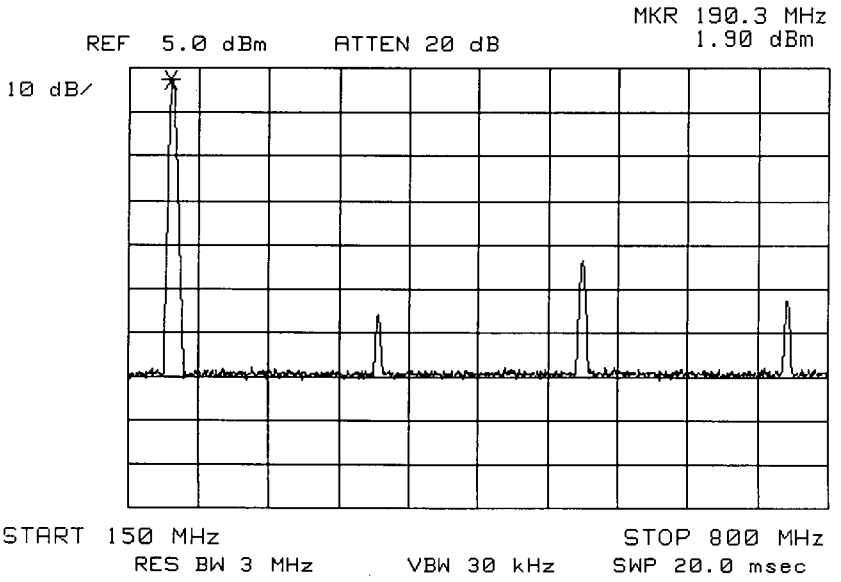
Proper Waveform Parameters

As shown in views A and B on the following page, and within the following parameters:

Frequency = 190 MHz
Power = approximately 0 dBm ± 3 dBm
Harmonics = ≤ −20 dBc



VIEW A



VIEW B

Figure B-16. A33J2 Output

A31TP1 SIGNAL CHECK

Test Setup

ON THE DUT:

The DUT should still be set to a CW frequency of 4530 MHz with its 10 MHz REF connected to the spectrum analyzer's FREQ REFERENCE input. Connect the HP 1121A active probe to A31TP1.

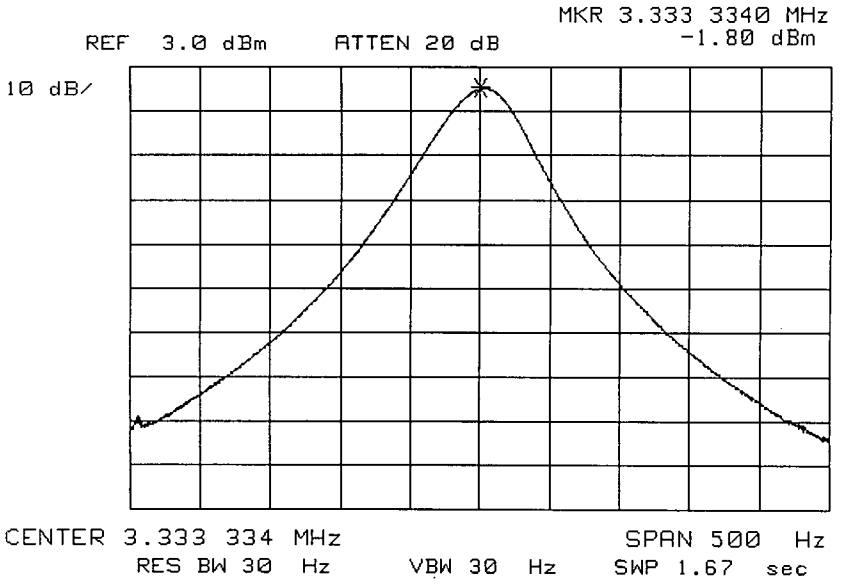
ON THE SPECTRUM ANALYZER:

As shown in the figures on the following page.

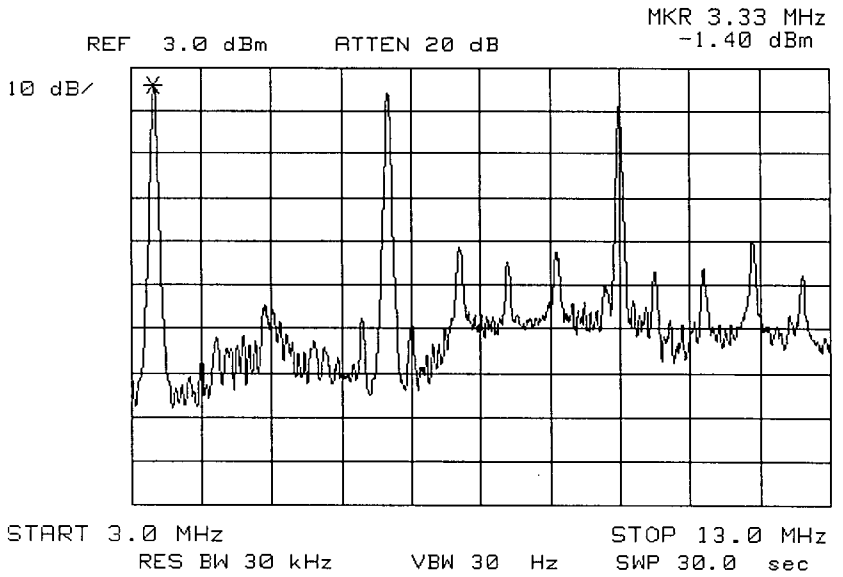
Proper Waveform Parameters

As shown in views A and B on the following page, and within the following parameters:

Frequency = 3.333333 MHz



VIEW A



VIEW B

Figure B-17. A31TP1 Signal Measured with Active Probe

A31TP2 OUTPUT CHECK

Test Setup

ON THE DUT:

The DUT should still be set to a CW frequency of 4530 MHz with its 10 MHz REF connected to the spectrum analyzer's FREQ REFERENCE input. Connect the HP 1121A active probe to A31TP2.

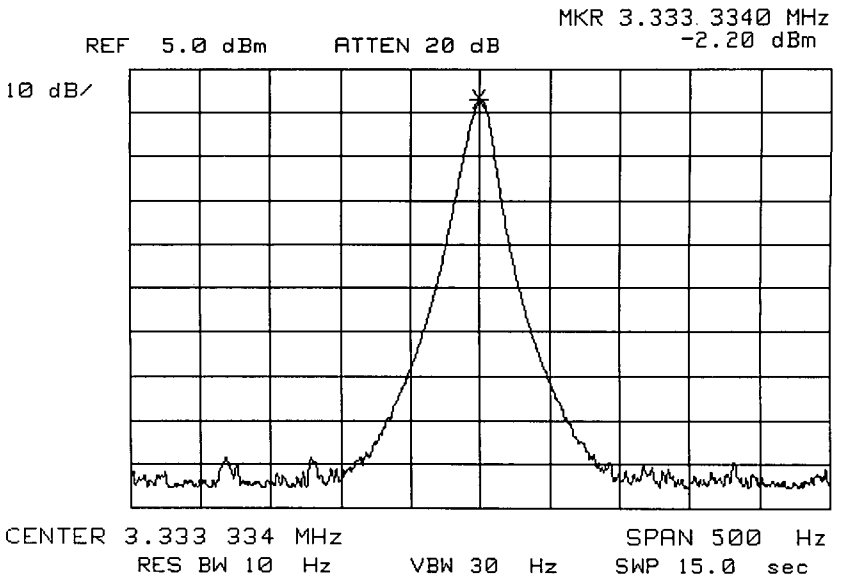
ON THE SPECTRUM ANALYZER:

As shown in figures on the following page.

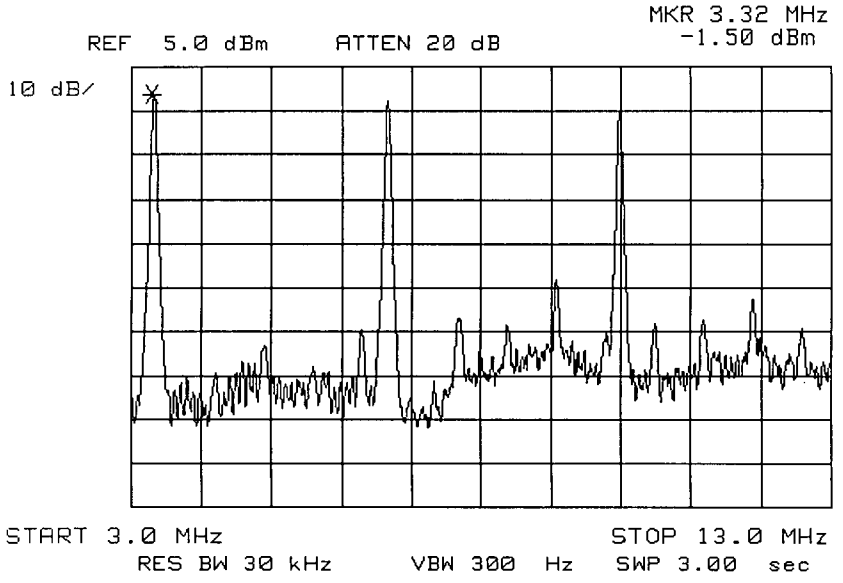
Proper Waveform Parameters

As shown in views A and B on the following page, and within the following parameters:

Frequency = 3.333333 MHz



VIEW A



VIEW B

Figure B-18. A31TP2 Output Using Active Probe

A32A1W1 OUTPUT CHECK

Test Setup

ON THE DUT:

The DUT should still be set to a CW frequency of 4530 MHz with its 10 MHz REF connected to the spectrum analyzer's FREQ REFERENCE input. Disconnect A32A1W1 from A33J3. Connect A32A1W1 to the input of the spectrum analyzer using the SMB to BNC test cable.

ON THE SPECTRUM ANALYZER:

As shown in the figure, below:

OTHER EQUIPMENT:

CAUTION

Do not apply a positive voltage to A30TP1.

Set the HP 6294A power supply to −0.5V and connect a jumper from the positive terminal and ground. Plug in a dual banana to alligator clip test lead Connect the ground side to instrument ground and the negative side to A30TP1 (TUNE). Also connect the DVM across these two points. Slowly adjust the power supply until the output of A32A1W1 is approximately 375 MHz (TUNE voltage approximately −11V).

Proper Waveform Parameters

As shown in the figure below, and within the following parameters:

Frequency = approximately 375 MHz
Power = approximately 0 dBm ± 3 dBm
Harmonics = ≤ −15 dBc

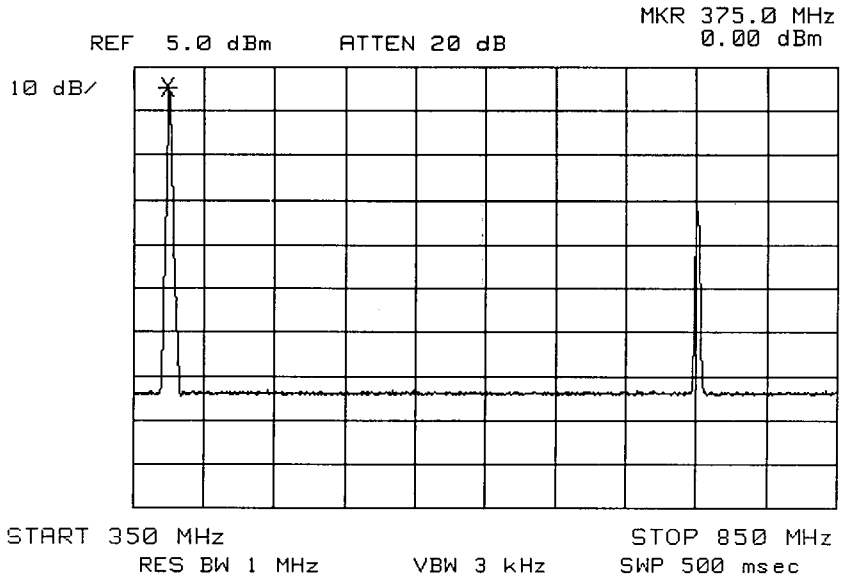


Figure B-19. A32A1W1 Output

A31TP1 and A31TP2 SIGNAL CHECK

Test Setup

ON THE DUT:

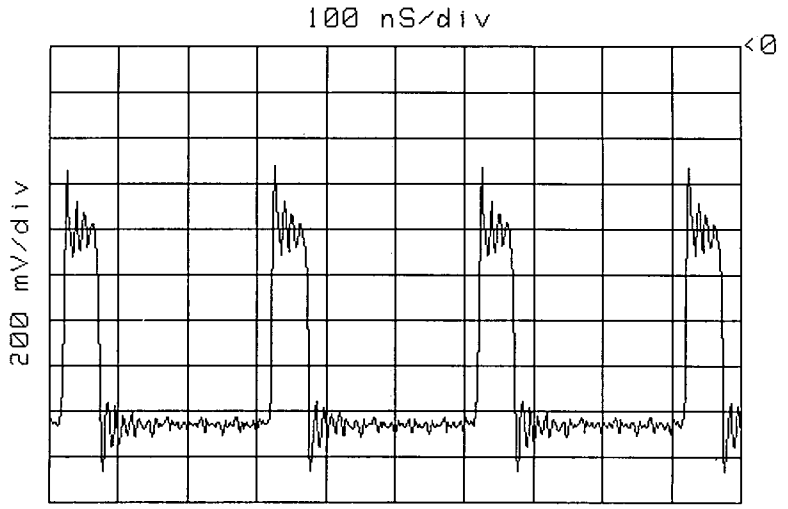
The DUT should still be set to a CW frequency of 4530 MHz. Disconnect the power supply from A32TP1 (TUNE). Turn the instrument OFF and wait approximately one minute. Place A31 on an extender board and turn the instrument back ON. Measure A31TP1 and A31TP2 with the oscilloscope.

ON THE OSCILLOSCOPE:

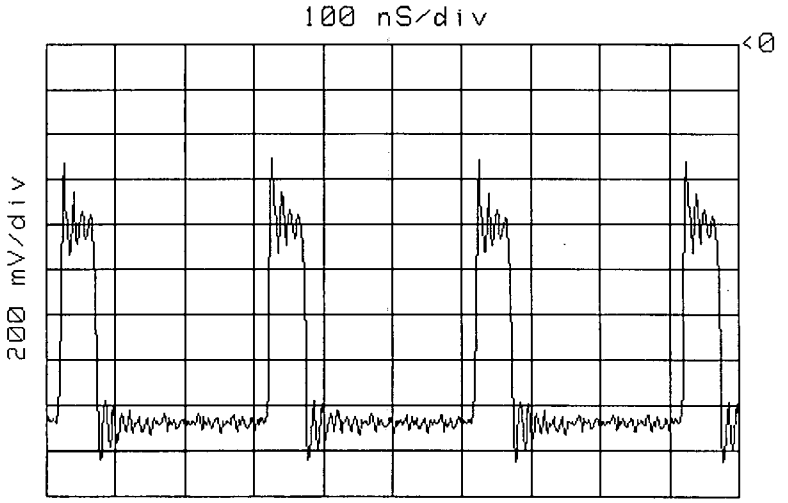
Set up as shown in the figures on the following page.

Proper Waveform Parameters

As shown in views A and B, below.



VIEW A



VIEW B

Figure B-20. A31TP1 and A31TP2 Signals

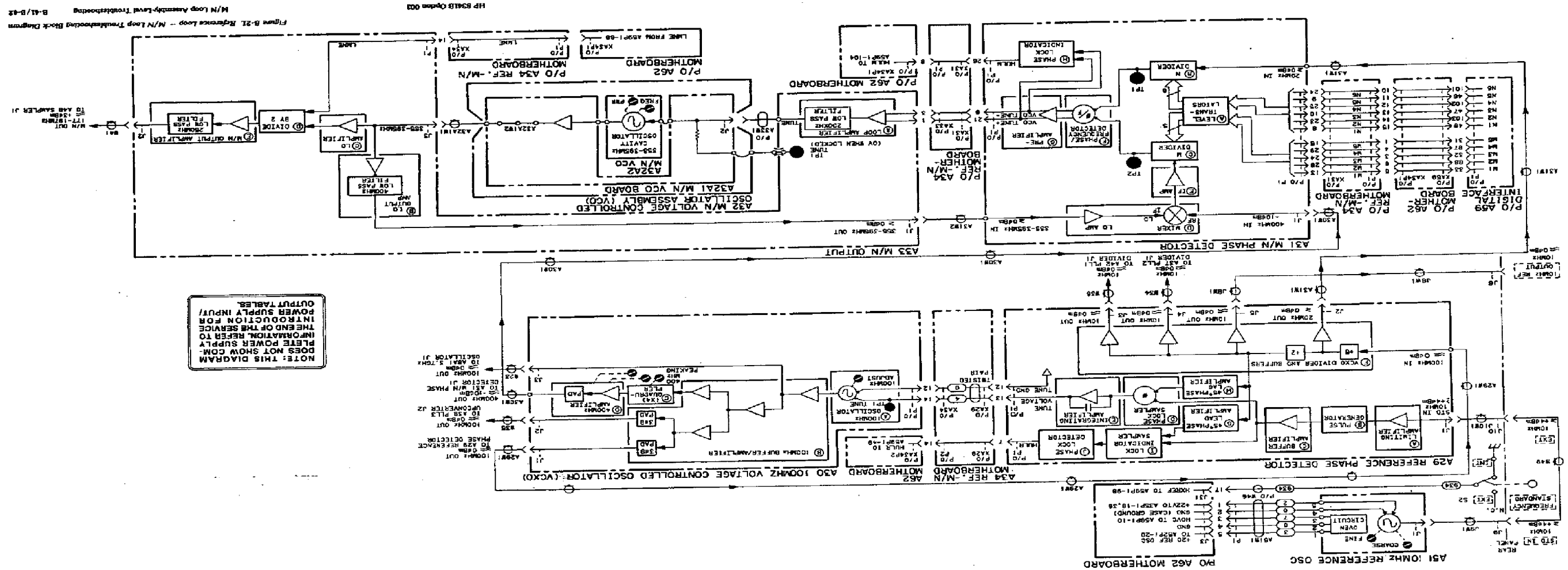


Figure B-21. Reference Loop -- M/N Loop Troubleshooting Block Diagram

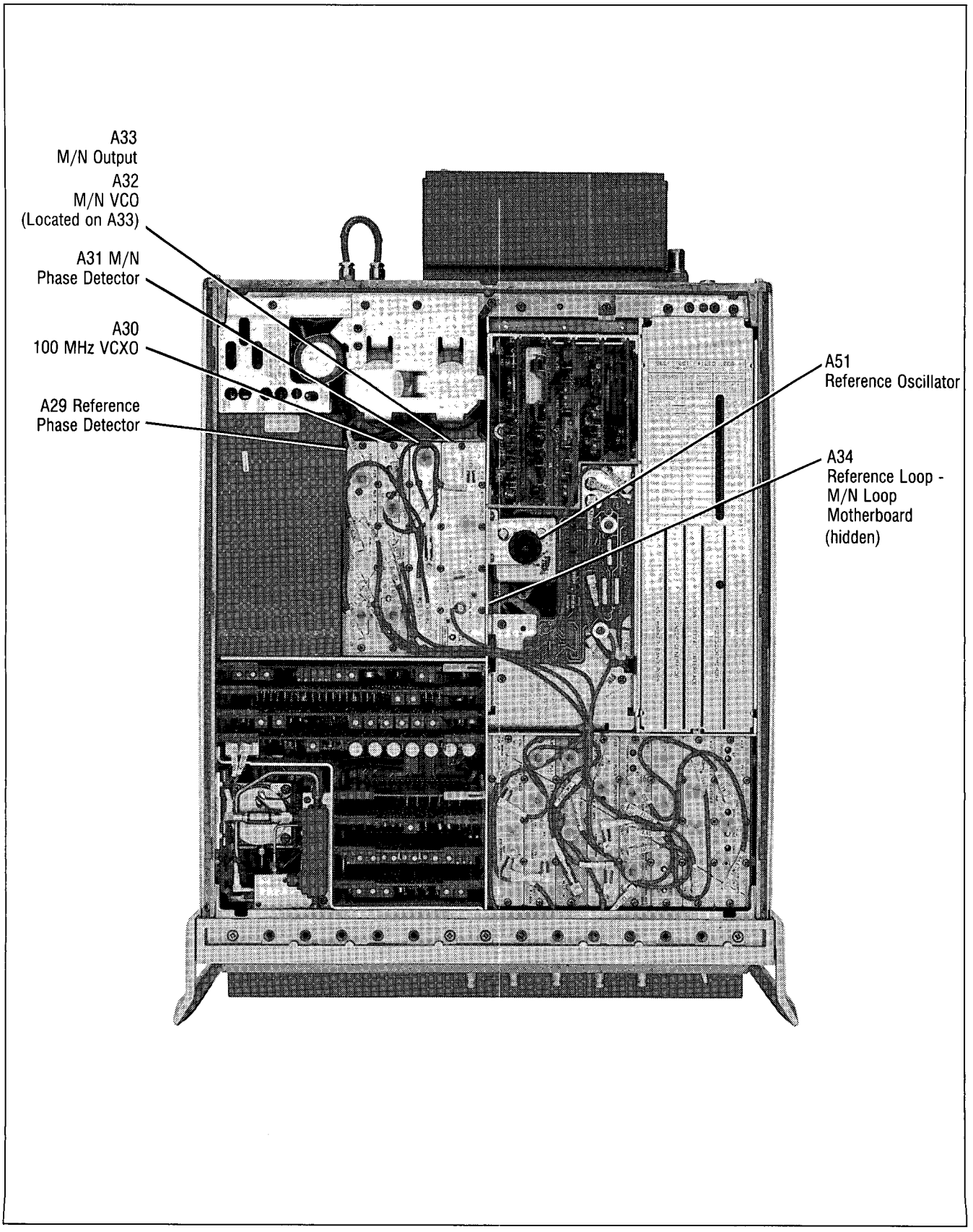


Figure B-22. Reference Loop — M/N Loop Major Assemblies Location Diagram

A34 REFERENCE LOOP – M/N LOOP MOTHERBOARD REPLACEMENT PROCEDURE

To remove the A34 assembly the hinged RF deck and A19 capacitor assemblies must first be removed. Perform the following steps:

Remove the Hinged RF deck as follows:

NOTE: Use of Phillips screwdrivers instead of pozidriv screwdrivers is not recommended.

1. Remove the top, bottom, and perforated side covers. Place the instrument on its left side (as viewed from the front).
2. Refer to the Hinged RF Deck Access Procedure Figure H 24: located in RF Section (Power Level Control), section H, Service, and perform the steps as shown.
3. Refer to Figure B-23, VIEW D. Using a small flat-head screwdriver or connector removal tool, disconnect the ribbon cable from the A13 SYTM.

CAUTION

Do not attempt to remove the ribbon cable with your fingers or you will certainly bend pins on the ribbon connector.

4. Refer to Figure B-23, VIEW C. Remove the following cables from components on the RF deck:

   Ribbon Cable W31 with a small tool, see the above caution.
   W29 (Located under W31 ribbon cable. W29 is marked "A16J4")
   W28 (W28 is marked "A16J3")
   W25 (W25 is marked "LO PLS MOD")
   W23 (W23 is marked "A8-100 IN")
   W24 (W24 is marked "A8-MOD IN")

5. Refer to VIEW C. Using a small posidriv, remove 5 screws, item 14.

   CAREFULLY REMOVE THE RF DECK.

Remove the A19 capacitor Assembly as follows:

6. Refer to VIEW A. Using a large posidriv, remove 2 screws, item 15.
7. Refer to VIEW C. Using a large posidriv, remove 2 screws, item 16.
8. Move the A19 capacitor assembly from side to side while pulling outward. Note that finger contacts on the A19 assembly are inserted into a connector on the main instrument motherboard. The A19 capacitor assembly may now be removed from the instrument.

Reference Loop – M/N Loop Motherboard/Casting Removal

The removal of the RF deck and A19 capacitor assembly exposes 8 screws on the main instrument motherboard that hold the Ref Loop – M/N Loop motherboard/casting in place. These 8 screws can be distinguished from other screws because each is marked with a letter "B" on the main instrument motherboard, right next to the screw. Four of these screws are longer in length than the others.

9. Remove the 8 screws marked with a "B".

10. Refer to Figure B-23, Reference Loop – M/N Loop Assemblies and Mounting Hardware. On the bottom of the instrument, remove all cables going to the A29, A30, A31, and A33 assemblies.

11. Again refer to Figure B-23. With a small pozidriv, remove all 28 screws that hold the A29, A30, A31, and A33 sheet metal covers in place. Note that 3 screws are shown in Figure B-24 which do not need to be removed. Remove the A29, A30, A31, and A33 assemblies.

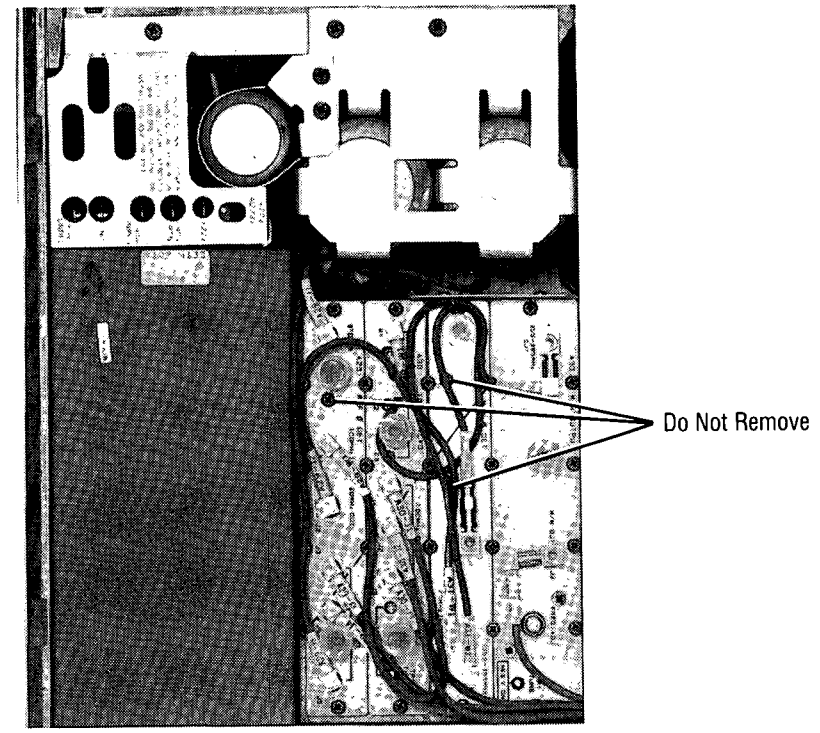


Figure B-23. Reference Loop – M/N Loop Assemblies and Mounting Hardware

12. Pull the reference loop – M/N loop casting out of the instrument.

13. Inspect the bare contacts on the main instrument motherboard before installing the new reference loop – M/N loop motherboard/casting assembly. Make sure they are clean and free of dirt, grit, metal shavings, or any other type of foreign material. Inspect the connectors on the bottom of the new motherboard/casting assembly, make sure they are not damaged or bent. Install the new motherboard/casting assembly so its contacts are oriented the same way as those on the main instrument motherboard.

    On the top of the instrument, replace the 8 screws removed in step 9.

Reinstall the A29, A30, A31, and A33 assemblies, along with the 28 retaining screws. Reconnect all cables. (Refer to Figure B-23 if necessary.)

Reinstall the A19 capacitor Assembly

14. Note that one end of the capacitor assembly has two tabs, or flanges, with one screw hole in each. This end should be lowered into the instrument first, so the other end will not hit the side panel. Press the P.C. board fingers of the A19 assembly into the connector on the main instrument motherboard.

15. Refer to VIEW A and C. With a large pozidriv, install the four screws, items 15 and 16.

Reinstall the RF deck

16. Place the RF deck hinge on the standoffs it attaches to. Make sure ribbon cable W29 (shown in VIEW C) runs under the RF deck, between the two standoffs nearest the center of the instrument. Make sure the ribbon cable is not pinched between the RF deck and the standoffs when screwing the hinge in place (next step).

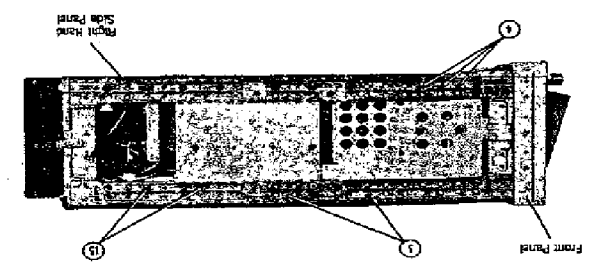
17. Refer to VIEW C. With a small pozidriv, install the 5 RF deck hinge screws, item 14. Plug the W29 ribbon cable into the sockets on the A20 and A16 assemblies.

18. Refer to VIEW D. Reinstall the ribbon cable which was previously removed from the A13 SYTM. Be sure to orient the ribbon connector so that pin 1 of the connector and pin 1 of the A13J1 socket are aligned. The socket is of the variety normally used to hold integrated circuits, and pin 1 is oriented just as it would be for an integrated circuit.

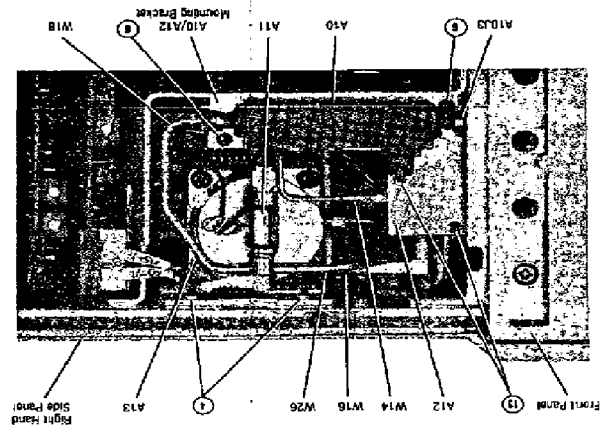
19. Refer to VIEW B. Swing the RF deck into its closed position, being careful not to pinch the A13 SYTM ribbon cable and that the various disconnected semi-rigid cables (W14 and W16 shown in VIEW B, and W13 shown in VIEW C) are not damaged by hitting microcircuit assemblies.

20. Reconnect scables W29, W28, W25, W23 and W24. Refer to VIEW C. To minimize signal leakage, lay cables W23 (A8-100 IN) and W24 (A8-MOD IN) well away from the A16 assembly.

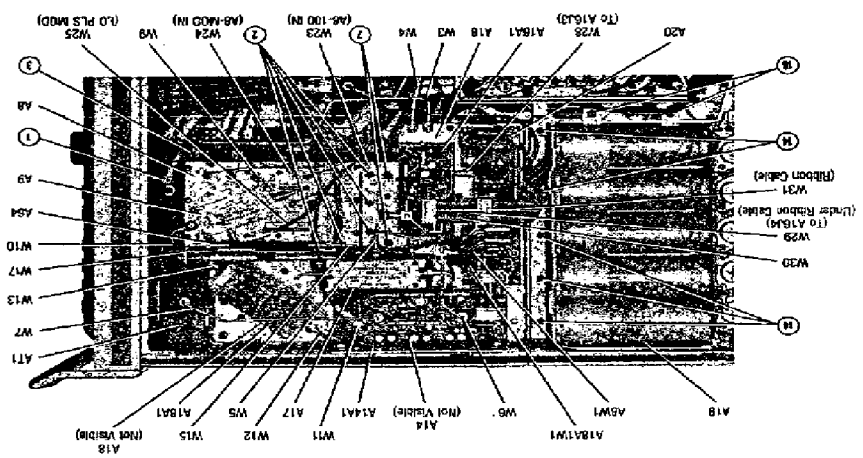
21. Reverse the Hinged RF Deck Access Procedure.



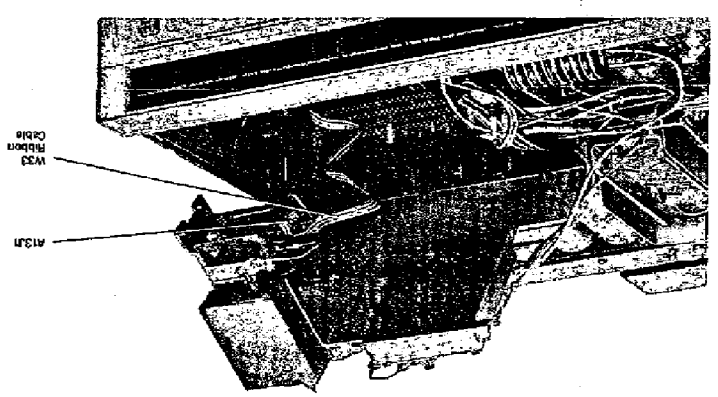
VIEW A



VIEW B



VIEW C



VIEW D

Figure B-24. Internal Assemblies, Cables, Mounting Hardware Locations

Table B-2. Reference Loop – M/N Loop Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
				REFERENCE LOOP - M/N LOOP REPLACEABLE PARTS		
A29	08340-60034	9	1	REFERENCE PHASE DETECTOR ASSEMBLY	28480	08340-60034
A30	08340-60035	0	1	100 MHz VCXO ASSEMBLY	28480	08340-60035
A31	08340-60036	1	1	M/N PHASE DETECTOR ASSEMBLY	28480	08340-60036
A32	08340-60091	8	1	M/N VCO REPLACEMENT ASSEMBLY (Includes A32 microcircuit and A32A1 bias assembly, - not separately replaceable).	28480	08340-60091
A33	08340-60038	3	1	M/N OUTPUT ASSEMBLY	28480	08340-60038
				NOTE: The A32 microcircuit, A32A1 bias, and A33 M/N output assemblies may be ordered as a single assembly, HP Part Number 08340-60092 CD9. This combined assembly has been adjusted at the factory.		
A34	08340-60039	4	1	REFERENCE M/N MOTHERBOARD ASSEMBLY	28480	08340-60039
A51	08340-60183	9	1	10 MHz REFERENCE OSCILLATOR	28480	08340-60183
				M/N LOOP ATTACHING HARDWARE		
1	2200-0103	2	6	SCREW-MACH 4-40 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
2	2200-0105	4	24	SCREW-MACH 4-40 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
3	5021-3208	7	1	HOUSING-MACH	28480	5021-3208
4	08340-60039	4	1	BOARD ASSY-REF ASSY MO	28480	08340-60039
5	86701-00024	2	1	SCOOP-AIR	28480	86701-00024
6	86701-00029	7	1	BAFFLE-AIR (TOP)	28480	86701-00029
7	86701-00030	0	1	BAFFLE-AIR (BOTTOM)	28480	86701-00030

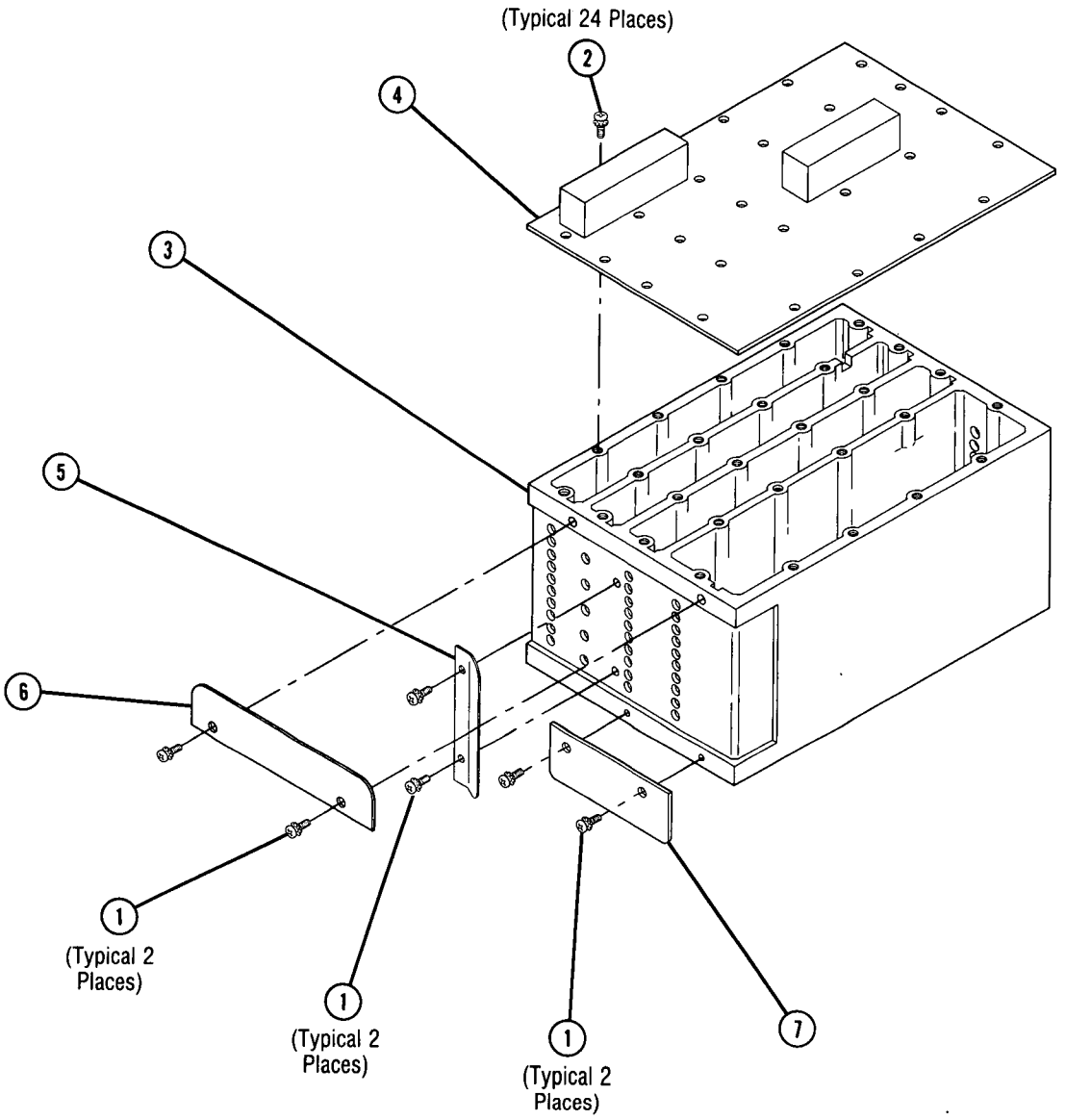


Figure B-25. Reference Loop — M/N Loop Attaching Hardware

20-30 Loops
Assembly-Level Service

CONTENTS

20-30 Loops Introduction

ASSEMBLIES

PLL2 Assemblies

- A40 PLL2 VCO (Voltage Controlled Oscillator)
- A41 PLL2 Phase Detector
- A42 PLL2 Divider
- A43 PLL2 Discriminator

PLL3 Assembly

- A39 PLL3 Upconverter

PLL1 Assemblies

- A36 PLL1 VCO (Voltage Controlled Oscillator).
- A37 PLL1 Divider
- A38 PLL1 IF

20-30 Loops
Overall Theory of Operation

The 20-30 loops provide the YIG oscillator loop with a synthesized reference signal. The YO feedback circuitry phase locks the YO to the 20-30 loops output signal as explained below:

NOTE: The phase lock loops PLL2, PLL3, and PLL1 are usually mentioned out of numeric order (e.g. instead of PLL1, PLL2, and PLL3 order). Instead, they are mentioned in functional order. PLL2 is the first phase lock loop, then PLL3, followed by PLL1.

IN CW/MANUAL MODE

The 20-30 loops directly phase lock the YO. PLL2, PLL3, and PLL1 operate together to produce high resolution tuning of the YO.

IN SWEPT MODES

The 20-30 loops are used in three different ways, depending on the frequency range over which the YIG oscillator is swept.

YO Sweep Width is Between 100 Hz and 5 MHz

The 20-30 loop is swept in this mode, and the output of the 20-30 loops sweeps the YIG oscillator. The other tuning inputs to the YO loop are held constant.

YO Sweep Width is >5 MHz

The 20-30 loops provide phase-lock reference to the YO only at the beginning of the sweep. When sweep begins, the YO phase-lock loop is opened, and the YO is swept by analog means.

Table C-1. 20-30 Loop Operation vs YO Sweep Width

YO Sweep Width	Loops Used			PLL2 VCO Divided By:	PLL1 Divide By 10	Total Divide Number	20-30 Output Resolution
	PLL1	PLL2	PLL3				
100 Hz to 5 kHz and CW Mode	X	X	X	500	ON	5000	1 Hz
>5 kHz to 100 kHz	X	X	X	25	ON	250	20 Hz
>100 kHz to 5 MHz	–	X	–	5	OFF	5	1 kHz

20-30 LOOP CHARACTERISTICS

20-30 Loop assemblies form a frequency synthesizer with the following performance characteristics:

- Fixed frequency output range from 20 to 30 MHz (required by the YO loop)
- Analog sweep widths between 100 Hz and 5 MHz
- CW frequency resolution as low as 1 Hz

The 20-30 Loops contain three phase locked loops that are used in three different configurations to achieve the required CW resolution and sweep range. The loops are referred to as PLL1, PLL2 and PLL3. PLL2 is used in all modes of operation. PLL1 and PLL3 are only used during narrow sweeps or in CW mode, and are designed to be phase-locked to the output of PLL2. The purpose of PLL3 and PLL1 are explained below.

PLL2 THEORY OF OPERATION

PLL2 Assemblies

- A40 PLL2 VCO (voltage controlled oscillator)
- A41 PLL2 phase detector
- A42 PLL2 divider
- A43 PLL2 discriminator

PLL2 VCO

The PLL2 phase lock loop is the primary phase lock loop in the 20-30 synthesizer, and is used in all modes of operation.

Refer to Figure C-1. PLL2 phase-locks to a 10 MHz signal from the reference loop. The 20-30 loops must sweep the YO directly during YO sweeps of 100 Hz to 5 Mhz, but the 20-30 loops output has to be divided down in steps to allow this. The three divided outputs each cover a portion of the 100 Hz to 5 MHz range:

YO Sweep width is between 100 Hz and 5 kHz. The 75 to 150 MHz VCO signal is divided by 500 to provide the necessary resolution, However, the output signal can not be used directly by the YO loop. The PLL3 and PLL1 loops convert this high-resolution, low-frequency signal to a frequency range that is usable by the YO loop (20 to 30 MHz).

YO Sweep width is Between >5 kHz and 100 kHz. The 75 to 150 MHz VCO signal is divided by 25 (divided by five twice). The output is 3 to 6 MHz, and can not be used directly by the YO loop. The PLL3 and PLL1 loops convert this high-resolution, low-frequency signal to a frequency range that is usable by the YO loop (20 to 30 MHz).

YO Sweep width is Between >100 kHz and 5 MHz. The 75 to 150 MHz VCO signal is divided by five to produce a 15 to 30 MHz output. This signal is sent directly to the YO loop.

PLL2 Feedback Loops

There are two feedback paths in the PLL2 Loop (refer to Figure C-1):

Analog Feedback. The VCO output is divided by 500 (divided by five twice and then divided by 20) and fed directly to the discriminator. Using the discriminator as the feedback element produces the equivalent of an extremely linear VCO.

Phase-Locking Feedback Loop. The phase-locking feedback loop compares the output of the VCO with a fixed reference signal, even though the VCO frequency may be sweeping. The A42 PLL2 divider converts the VCO frequency to a fixed 500 kHz signal that retains the original VCO signal's phase/frequency error. The A41 PLL2 phase detector compares this signal to a 500 kHz reference signal, and the phase/frequency error is sampled and fed the the A43 PLL2 discriminator. The discriminator sums the error voltage with other tuning signals and tunes the A40 PLL2 VCO.

The following is a general description of the PLL2 assemblies:

A40 PLL2 VCO

This voltage controlled oscillator is tuned by a summing amplifier on the A43 PLL2 discriminator. The VCO produces a 75 to 150 MHz signal that is divided to provide signals of three different resolutions. As explained above, these outputs are required for operation at different YIG oscillator (YO) sweep widths, or for CW/Manual operation.

To produce the different resolution signals, the 75 to 150 MHz VCO signal is divided by 5, 25, or 500. Signals that are divided by 25 or 500 are converted by PLL3 and PLL1 for use by the YO loop.

The A40 PLL2 VCO has an analog feedback loop output that goes to the A43 PLL2 discriminator, and a phase-lock feedback loop output that goes to the A42 PLL2 Divider.

The PLL2 VCO is a varactor-tuned transistor oscillator with a tuning range of 75 to 150 MHz. The phase-lock loop allows it to be programmed in 5 kHz steps between 100 and 150 MHz. The sweep width can be as wide as 25 MHz (PLL2 VCO sweeps down in frequency) and as narrow as 500 kHz. The output of the VCO is divided by several digital frequency dividers and are sent to the destinations shown in Table C-2:

Table C-2. 20-30 Loop Frequency Range vs Divider Configuration.

Output of PLL2 VCO	Frequency Range	Destination
Divided by 5	15 to 30 MHz	Used as a 20-30 output
Divided by 25	3 to 6 MHz	Sent to PLL3 Upconverter
Divided by 500	150 to 300 kHz	Sent to PLL3 Upconverter

A42 PLL2 Divider

Refer to Figure C-1. The next assembly is (functionally) the A42 PLL2 divider. This assembly converts the output of the VCO, which is sweeping during many instrument modes, to a fixed 500 KHz output. To accomplish this, a microprocessor-controlled fractional divider anticipates the instantaneous frequency and divides it by a programmed amount. The output signal contains any phase/frequency error present in the original VCO output, and is sent to the A41 PLL2 phase detector.

This assembly also divides a reference signal from the reference loop for use by the A41 PLL2 phase detector.

A41 PLL2 Phase Detector

In CW/Manual operation, this circuit passes phase-error information directly to the A43 PLL2 discriminator. During swept modes the phase-lock loop path is closed during the pre-sweep interval, and a sample and hold circuit stores the phase/frequency error voltage. The start of sweep is established with phase-lock precision. The phase-lock loop path opens and a precision voltage ramp sweeps the VCO via the A43 PLL2 discriminator.

A43 PLL3 Discriminator

This assembly sums two VCO tuning inputs and two feedback paths into a voltage-to-current converter. The output is used to tune the A40 PLL2 VCO. The inputs to the summing circuit are listed below:

Tuning Inputs:

- 20-30 precision sweep signal from the A58 sweep generator.
- Microprocessor-controlled pretune signal from a digital-to-analog converter.

Feedback Inputs:

- Analog feedback from the A40 PLL2 VCO.
- Phase/frequency error voltage from the A41 phase detector

The discriminator is a very accurate voltage-to-current converter that provides the PLL2 loop with extremely linear performance.

While the phase-lock loop is locked, the 20-30 sweep input is zero volts, and the phase detector tunes the VCO by changing the frequency-to-current ratio of the discriminator. After phase-lock is established, the phase-lock error voltage stored in the A41 assembly's sample and hold removes any warmup or drift effects. The 20-30 input is then swept, sweeping the VCO frequency. The analog feedback loop provides negative feedback to the discriminator, exactly canceling the voltage introduced at the input to the discriminator summing amplifier.

PLL3 THEORY OF OPERATION

PLL3 Assembly

- A39 PLL3 upconverter.

The PLL3 and PLL1 phase-lock loops are only used when in CW mode, or in swept frequency modes requiring YIG oscillator (YO) sweep widths less than 100 kHz.

Refer to Figure C-1. During YO sweep widths of 100 kHz to 5 MHz, the output of the PLL2 VCO (75 to 150 MHz) is divided by 5 to provide a 15 to 30 MHz output. This output is sent directly to the YO loop. For sweep widths less than 100 kHz, this configuration provides insufficient resolution (1 kHz) to set the start frequency to closer than 0.5% of the sweep width.

To provide finer resolution, the output of the PLL2 VCO is divided further (either by 25 for YO sweep widths between 5 kHz and 100 kHz, or by 500 for YO sweep widths less than 5 kHz). The frequency, however, is also reduced such that it is no longer in the 20 to 30 MHz range. PLL1 and PLL3 Loops translate the high resolution, low frequency PLL2 output up to a 200 to 300 MHz range. Since frequency translation is a fixed offset in frequency, it does not change the resolution or sweep width. After the frequency translation, the output of PLL1 is divided by ten to reduce the 200-300 MHz signal to 20-30 MHz. This also increases the output resolution by a factor of ten.

The A39 PLL3 assembly mixes 160 MHz with the output of the A40 PLL2 VCO, and outputs the sum of the two frequencies. This is done using a phase-lock loop with a closed-loop bandwidth of approximately 10 kHz. PLL3 uses a reference signal from the 100 MHz VCXO reference to generate the 160 MHz offsetting frequency. As the PLL2 output changes frequency, the PLL3 output also changes frequency with the same resolution and sweep width, but at a higher operating frequency.

Frequency Multiplier x 1.6. A 160 MHz reference signal is required to offset the PLL2 output by 160 MHz. The frequency multiplier X 1.6 generates 160 MHz by dividing the 100 MHz input reference signal by five and then selecting the eighth harmonic.

Mixer. The mixer output is amplified, filtered, and sent to the phase/frequency detector. The desired mixer output is the difference frequency and is between 150 kHz and 6 Mhz.

Phase/Frequency Detector. The phase/frequency detector generates a differential output signal that is used by the loop amplifier and the phase lock indicator.

Loop Amplifier. The phase detector differential outputs are the loop amplifier inputs. Each of the differential inputs is passed through identical low-pass filters and a voltage divider/filter. The output of the voltage divider is sent to a varactor diode that tunes the VCO.

160 to 166 MHz VCO. The 160 to 166 MHz VCO is a varactor-tuned oscillator. A buffer transistor output provides a 160 to 166 MHz signal that drives the mixer.

Phase Lock Indicator. The phase lock indicator senses the outputs of the phase detector to determine when the loop is locked. The ON=LOCKED LED indicates a phase locked condition.

PLL1 THEORY OF OPERATION

PLL1 Assemblies

- A36 PLL1 VCO
- A37 PLL1 divider
- A38 PLL1 IF

The PLL1 and PLL3 phase-lock loops are only used when in CW Mode, or in swept frequency modes with YIG oscillator (YO) sweep widths less than 100 kHz.

PLL1 is a frequency translator. It produces a 20 to 30 MHz signal that is phase-locked to:

- The 160.15 to 166 MHz output of the PLL3 upconverter
- A reference signal from the reference loop.

The 20 to 30 MHz output signal is generated by the PLL1 VCO. Refer to Figure C-1. The PLL1 VCO produces a 199 to 300 MHz signal. This is divided by 10 to produce the 20-30 MHz signal required by the YO loop. The PLL1 feedback loop phase-locks the VCO to the PLL3 upconverter's output, and to a reference signal from the reference loop.

The feedback/phase lock loop contains the A37 PLL1 divider and the A38 PLL1 IF (mixer). The PLL1 IF (mixer) phase-locks the VCO to the PLL3 output . The 160.15 to 166 MHz PLL3 output is mixed with the 199 to 300 MHz output of the PLL1 VCO. The IF signal (36 to 139.7 MHz) is divided by two (18 to 69.85 MHz). This IF signal is phase/frequency compared to a fixed 5 MHz reference signal, even though the IF frequency may be sweeping. A microprocessor-controlled fractional divider divides the IF signal by a number between 3.6 to 13.97. This produces a fixed 5 MHz output which retains the phase/frequency errors from the PLL1 VCO. The 10 MHz reference signal is divided by two, the resultant 5 MHz reference signal phase/frequency compared with the output of the fractional divider, and the error voltage is sent to the PLL1 VCO. This completes the phase-lock loop.

The following is a general description of PLL1 assemblies:

A36 PLL1 VCO

PLL1 VCO operates from 200 to 300 MHz. Its output is divided by ten to provide the 20 to 30 MHz signal required by the YO loop.

After the final divide-by-ten, the output frequency of the 20-30 loop becomes:

$$F_{out} = (F_{pll3})/10 + N1 \text{ MHz}.$$

Fp_{ll3} can be determined from the instrument diagnostics by pressing **[SHIFT] [M3]** and reading the right-hand FREQUENCY MHz display.

If this display reads 0.0000, the PLL3/PLL1 path is not being used in this mode, and PLL2 is used by itself. To determine F_{out}, the 20-30 output frequency, press **[SHIFT] [M1]** and read the right FREQUENCY MHz display. N1 can be calculated from these two frequencies using the above equation.

As the N1 divide number changes, the gain of the loop amplifier is adjusted through FET switches on the A36 PLL1 VCO assembly to maintain a constant loop gain.

The PLL1 VCO assembly also contains an output switch to select from one of two 20-30 loop paths;

1. The PLL1 VCO divide-by-ten is used as the 20-30 output. PLL2 is translated up through PLL3 and PLL1.

2. The PLL2 VCO divided output is used directly. PLL1 and PLL3 are not used.

The switch positions are defined for the different instrument operating modes in the table shown on Figure C-1.

A38 PLL1 IF (Mixer)

The A38 PLL1 IF assembly mixes the output of PLL1 VCO with the output of the PLL3 loop (Fpll3). The frequency relationships at the mixer are:

$$F1 = F2 - F_{pll3}$$

Where F1 is the PLL1 IF frequency and F2 is the PLL1 VCO frequency.

The PLL1 VCO frequency is: $F2 = F_{pll3} + 10 \times N1$ MHz

This shows that the PLL1 VCO frequency is offset by $10 \times N1$ MHz from the PLL3 output frequency.

A37 PLL1 Divider

The PLL1 phase/frequency detector, which resides on the A37 PLL1 divider assembly, operates at 5 MHz. One of the phase detector inputs comes from a 10 MHz reference (A29 reference phase detector in the reference loop), which is divided by two on the A37 assembly. The second phase detector input is the PLL1 IF output, after it passes through a divide-by-two and a fractional divider. The fractional divider uses pulse-swallowing techniques to divide by numbers between 3.60 and 13.97. It changes the sweeping IF signal to a fixed 5 MHz signal that can be phase/frequency compared to the 5 MHz reference.

When the loop is locked, both phase detector inputs are equal in frequency. The PLL1 IF output is then described by: $F1 = N1 \times 10$ MHz, where F1 is the PLL1 IF output frequency (in MHz) and N1 is the fractional divide number (3.60 to 13.97).

PLL2 OUTPUT SWITCH OPERATION

ΔF OF YIG OSCILLATOR:	100Hz TO 5kHz AND CW MODE	>5kHz TO 100kHz	>100kHz TO 5MHz	>5MHz
STEP SIZE: OUT OF 20-30MHz	1Hz	20Hz	1kHz	1Hz
SWITCH POSITION: (CONFIGURATION)	3	2	1	3

PLL1 OUTPUT SWITCH OPERATION

ΔF	POSITION
100Hz TO 100kHz AND CW MODE	2
>100kHz TO 5MHz	1
>5MHz	2

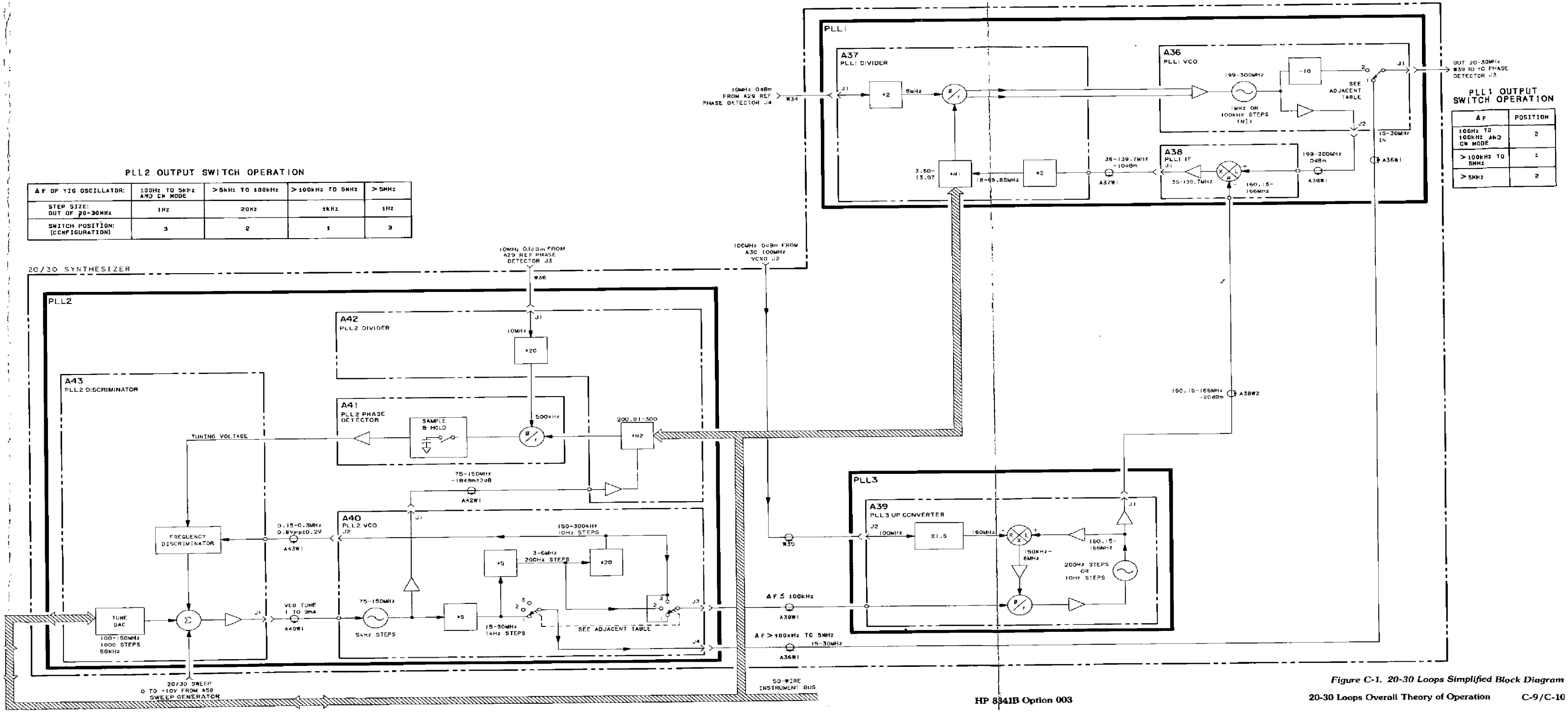


Figure C-1. 20-30 Loops Simplified Block Diagram

TROUBLESHOOTING PHASE LOCK LOOP 2

CAUTION

This instrument contains assemblies that are susceptible to damage from static electricity. Troubleshoot at a workstation equipped with a grounded anti-static mat and wrist bracelet. Place any removed assemblies on a anti-static surface or inside an anti-static bag.

Verifying the Operation of the A40 PLL2 VCO

1. Disconnect the five coax cables connected to the PLL2 VCO:
   - A43J1
   - A40J1
   - A40J2
   - A40J3
   - A40J4
2. Press **[INSTR PRESET]**.

   Using a spectrum analyzer, measure the locations shown in the following table, and verify the frequency and power at the following points:

Instrument State	Measurement Location	Normal Output Frequency (CW)	Normal Output Power (approximate)
INSTR PRESET	A40J1	>150 MHz	−18 dBm
INSTR PRESET	A40J2	>300 kHz	−15 dBm
INSTR PRESET	A40J3	>300 kHz	−15 dBm
STOP FREQUENCY = 10.05 MHz	A40J3	>6 MHZ	−5 dBm
CW MODE	A40J3	>300 kHz	−5 dBm
STOP FREQUENCY = 15 MHz	A40J4	>30 Mhz	0 dBm

3. If any of the above outputs do not meet the frequency or power values shown, repair or replace the A40 PLL2 VCO.

4. Disconnect the spectrum analyzer. Reconnect the five cables listed in step 1.

Verifying the Operation of the A42 PLL2 Divider

5. Turn the SOURCE's power switch to STANDBY and remove the A41 PLL2 phase detector.

6. Place the A42 PLL2 divider on a 36-pin extender board.

7. Turn the instrument's power switch on and press **[INSTR PRESET]**.

8. Connect an HP 1740A oscilloscope to A42TP4. Set the horizontal sweep time to 0.2 us/div. 20 cycles should be displayed across the oscilloscope display.

9. Measure A42TP5 with the oscilloscope. Verify one cycle of a pulsed waveform.

10. Set a frequency synthesizer to 100 MHz at −20 dBm and connect the output to the cable marked A40J1. This injects the signal into the N2 divider on the A42 PLL2 divider.

11. Connect an oscilloscope to A42TP1 and set the horizontal sweep speed to 0.5 us/div. The pulsed waveform consisting of two pules should be displayed.

12. Set the frequency synthesizer's frequency to several values above and below 100 MHz. As the value approaches 75 MHz, the time delay between the pulses will increase. As the value approaches 150 MHz, the time delay between the pulses should decrease.

13. If the waveforms are incorrect, replace or repair the A42 PLL2 divider. If the waveforms are correct, turn the instrument's power switch to STANDBY. Disconnect all test probes and replace the A41 phase detector, the A42 divider, and related hardware (screws). Reconnect all instrument cables. proceed to the next test.

Verifying the PLL2 Phase Detector

14. Turn the instrument's power switch to STANDBY. Remove the PLL2 discriminator and turn the power switch on.

15. Set a frequency synthesizer to 100 MHz at −20 dBm and connect its output to the cable marked A40J1.

16. Connect an oscilloscope to the φ detector test point of the top casting of the A41 PLL2 phase detector. Note the sawtooth waveform.

17. Remove the cable from A42J1, then replace it. Note that the oscilloscope trace changes levels and/or the sawtooth waveform reverses phase. Repeat this step with the cable marked A40J1.

18. Disconnect the frequency synthesizer from the cable marked A40J1. Remove the oscilloscope probe from the A40 phase detector test point.

Verifying the PLL2 Discriminator

19. Turn the instrument's power switch to STANDBY.

20. Remove all coaxial cables and mounting screws from the A43 PLL3 discriminator assembly. Place the A43 assembly on a 36-pin extender board and reconnect all coaxial cables.

21. Turn the instrument's power switch on and press:

    [INSTR PRESET]
    [START FREQ] [2] [.] [3] [GHz]
    [STOP FREQ] [7] [GHz]

22. Connect an oscilloscope to pin 1 of the extender board. Set the oscilloscope's horizontal time base to 2 ms and verify a ramp voltage from 0 to approximately 9 volts. If the ramp is not present, repair or replace the A58 sweep generator assembly.

23. Connect a DVM to A43TP1. Press the following instrument keys:

    [INSTR PRESET]
    [CW]
    [SHIFT] [GHz] [0] [Hz]
    [SHIFT] [MHz] [1] [Hz]
    [SHIFT] [kHz]
    [0] [Hz]

    Measure 0V $\pm$0.005 on the DVM. Press **[1] [0] [2] [3] [Hz]**. Measure 7.0V $\pm$0.2V on the DVM. If this test fails, repair the pretune circuit or replace the PLL2 discriminator.

24. The other inputs to this assembly have been verified in previous tests. This assemblies output is the error voltage for the PLL2 VCO. If the loop fails to lock, troubleshoot or replace this assembly.

25. Turn the instrument's power switch to STANDBY, remove the extender board and replace the A43 assembly.

TROUBLESHOOTING PHASE LOCK LOOP 3

PLL3 is fully contained on the A39 PLL3 upconverter assembly. Troubleshooting this assembly consists of verifying two inputs and one output.

1. On the instrument, press **[INSTR PRESET] [CW]**.

2. Connect an oscilloscope to A39J1 (PLL3 output) and check for a CW signal between 160 and 166 MHz at approximately -20 dBm. If this signal is present go to step 5.

   If the signal is not present, first check the inputs to the A39 assembly as follows:

Verify the 100 MHz Input to the A39 Assembly.

3. Disconnect the coax cable from A39J2 and connect the spectrum analyzer to the cable. Make sure a 100 MHz CW signal of approximately 0 dBm is present. If not, troubleshoot the reference loop. Refer to the reference loop $-$ M/N loop section.

Verify the PLL2 Input to the A39 Assembly.

4. Connect the oscilloscope to A40J3. Verify a CW signal between 0.15 and 6 MHz at 0.9V P-P ±0.2V. If this signal is not correct, troubleshoot the PLL2 loop.

Further Verification of PLL3

5. Use a frequency synthesizer to inject a 150 kHz signal into the cable marked A40J3.
6. Connect a spectrum analyzer to A39J1. Verify a 160 MHz CW signal at approximately −20 dBm. If this signal is not present, repair or replace the A39 assembly.
7. Change the frequency synthesizer output frequency to 6 MHz, and verify that the output of A39J1 is a 166 MHz CW signal at approximately −20 dBm. If this signal is not present, repair or replace the A39 assembly. If the signals described in steps 6 and 7 are correct, the PLL3 loop (A39 upconverter assembly) is functioning properly.

TROUBLESHOOTING PHASE LOCK LOOP 1

Verifying the Operation of the A36 PLL1 VCO

1. Turn the instruments power switch to STANDBY.
2. Remove the A37 and A38 assemblies mounting screws. Disconnect all coax cables going to the A37 and A38 assemblies, and remove the assemblies from the instrument.
3. Connect a spectrum analyzer to A36J2.
4. Turn on the instrument's power switch and press **[INSTR PRESET]**.
5. As the instrument is turned on, verify a −5 dBm signal at A36J2 that starts at < 200 MHz and slowly sweeps up to a CW frequency >300 MHz. If this occurs, the VCO is operating, and is sweeping up to the high end of its tuning range. **Do not** reinsert the A37 assembly, proceed directly to step 6.

   If this does not occur, repair or replace the A36 PLL1 VCO assembly.

Verifying the Operation of the A38 PLL1 IF Assembly

6. Turn the instrument's power switch to STANDBY.
7. Insert the A38 PLL1 IF assembly into the instrument and remove the A36 PLL1 VCO.
8. Connect the spectrum analyzer to A39J1. Turn the instrument's power switch on and press **[INSTR PRESET]**. Verify that the input to A38 is a CW frequency between 160.15 and 166 MHz at approximately −20 dBm. If not, troubleshoot PLL3.
9. Disconnect the spectrum analyzer and reconnect the coax cable from the A38 assembly to A39J1.

10. Using a frequency synthesizer, inject a 250 MHz CW signal, at 0 dBm, into the cable marked A36J2.

11. Connect a spectrum analyzer to A38J1 and verify a CW output between 84 and 89.85 MHz, at approximately −10 dBm. If this output is not correct, repair or replace the A38 assembly.

12. Disconnect the cables from the frequency synthesizer and the spectrum analyzer. Turn the instrument's power switch to STANDBY.

13. Reinstall the A36 PLL1 VCO and related coax cables. Leave the power switch in the STANDBY position and proceed directly to step 14.

Verifying the Operation of the A37 PLL1 Divider

14. Place the A37 PLL1 divider on an extender board. This closes the PLL1 phase lock loop. Turn the instrument's power switch on.

15. Connect a spectrum analyzer to the cable marked A37J1 and verify a CW frequency of 10 MHz at 0 dBm. If this signal is not correct, troubleshoot the reference loop. Refer to the reference loop — M/N loop section.

16. Disconnect the spectrum analyzer and reconnect the cable marked A37J1 to A37J1.

VERIFY THAT THE PHASE/FREQUENCY DETECTOR WILL CAUSE THE VCO TO REACH OPERATIONAL LIMITS.

17. Connect an oscilloscope to the A37 PLL1 divider as follows:

    Connect Channel A to A37TP11
    Connect Channel B to A37TP12
    Set the Horizontal sweep time to 2 μs/div

18. Using a frequency synthesizer, inject a 34 MHz, −10 dBm signal into the cable marked A38J1.

19. Monitor the waveforms on the oscilloscope. Note that the waveform on channel A is pulsed.

20. Change the frequency synthesizer's output to 140 MHz. Note that the waveform on channel B is pulsed.

21. Force the phase/frequency detector to reach operational limits by changing the output of the frequency synthesizer to 145 MHz.

VERIFY THE N1 DIVIDER

22. Refer to the *HP 8341B Option 003 Calibration Manual* and perform the N1 loop frequency check as described in the Frequency Range and CW Mode Accuracy test in Section 4, Performance Tests.

23. If the instrument doesn't pass this test, troubleshoot the A37 PLL1 divider or the A59 digital interface assemblies.

24. After performing all tests, turn the instrument's power switch to STANDBY. Remove all test leads. Remove the extender board and reinstall the A37 PLL1 divider. Reinstall all cables and mounting hardware.

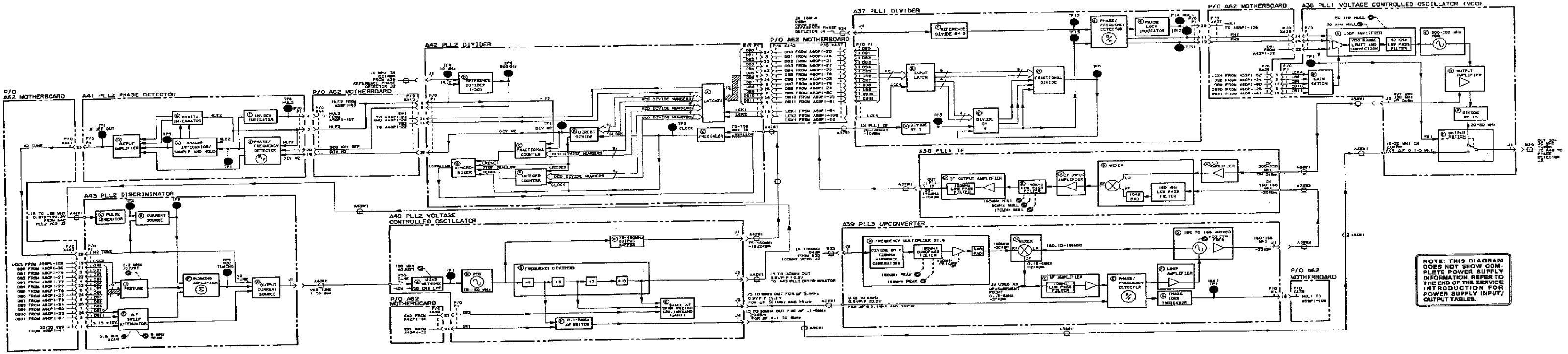
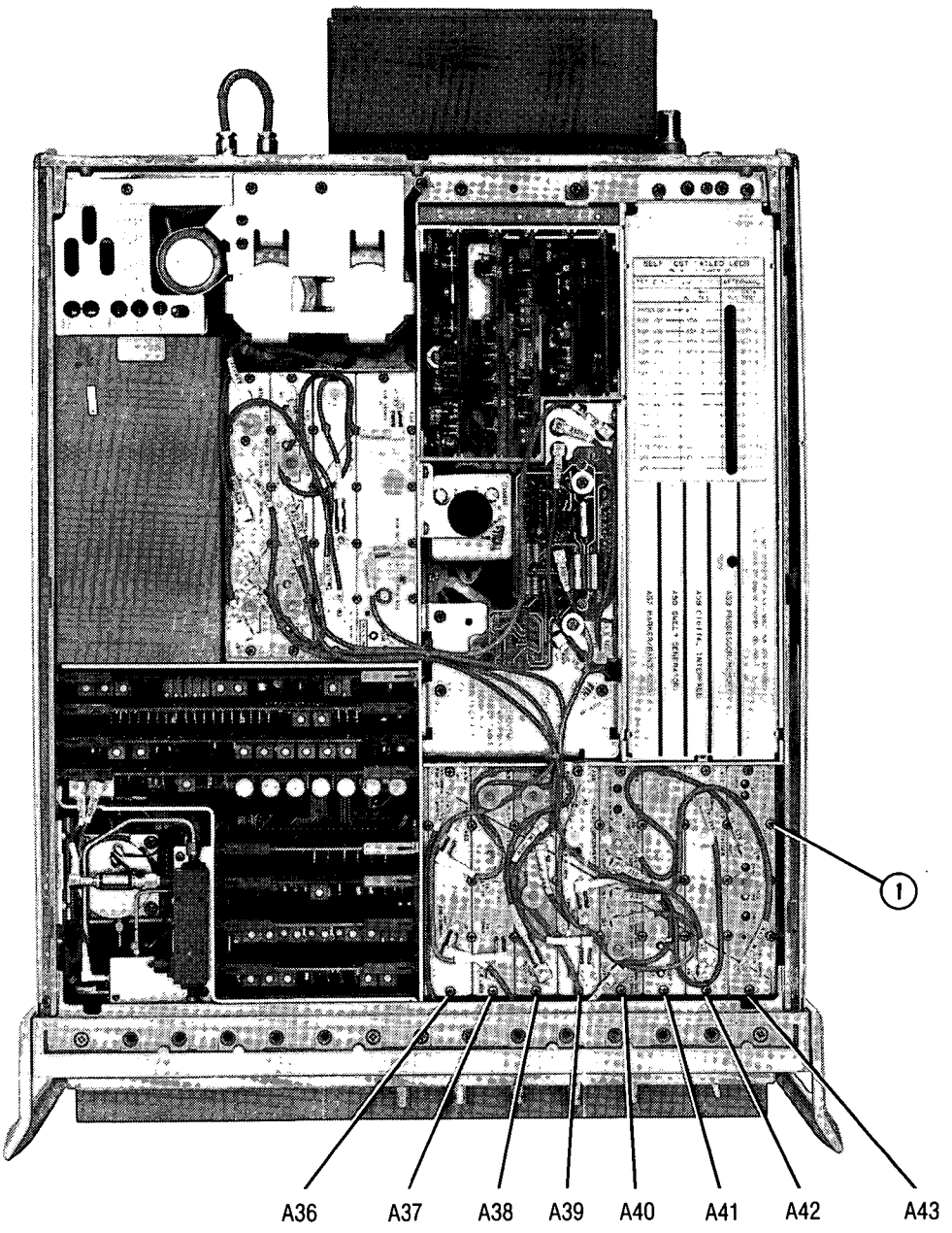


Figure C-2. 20-30 Loops Troubleshooting Block Diagram



Bottom View (Bottom Cover Removed)

Figure C-3. 20-30 Loops Major Assemblies Location Diagram

Table C-3. 20-30 Loops Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
				20-30 LOOPS REPLACEABLE PARTS		
A36	08340-60042	9	1	PLL1 VCO ASSEMBLY	28480	08340-60042
A37	08340-60043	0	1	PLL1 DIVIDER ASSEMBLY	28480	08340-60043
A38	08340-60044	1	1	PLL1 IF ASSEMBLY	28480	08340-60044
A39	08340-60045	2	1	PLL3 UPCONVERTER ASSEMBLY	28480	08340-60045
A40	08340-60046	3	1	PLL2 VCO ASSEMBLY	28480	08340-60046
A41	08340-60162	4	1	PLL2 PHASE DETECTOR ASSEMBLY	28480	08340-60162
A42	08340-60048	5	1	PLL2 DIVIDER ASSEMBLY	28480	08340-60048
A43	08340-60049	6	1	PLL2 DISCRIMINATOR ASSEMBLY	28480	08340-60049
				20-30 LOOPS ATTACHING HARDWARE		
1	2200-0105	4	43	SCREW-MACH 4-40 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION

Sweep Generator – YO Loop Assembly-Level Service

CONTENTS

Sweep Generator — YO Loop
Introduction

The inputs to this functional group come from the instrument processor, the 20-30 loop, and the M/N loop. The main output is YO RF output. Other important outputs are PRETUNE, used to tune the YIG oscillator (YO) and the A13 switched YIG-tuned multiplier (SYTM); BVSWP (buffered voltage sweep), used on the A27 level control assembly; 20-30 SWP, used to sweep the 20-30 loop for sweep widths ≤5MHz; and MKR RAMP, used as the reference for all sweep events.

ASSEMBLIES

The Sweep Generator — YO Loop consists of the following assemblies:

Main Tuning Assemblies (Listed in Functional Order)

- A58 Sweep Generator Assembly
- A54 YO Pretune/Delay Compensation Assembly
- A55 YO Driver Assembly
- A47 Sense Resistor Assembly

RF Source

- A44 YIG Oscillator/A44A1 Bias Assembly

Feedback Loop Assemblies (Listed in Functional Order)

- A45 Directional Coupler
- AT2 15 dB Attenuator
- A46 7 GHz Low-Pass Filter
- A48 YO Loop Sampler Assembly
- A49 YO Loop Phase Detector Assembly
- A50 YO Loop Interconnect Assembly
- A55 YO Driver

Frequency Modulation

- A23 FM Driver

Sweep Generator – YO Loop Theory of Operation

SWEEP GENERATOR – YO LOOP OVERALL THEORY OF OPERATION

Main Tuning Assemblies

Four instrument assemblies provide coarse tuning for the A44 YIG Oscillator (YO), these are:

A58 Sweep Generator. This assembly produces signals required to sweep the YO when in swept instrument modes.

A54 YO Pretune/Delay Compensation Assembly. The A54 assembly tunes the YO close to the desired output frequency. The following signals are summed on the A54 assembly:

- The coarse tuning signal (VSWP) from the A58 sweep generator (during sweeps >5 MHz only).
- A microprocessor-controlled pretune voltage.
- A fixed reference voltage.

The resultant signal, PRETUNE, is sent to the A55 YO driver and the A28 SYTM driver. The A28 assembly is in the RF Section.

The A54 assembly delay compensation circuitry counteracts the sweep delay inherent in the YIG oscillator. This circuit is controlled by the instrument microprocessor. VCOMP speeds the YIG oscillator's response during a sweep. This compensates for YO eddy current-related delays. VCOMP is sent to the A55 YO driver.

This assembly also produces a kick pulse (LKICK) that eliminates magnetic hysteresis in the YIG oscillator. This kick pulse is also sent to the A55 YO driver.

A55 YO Driver. The A55 YO driver sums VSWP, VCOMP, and LKICK and converts them into a current signal to drive the YIG oscillator's main coil. The A55 assembly is also in the phase-lock feedback loop. Low frequency phase/frequency error voltages are summed into the voltage-to-current converter with the VSWP, VCOMP, and LKICK signals. Low frequency phase-error correction must be input to the YO main coil, which can respond to signals below 100 Hz. High frequency phase-error correction is explained in the feedback loop description, below.

A47 Sense Resistor Assembly. The YO main coil requires a powerful current source. The A55 YO driver can not supply the required current, so its output is amplified by the A47 sense resistor assembly and sent to the YIG oscillator's main coil.

This assembly contains the high current components of the A55 YO driver's voltage-to-current converter. The components are placed on the A47 assembly for proper heat dissipation. This assembly also contains high power portions of the A28 switched YIG-tuned multiplier driver assembly (part of the RF section). This function is relevant to the RF section.

RF Source

A44 YIG Oscillator/Bias Assembly. The A44 YIG oscillator (YO) provides the fundamental RF output frequency for the instrument. The frequency range of the YO is 2.3 to 7.0 GHz.

The YO uses two tuning coils:

- Main Coil

The main coil is the primary tuning component of the YO. The main coil tunes the YO to within the capture range of the phase-locked YO feedback loop (within ± 20 MHz of selected frequency), and provides low-frequency (<100 Hz) phase-error correction.

- FM Coil

The FM coil frequency modulates the YIG oscillator when a signal is input to the instrument's FM input BNC. The FM coil also allows high frequency (>100 Hz) phase-error correction, that is provided by the A49 YO loop phase detector (described below).

Feedback Loop Assemblies

A45 Directional Coupler. The directional coupler splits the output of the YIG oscillator. One output goes to the RF Section (and eventually to the instrument's RF output) and the other goes to the YO feedback loop. The feedback loop portion goes to the AT2 15 dB attenuator.

AT2 15 dB Attenuator. AT2 attenuates the coupled-off portion of the YIG oscillator output. Signal attenuation is required so that the feedback signal can be mixed with a synthesized reference and be phase/frequency compared. These processes are described below. AT2 also provides isolation between the feedback loop assemblies and the YIG oscillator.

A46 7 GHz Low Pass Filter. The low pass filter reduces harmonics from the coupled-off YIG oscillator output to prevent unwanted mixing products in the A48 YO loop sampler.

A48 YO Loop Sampler. The sampler mixes the coupled-off YIG oscillator output (from the A46 assembly) with the synthesized output of the M/N loop. The output is a 20 to 30 MHz difference signal, that is sent to the A49 YO loop phase detector.

A49 YO Loop Phase Detector. The 20-30 MHz IF signal from the A48 assembly is phase/frequency compared to the output of the 20-30 synthesizer. The resultant error signal is integrated and sent to the sample and hold circuit.

SAMPLE MODE. This no-memory mode sends a low frequency error correction signal (YO TUNE) directly to the A55 YO driver. This mode is used in CW/Manual operation, or in swept mode when the YIG oscillator (YO) is swept 5 MHz or less. This completes the YO feedback loop and phase-locks the YO.

HOLD MODE. This mode must be used when the YO is swept >5 MHz. Sample mode first allows the YO to phase-lock at the beginning of the sweep. Afterwards, the hold mode holds the YO TUNE voltage constant while VSWP is summed into the PRETUNE signal, which in turn sweeps the YO. This sequence is repeated at the beginning of each sweep.

The other outputs of the A49 phase detector are:

- FM Coil Drive – The high frequency (>100 Hz) phase/frequency error voltage is output to the YO FM coil.
- High Unlock YO – Outputs a TTL high when the YO loop is unlocked. The status of the YO loop is monitored by the instrument microprocessor.
- Low Overmod – Outputs a TTL low when the phase difference between the sampler IF and the 20-30 synthesizer is greater than approximately 300°.

Frequency Modulation

A23 FM Driver. This assembly receives the ±1V or ± 8V frequency modulation input from J22 on the front panel. Frequency modulation voltage information is converted to a corresponding current that goes directly to the A44 FM coil via the A62 motherboard and A44A1 YO bias assembly.

The FM driver outputs a low signal (LOMD) if the the peak deviation of the FM input signal exceeds 10 MHz.

SWEEP GENERATOR – YO LOOP FUNCTIONAL GROUP THEORY OF OPERATION

This functional group can best be described by considering the two main instrument modes of operation: CW/manual, and swept frequency. The swept mode can be in one of three conditions: single band sweep, multiband sweep, or narrow band sweep.

CW/MANUAL Sweep Operation

When either mode is selected, the sweep generator/YO loop circuitry phase-locks the YO at the appropriate frequency. The instrument microprocessor addresses and sends a number to the A54 YO pretune/delay compensation assembly, which produces a proportional voltage, VDAC. VDAC is summed with the constant DC voltage, VREF, producing PRETUNE – a voltage that tunes the YO to approximately the desired frequency (i.e. to within the capture range of the YO phase-locked loop). VSWP makes no contribution to the PRETUNE voltage in CW operation.

The processor also sets the frequencies of the M/N and 20-30 synthesizer loops according to the CW frequency selected. The outputs of these two loops are used by the YO loop to exactly tune and phase-lock the YO. The A45 directional coupler couples a portion of the YO RF output back through a low-pass filter to the A48 sampler, where it is mixed with the Nth harmonic of the M/N output. This generates a difference signal, Sampler IF, in the range of 20-30 MHz that is input to the A49 YO loop phase detector. There the phase is compared to the 20-30 MHz output signal. The resultant error signal, YO TUNE, phase-locks the YO. The high frequency portion on YO TUNE (>100 Hz) is applied to the YO FM coil by the FM coil driver on the A49 YO loop phase detector assembly. The low frequency portion (<100 Hz) is summed with PRETUNE on the A55 YO driver and applied to the YO main coil. This completes the YO loop and phase-locks the YO.

Manual Sweep operation is identical to CW in the operation of the sweep generator and YO loop circuitry.

Swept Mode

Single Band Sweeps >5 MHz. In swept mode, the instrument phase-locks the YO at the beginning of each sweep, undergoing the same sequence of events as in the CW mode. The sample and hold on the A49 YO loop phase detector assembly holds the YO TUNE error signal constant at its phase-locked value. In the hold mode the YO phase-lock loop is opened, allowing a ramp signal, VSWP, to be summed into the PRETUNE signal and subsequently applied to the YO main coil to sweep the YO. This sequence is called lock and roll. The processor writes the sweep time and sweep width numbers to to the A58 sweep generator assembly, which generates the voltage ramp, VSWP, with the appropriate slope and duration. The A58 sweep generator assembly also generates a 0 to 10V ramp (MKR RAMP), that has the same duration as VSWP.

Because of the inherent delay characteristics of the YO during sweeps, a ramping compensation voltage, VCOMP, is summed with PRETUNE in the A55 YO driver. VCOMP is generated by summing correction data from the processor with the VSWP ramp. This is done in the YO Delay Compensation portion of the A54 YO pretune delay compensation assembly.

At each YO sweep retrace, the YO retrace kick pulse generator (on the A54 assembly) produces a pulse with a programmable width (via the microprocessor) that is sent to the A55 YO driver. This signal causes current drain from the YO tuning coil. When activated, this momentarily tunes the YO lower in frequency (by about 2.5 GHz) to remove the effects of YO magnetic hysteresis.

Multiband Sweeps. The operation of the sweep generator/YO loop circuitry in multiband sweeps is essentially the same as in single band sweeps. The difference is that at each band crossing, the YO is retraced and the lock and roll sequence is initiated again. This produces a pause in the instrument sweep at each bandcrossing while each loop is being reset. VSWP is reset to zero volts between bands, however the MKR RAMP signal remains fixed at its end-of-band value until the lock and roll sequence for the next band begins. The sum of the durations of the ramping portions of MKR RAMP will still equal the selected instrument sweep time.

VSWP has a sensitivity of +2 V/GHz of YO frequency. The distinction between YO frequency and instrument frequency is important because the instrument frequency is not necessarily the same as the YO frequency. In the 10 MHz to 2.3 GHz band (band 0), the YO output is heterodyned with a 3.7 GHz oscillator. Consequently, the YO frequency is 3.7 GHz higher than the instrument frequency.

In the higher bands (SYTM multiply bands 1 through 3, the instrument frequency is derived from the first, second, or third multiple of the YO frequency as shown in Table D-1.

Table D-1. RF Output Frequency vs. YO Frequency

Band	Multiplication	RF Output Frequency	YO Frequency
0	Heterodyned (mixed)	0.01 to 2.3 GHz	3.71 to 6.2 GHz
1	YO fundamental used	2.3 to 7.0 GHz	2.3 to 7.0 GHz
2	Multiplied by 2	7.0 to 13.5 GHz	3.5 to 6.75 GHz
3	Multiplied by 3	13.5 to 20.0 GHz	4.5 to 6.67 GHz

The mixing and multiplying make bandcrossings necessary. At each crossing, VSWP resets to zero and the YO is phase-locked to the appropriate frequency for the start of the next band. The result is that in a multi-band sweep the MKR RMP is a ramp that pauses for bandcrossings, and VSWP is a series of ramps, each starting at zero volts. The slope of any particular ramp depends on the YO harmonic being used in that band.

The MKR RMP is a 0 to +10V ramp used as the reference for all sweep events. In a single band sweep, the voltage goes linearly from 0 to +10 volts in the selected sweep time. In a multi-band sweep, the voltage is a segmented ramp where the linear ramp portions correspond to the particular bands swept, and the flat portions correspond to the time necessary to re-phase-lock the instrument for the next band. In the multi-band case the sum of the times for the various linear ramp portions equal the selected instrument sweep time. That is to say, the instrument sweep time is the time during which the instrument is actually sweeping and does not include the re-phase-lock time at each band-crossing.

Narrow Band Sweep. YO sweep widths $\leq$5 MHz are achieved by sweeping the 20-30 synthesizer. The A58 sweep generator assembly produces the 20-30 SWP (from inputs from the processor), that causes the 20-30 output to sweep in frequency. The A49 YO loop phase detector keeps the YO phase-locked to this signal for the duration of the sweep. For narrow band YO sweep widths between 500 kHz and 5 MHz, PRETUNE is also swept (VSWP summed in) a proportional amount so that the pretuned YO frequency remains within the capture range of the YO phase lock loop. This is in addition to the phase-locked error correction by YO TUNE. For YO sweep widths $<$ 500 kHz, VSWP is disabled, and YO TUNE alone supplies the correction to keep the YO phase-locked for the entire sweep ramp voltage.

YO Loop Detailed Theory Of Operation

The assemblies (documented in this functional group) that comprise the YO loop are show below:

- A44 YIG oscillator
- A45 directional coupler
- AT2 15 dB attenuator
- A46 7 GHz low pass filter
- A48 YO loop sampler assembly
- A49 YO loop phase detector assembly
- A50 YO loop interconnect assembly
- A54 YO pretune/delay compensation assembly
- A55 YO driver assembly

In CW and manual modes, the YO loop phase-locks the YO at the appropriate frequency. The information to tune the YO comes from two sources: PRETUNE and YO TUNE, that combine to form the YO FM COIL DRIVE and the YO MAIN COIL DRIVE.

Pretune. The PRETUNE voltage is generated on the A54 YO pretune/delay compensation assembly. It is the scaled sum of VDAC, a tune voltage generated from inputs from the instrument processor, and VREF, a constant DC offset voltage. PRETUNE has a sensitivity of −2.5V/GHz of YO sweep.

VCOMP makes no contribution to PRETUNE in the CW or Manual modes. LVSX (low voltage sweep disable) is low to shunt out any unwanted noise contribution from the VSWP line.

YO Tune. The YO TUNE voltage is generated by the A49 YO loop phase detector from the 20-30 MHz input (from the 20-30 loop) and the Sampler IF, which is the down-converted product of the YO RF output and the Nth harmonic of the M/N output. The A45 directional coupler couples a portion of the YO output back through the AT2 15 dB attenuator and A46 7 GHz low pass filter to the A48 YO loop sampler. There it is mixed with the Nth harmonic of the M/N output to produce the Sampler IF, that is in the frequency range of 20-30 MHz. This signal and the one from the 20-30 loop are compared in the A49 YO loop phase detector. The resulting error signal is amplified and integrated to produce YO TUNE, with a sensitivity of −3 MHz/V. When HLEY (high lock enable YIG oscillator) is high, the YO loop is closed. When HLEY is low, the sample and hold circuit holds the phase-locked value of YO TUNE constant, breaking the loop to allow a voltage ramp (VSWP) to be summed into PRETUNE to sweep the YO.

YO FM Coil Drive. The A49 FM coil driver has a 100 Hz high pass filter. Only high frequency (>100 Hz) portion of YO TUNE is applied to the YO FM coil. The resulting output is the YO FM COIL DRIVE current. The low frequency portion (<100 Hz) of YO TUNE is summed with PRETUNE and applied to the YO main coil.

YO Main Coil Drive. The YO MAIN COIL DRIVE current is derived at the A55 YO driver from the PRETUNE and YO TUNE voltages. The A55 YO driver sums YO TUNE with the OFFSET voltage, and scales PRETUNE via the GAIN adjustment. The YO MAIN COIL DRIVE current is constructed as a linear function of the desired YO frequency. The OFFSET adjustment varies the offset of the curve; the GAIN adjustment varies the slope. These two adjustments are used to ensure the tuning accuracy of the YO versus PRETUNE voltage over its full range of operating frequency. OFFSET has greater effect on the low end of the range (2.30 GHz), and GAIN has greater effect on the high end (6.99 GHz).

The A55 YO driver voltage-to-current converter and the A47 sense resistor assembly are part of the same circuit. This circuit converts the (scaled) sum of the PRETUNE and YO TUNE voltages to the YO MAIN COIL DRIVE current that drives the YO main coil. This completes the YO loop, which tunes and phase-locks the YO.

Sweep Generator Detailed Theory Of Operation

The following assemblies cause the frequency of the instrument to sweep:

- A58 sweep generator
- A54 YO pretune/delay compensation assembly
- A55 YO driver.

When the YO loop phase-locks at the start frequency of an instrument sweep or at the start of a new band, the A54 YO pretune/delay compensation assembly provides PRETUNE voltage to the A55 YO driver. PRETUNE is a DC voltage proportional to the frequency at which the YO is locking. The sensitivity of this voltage is −2.5 volts/GHz (YO frequency). The A55 YO driver converts this voltage to a current that is also proportional to the lock frequency. This current is fed to the YO main coil where it tunes the frequency of the YO to be within the capture range of the YO phase lock loop.

For sweep widths >5 MHz, the A49 YO loop phase detector opens the YO phase-locked loop by activating the sample and hold, thus holding YO TUNE constant at its phase-locked value. The A58 sweep generator provides a voltage ramp which is summed with the PRETUNE voltage on the A54 YO pretune/delay compensation assembly. The resulting voltage ramp produces a current ramp from the A55 YO driver assembly that in turn sweeps the frequency of the YO.

VSWP is also used on the A54 YO pretune/delay compensation assembly to produce another negative going ramp called VCOMP. This is added to PRETUNE on the A55 YO driver assembly to compensate for the eddy-current induced swept frequency error inherent in the YO magnetic structure.

When a bandcrossing or end of sweep is reached, LBX (low bandcross) and HSP (high sweep) are pulled low by the A57 marker/bandcross assembly. This causes VSWP to pause (stop ramping). The instrument processor pulls LRSP (low reset sweep) low, resetting VSWP to zero volts.

To eliminate unwanted magnetic hysteresis, the instrument processor initiates a retrace kick via the YO retrace kick pulse generator in the A54 YO pretune/delay compensation assembly. This pulse is sent to the A55 YO driver where it is converted to a 60 ma current drain on the YO drive current. This temporarily offsets the YO frequency by approximately −2.5 GHz, eliminating the magnetic hysteresis in the YO.

Finally, the instrument processor sets PRETUNE to a value proportional to the next lock frequency. When the loop is locked, the sweep sequence is repeated.

In sweeps where the YO is to sweep 5 MHz or less, the 20-30 loop is swept and the YO loop remains phase-locked. Since the YO loop is phase-locked to the 20-30 loop output, the YO frequency will follow that of the 20-30 loop.

The 20-30 loop is swept by a voltage ramp, 20-30 SWP, generated by the A58 sweep generator assembly. For YO sweeps <500 kHz, the sweep width range attenuator on the A58 sweep generator assembly is open-circuited so that VSWP remains at zero volts.

START/STOP Sweep Operation. Starting and stopping the sweep ramp is controlled primarily by high sweep (HSP), which is generated on A57 marker/bandcross assembly (located in the controller section). When HSP is high, the A58 sweep generator is free to sweep. When HSP is low, the A58 sweep generator stops, but does not reset sweep voltage, VSWP.

The A57 marker/bandcross assembly pulls HSP low, stopping the sweep whenever any one of the following three events takes place.

- LBX (low bandcross) goes low. The A57 marker/bandcross assembly pulls LBX and HSP low at bandcrossings and at the end of the sweep. The A58 sweep generator pulls LBX low if there is an instrument malfunction that allows VSWP to go beyond its normal limits.
- LSSP (low stop sweep) on the rear panel is pulled low. Note: this line is meant for special, dedicated applications and is not designed to be a general purpose stop sweep input.
- The instrument microprocessor issues a STOP SWEEP.

The A57 marker/bandcross assembly drives HSP high, starting a sweep whenever any one of the following three events takes place.

- A line trigger input is received after line trigger mode has been selected.
- An external trigger input is received after external trigger mode has been selected.
- The instrument processor issues GO SWEEP IMMEDIATE.
- LSSP on the rear panel goes high after the instrument processor has completed its tasks and is waiting for the input.

The A57 marker/bandcross assembly controls the timing of the various sweep events (marker on/off, bandcross, and end of sweep) by monitoring MKR RMP. This is a zero to ten volt ramp generated by the A58 sweep generator assembly. A buffered version of this, SWEEP OUTPUT, is available on the front and rear panels. MKR RMP pauses for bandcrossings. It starts at zero volts at the beginning of each sweep. It reaches five volts at the center frequency of the sweep and goes to ten volts at the end of the sweep.

A23 FM Driver Theory of Operation

The front panel FM input can accept an AC signal that is sent to the A23 FM driver. This signal can be of two different ranges: ±8 Vac in 1 MHz/V FM sensitivity or ±1 Vac in 10 MHz/V FM sensitivity. The FM driver scales this signal and converts it into a current that drives the YIG oscillator's FM coil.

The FM Driver provides:

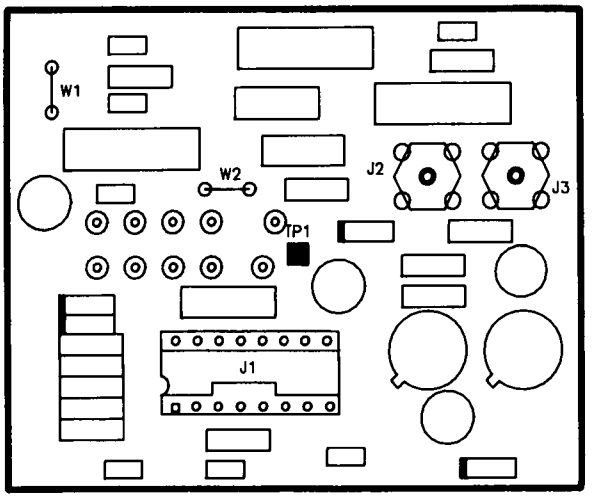
- FM input range attenuation
- Harmonic number (band number) attenuation
- FM overmodulation detection
- FM coil drive.

A44/A44A1 YIG Oscillator/Bias Assembly Theory of Operation

NOTE: The A44 microcircuit and A44A1 bias assembly are not field repairable and are not separately replaceable.

The FM coil in the instrument is connected to chassis ground at the bias assembly. During testing, however, the coil must be floating so a jumper has been provided to connect ground after testing.

YO Switchable Filtering. The filtering required at the YO main coil depends upon whether the instrument is in the CW mode or in swept modes. A switch circuit is provided to accomplish this filter change. A signal from the processor (HFIL) goes high in CW mode. This signal is buffered on the A50 YO loop interconnect assembly. The resulting signal (LFIL) goes to the A44A1 YO bias assembly where it provides a very low impedance path for the CW filter circuit. The CW filter is connected directly across the YO main coil in CW mode. The filter reduces residual FM of the YO. A swept mode filter matches the delay characteristics of the YO main coil to those of the YO main coil driver circuitry.



NOTE

Refer to Sweep Generator — YO Loop Troubleshooting Block Diagram for schematic of A44.

Figure D-1. A44A1 YIG Oscillator Bias Assembly Drawing

A45 Directional Coupler Theory of Operation

The A45 directional coupler divides the RF output of the A44 YO into two paths. The output of the coupled arm goes to A45J1. This signal is attenuated by AT2 and goes through the A46 7.0 GHz low pass filter to the A48 YO loop sampler. The sampler mixes the coupled-off YO signal with the Nth harmonic of the M/N output signal. The result is the Sampler IF signal, which goes to the A49 YO loop phase detector.

The RF signal from the coupler's main path is the YO output signal at A45J3. This signal is sent to the A16 modulator/splitter (located in the RF section).

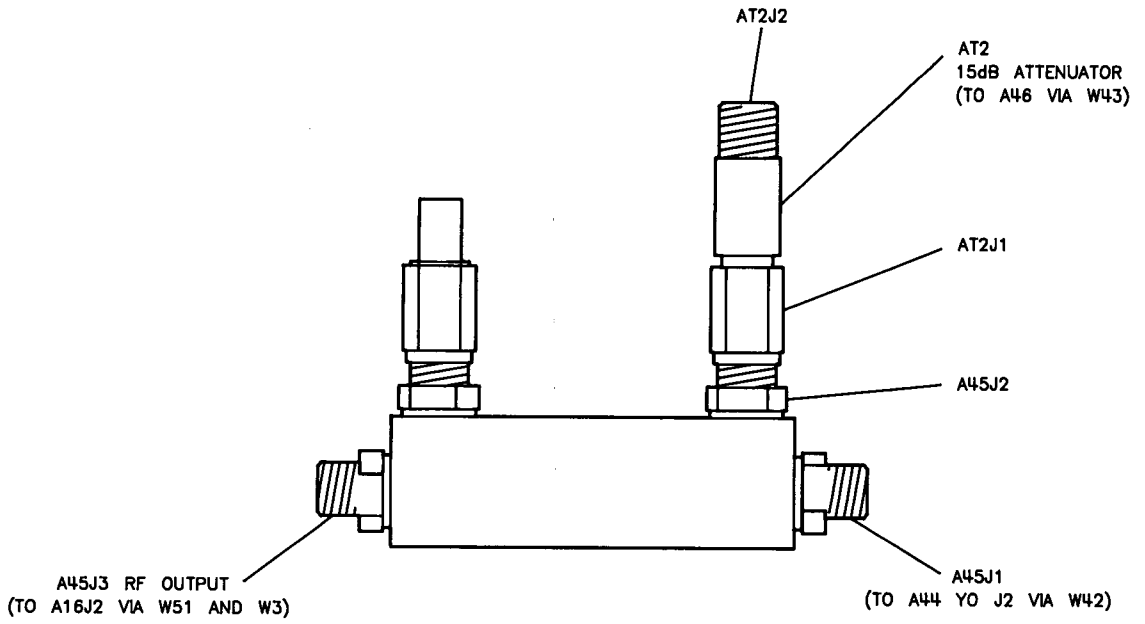


Figure D-2. A45 Directional Coupler Assembly Drawing

A46 7 GHz Low Pass Filter Theory of Operation

The A46 7 GHz low pass filter is connected by coaxial cables between the AT2 15 dB Attenuator and the A48 YO loop sampler. It filters out the harmonics of the coupled-back portion of the YO output from the directional coupler to prevent unwanted mixing products in the sampler.

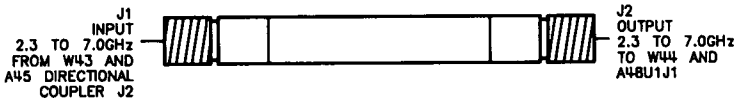


Figure D-3. A46 7.0 GHz Low Pass Filter Assembly Drawing

A47 Sense Resistor Assembly Theory of Operation

The A47 sense resistor assembly contains the high power portions of both the A55 YO driver and the A28 SYTM driver. The A28 assembly is discussed in the RF Section.

Many components on the A47 sense resistor assembly are part of the A55 YO driver voltage-to-current converter. These components are mounted on the A47 assembly (which is a heat sink) for proper heat dissipation.

A48 YO Loop Sampler Theory of Operation

The A48 YO Loop Sampler mixes the output of the A44 YIG oscillator (via the A45 directional coupler, AT2 15 dB attenuator and A46 7 GHZ low pass filter) with the Nth harmonic of the output of the M/N Loop. The sampler IF output is a 20 to 30 MHz difference signal that is output to the A49 YO loop phase detector.

A49 YO Loop Phase Detector Theory of Operation

Sampler IF signal (from the A48 YO loop sampler) and the 20-30 MHz signal (from the A36 PLL1 VCO) are inputs to the A49 YO loop phase detector assembly. These signals are phase-compared and the result is integrated to produce the following signals:

- YO TUNE
- FM Coil Drive
- High Unlock YO (HULY)

YO TUNE. Phase-locks the YO. Coarse error correction and AC noise >100 Hz are performed by YO TUNE (via the A55 YO driver and YO main coil).

The YO frequency is related to the M/N output frequency and the 20-30 MHz reference loop frequency in the following way:

$$F_{YO} = (N)(F_{M/N}) - F_{20\text{-}30}$$

Where:

F_{YO} = YO output frequency (MHz)

N = N number input to the M/N Loop (harmonic near the frequency to which the YO loop is tuned)

$F_{M/N}$ = M/N loop output frequency (MHz)

$F_{20\text{-}30}$ = 20-30 loop output frequency (MHz) (the 20-30 frequency can be changed in 1 Hz steps)

The YO TUNE output from the A49 YO loop phase detector board goes to the A55 YO driver where it is summed with the PRETUNE voltage from the A54 YO pretune/delay compensation assembly. This sum is applied to the YO main coil.

FM Coil Drive. This signal provides >100 Hz AC error correction to the YO. The YO FM coil drive from the A49 YO loop phase detector assembly goes to to the A44A1 YO bias assembly and then to the YO FM coil.

A50 YO Loop Interconnect Assembly Theory of Operation

The A50 YO loop interconnect assembly distributes power and signals to the A48 YO sampler assembly, the A49 YO phase detector, and the A44A1 YO bias assembly. It also contains the following signals, each of which is provided with a test point.

TP2 LOMD low = FM overmodulation is occurring.
TP4 HFIL high = The YIG Oscillator CW filter is engaged.
TP5 HLEY high = The YIG Oscillator loop phase-lock is enabled.
TP7 HULY high = The YIG Oscillator loop is not phase-locked.

The test points serve two purposes:

- Each test point can be used to monitor the state of the digital signal (The level will be somewhat less than the actual signal level due to the resistors on each side of the test points).
- The test point can also be used to force a logic condition to occur by connecting it to +5V or ground.

Test points are provided on the YO loop interconnect assembly for each supply voltage and for the YO coil voltage.

The A50 YO loop interconnect assembly isolates and separately filters supplies going to different portions of the YO loop assembly.

A54 YO Pretune/Delay Compensation Assembly Theory of Operation

The A54 YO pretune/delay compensation assembly performs three major functions:

- It provides a DC voltage (PRETUNE) to the A55 YO driver that is proportional to the frequency to which the YO is being phase-locked. The YO sensitivity of this line is −2.5 V/GHz (of YO frequency). PRETUNE is also used by the A28 SYTM driver to tune the A13 switched YIG-tuned multiplier (located in the RF section).
- It generates the kick pulses that are necessary at a YO retrace to eliminate magnetic hysteresis. These pulses are of constant amplitude, corresponding to about 2.5 GHz, and are of varying width. The width is a function of the YO start frequency and sweep width of the previous sweep as well as the YO start frequency of the next sweep. These pulses are subtracted from the phase-lock PRETUNE voltage and temporarily tune the YO 2.5 GHz below the next phase-lock frequency.
- It provides a voltage (VCOMP) to the A55 YO driver that compensates for the YO's normal delay at start of sweep.

A55 YO Driver Assembly Theory of Operation

The A55 YO driver performs the following functions:

- It acts as a voltage-to-current converter to change the PRETUNE voltage (sensitivity = −2.5 V/GHz) to YO main coil current (sensitivity is approximately 24 ma/GHz). The two sensitivities mentioned above are expressed in terms of YO frequency, not RF output frequency.
- It provides the summing point for the low frequency portion (<100 Hz) of the YO phase-locked loop error voltage (YO TUNE).
- It provides the summing point for the YO delay compensation voltage (VCOMP).
- It provides the summing point for the YO coil offset current.
- It provides the driver circuitry for the YO retrace kick pulse.

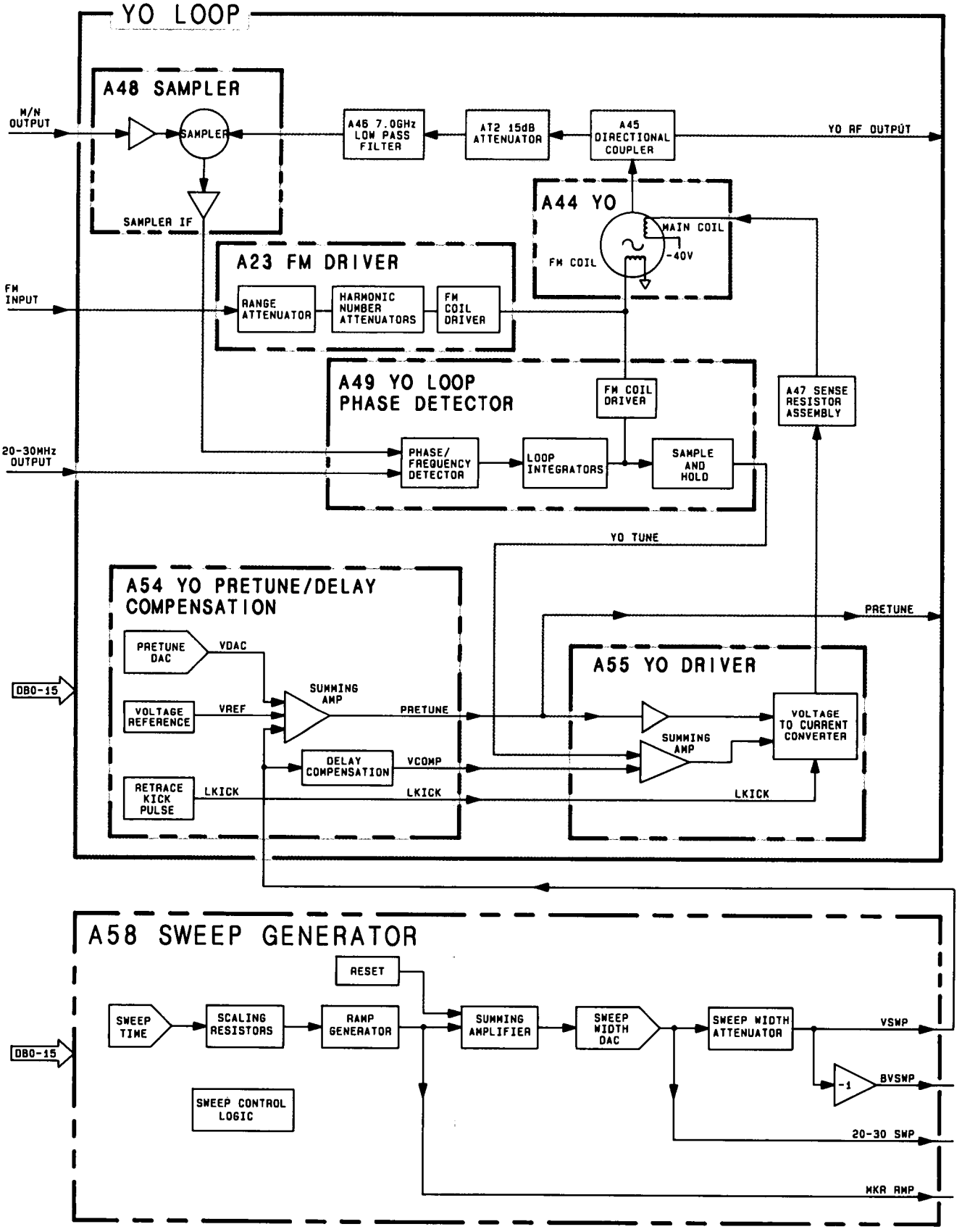


Figure D-4. Sweep Generator — YO Loop, Simplified Block Diagram

YO Loop
Assembly-Level Troubleshooting

INTRODUCTION

The YO UNLOCKED error condition can be caused by a number of different failures. Figure D-5, YO Loop Troubleshooting Flow Chart, provides a systematic way to identify the malfunctioning assembly. Also refer to Figure D-4, Sweep Generator and YO Loop Simplified Block Diagram. Each of the following headings refer to the Troubleshooting Flow Chart and assumes that the front panel UNLK indicator is on.

Power levels are shown on Figure D-6. Sweep Generator and YO Loop Troubleshooting Block Diagram.

YO UNLK – CW/MANUAL MODE

NOTE: The **[SHIFT] [M4]** diagnostic can help isolate the cause of an UNLK condition. Use this diagnostic feature after performing the troubleshooting procedure shown below. Refer to the overall instrument troubleshooting section in the service introduction for details.The instrument UNLK diagnostics can be selected by pressing **[SHIFT] [EXT]** on the front panel. This will display the following:

OSC: REF M/N HET YO N2 N1

A YO unlock condition exists when the "YO" indicator is flashing.

In most cases, the error condition will occur in the CW/MANUAL mode, and the troubleshooting should be done in this mode first. If the YO loop will not phase-lock in CW/MANUAL at all frequencies, it will not function properly in the SWEPT mode.

To troubleshoot in the CW/MANUAL mode, perform the following steps. Refer to Figure D-5:

1. **Are Other Loops Locked?**

   Check to see that the UNLK indicators for the REF, M/N, N2, and N1 loops are not flashing. If these other loops are unlocked, the YO loop will not function correctly. Troubleshoot the other loops first. If they are all locked, proceed to question 2.

2. **Is Front Panel RF Power Correct?**

   Check that RF is present at the front panel at a level close to the selected power. If not, there is a problem in the RF path – go to question 14. If the front panel RF is present at the correct power, proceed to question 3.

3. Is YO Frequency Within ±25 MHz?

The correct YO frequency can be found by pressing **[SHIFT] [M2]** on the front panel that will display the following:

BAND # YO FREQUENCY (MHz)

Typically PRETUNE will tune the YO within ±5 MHz. YO tune can change the YO frequency by ±20 MHz (capture range of YO phase-locked feedback loop).

If the YO frequency offset is more than ±25 MHz, the offset is more than the YO TUNE can normally cause — go to question 17. If the YO offset is less that 25 MHz, the problem is most likely with YO TUNE — go to question 4.

4. Is YO TUNE at Maximum Positive or Negative? (Approximately ±6.9V)

This test must be made at a CW frequency that exhibits the UNLK error condition. The YO TUNE and FM COIL cables must remain connected so YO loop remains closed. Check the YO TUNE voltage at TP3 (TUNE) on the A55 YO driver. When the loop is operating properly, the YO TUNE voltage should be close to zero volts. If YO TUNE is within the range of approximately ±6.0 Vdc, the YO loop is locked and the UNLK indication is false — proceed to question 5. If YO TUNE is at maximum positive or negative (approximately ±6.9V), the YO loop is unlocked — go to question 6.

NOTE: In the CW/MANUAL mode, whenever the YO is locked, YO TUNE should be within the range of ±2 Vdc. If the actual magnitude is between 2 and 6 Vdc, proceed to question 5 and 6, and then return to question 4. If the actual magnitude of YO TUNE is greater than approximately 6.9V, suspect the A49 YO loop phase detector assembly.

5. Is HULY High?

If the YO loop is actually locked but HULY (high unlock YIG oscillator) is high indicating unlock, the unlocked detector on the A49 YO loop phase detector is at fault. If HULY is low, the problem is on the A59 digital interface assembly.

6. Is HLEY High?

HLEY (high lock enable YIG oscillator) must be high for the YO loop to lock. If HLEY is low or intermittent, suspect the A59 digital interface assembly. If not, proceed to question 7.

7. Is M/N Output Frequency and Power Correct?

Check for the proper M/N signal frequency and power at the output of A33J2. The correct frequency can be found by pressing **[SHIFT] [M1]** on the front panel. The following will be displayed:

M # N # M/N FREQUENCY (MHz) 20-30 FREQUENCY (MHz)

The correct M/N signal power is 0 dBm ±3 dB. If no signal is present or if the power and/or frequency is incorrect (at A33J2), troubleshoot the M/N Loop. If the M/N signal is correct, proceed to question 8.

8. Is 20-30 Output Frequency and Power Correct?

Check for the proper 20-30 signal frequency and power at the output of A36J2. The correct frequency can be found by pressing **[SHIFT] [M1]** on the front panel (see question 7 above). The correct power is 0 dBm ±3 dB. If no power is present or if the power and/or frequency is incorrect, troubleshoot the 20-30 loop. If the signal is correct, proceed to question 9.

9. Is the YO Frequency Change Porportional to YO TUNE?

Record the actual YO frequency. Disconnect YO TUNE and FM COIL DRIVE, cables A49J1 and A49J2. Place a 50Ω load on the YO TUNE cable, A49J2. (These cables will remain disconnected for the remainder of the troubleshooting.)

Note the YO frequency now and compare it with the value recorded before the cables were removed. It should have changed 10 MHz or less. The YO frequency sensitivity to YO TUNE is approximately −3.0 MHz/V. If the frequency does not change, or if it changes by more than 10 MHz, this indicates a problem on the A55 YO driver.

If the frequency change is proportional to the YO TUNE voltage, proceed to the next step.

10. Is the Open-Loop YO Frequency Accuracy ±5 MHz at 2.300 and 6.999 GHz?

With the YO TUNE and FM COIL cables disconnected (and a 50Ω load on the YO TUNE cable, A49J2), the YO frequency accuracy should be within a ±5 MHz window over the entire YO operating range. The YO accuracy should be checked at 2.300 and 6.999 GHz. If the actual YO frequency is outside of these limits, go to step 17; if not, proceed to step 11.

11. Is Sampler IF Frequency and Power Correct?

Check for the correct frequency and power for the SAMPLER IF. The frequency accuracy (open loop) should be ±5 MHz, the same as the YO. If the SAMPLER IF frequency and power are correct, suspect the A49 YO loop phase detector; if not correct, proceed to question 12.

12. Is RF Power into the A48 YO Loop Sampler Correct?

Check the RF signal power into the A48 YO loop sampler. If the RF power is correct, troubleshoot the A48 YO loop sampler. If no signal is present or if the power is incorrect, proceed to question 13.

13. Is Directional Coupler Power Output at A45J2 Correct?

Check the coupled-back RF power out of the A45 directional coupler at A45J2. If no signal is present or the power level is incorrect, replace the A45 directional coupler. If the RF power is correct, check the AT2 15 dB attenuator, the A46 7 GHz low pass filter, and connecting cables.

14. Is Directional Coupler Power Output at A45J3 Correct?

This portion of the troubleshooting guide is a branch from question 2.

Check the RF power out of the A45 directional coupler at A45J3. If the signal is present at the correct power (Refer to Figure D-6, 2 of 2), then a problem also exists in the main RF path (RF Section). To continue to troubleshoot the YO UNLK, however, go to question 3. If no signal is present or if the power output is low, proceed to question 15.

15. Is YO Power Output Correct?

Check the RF power out of the YO. If the power is correct (Refer to Figure D-6, 2 of 2), troubleshoot the A45 directional coupler. If no signal is present or if the power is low, proceed to question 16.

16. Is the YO Main Coil Drive Correct?

Check the YO MAIN COIL DRIVE. This can be done by testing the SENSE voltage, TP4 on the A55 YO driver assembly. (The SENSE voltage is related to the YO frequency by −2.4 V/GHz.) If the YO main coil is greatly mistuned, no YO signal will be present. If the SENSE voltage (hence the YO MAIN COIL DRIVE current) is correct to within ±1V, troubleshoot the YO; if not, proceed to question 17.

17. Is the PRETUNE Voltage Correct?

This portion of the troubleshooting guide is a branch from question 3, question 10, and question 16.

Check the PRETUNE voltage. PRETUNE has a sensitivity of −2.5 V/GHz of YO frequency. If the PRETUNE voltage is correct, troubleshoot the A55 YO driver (OFFSET and GAIN) and the A47 sense resistor assembly. If PRETUNE is not correct, proceed to question 18.

18. Is the VSWP Voltage Correct?

Check that the VSWP voltage is zero volts. If it is correct, suspect the A54 YO pretune/delay compensation assembly. If VSWP is much different than zero volts, proceed to question 19.

19. Is LVSX Low?

If the VSWP voltage is much different than zero volts, it will affect the PRETUNE voltage only if the A54 YO pretune/delay compensation assembly is also not operating correctly. If LVSX (low voltage sweep disable) is high or intermittent, troubleshoot the A59 digital interface assembly (in the controller section). If LVSX is low (that should be the case for CW/MANUAL), the trouble is in the A54 YO pretune/delay compensation assembly. In either case, also troubleshoot VSWP on the A58 sweep generator assembly.

YO UNLK – SWEPT MODE

To troubleshoot in the swept mode with the YO unlocked, perform the following steps:

1. Is CW/MANUAL Mode Correct?

If the YO UNLK error condition can be made to occur in the CW/MANUAL mode, go to the YO UNLK – CW/MANUAL troubleshooting section. It will also be helpful if the YO UNLK condition can be made to occur in the SINGLE SWEEP mode, for this will hold the YO loop (error) condition constant while troubleshooting.

If the error condition can only be made to occur in the SWEPT mode and CONTINUOUS SWEEP mode, the problem will be more difficult to solve. Proceed to question 2 in this section. There are several malfunctions that could cause a YO loop unlock in only the swept mode – these relate to the function and operation of VSWP, LKICK, HLEY (high lock enable YIG oscillator), and possibly VCOMP, LVSX, and LYSP. Most of the potential causes of the error are related to timing, mainly at the start of sweep.

2. Is VSWP Correct?

Check to see that VSWP (A58TP10) is at zero volts at the start of each sweep. LVSX (low voltage sweep disable) is high in swept mode for sweep widths >500 kHz, but low in CW/MANUAL. Thus, any offset in VSWP would only affect the YO tuning in the SWEPT mode. Because of the high sensitivity of the YO frequency to VSWP (500 MHz/V), an offset of as little as 50 mV added from VSWP to PRETUNE will result in the YO being tuned outside of the capture range of the YO phase locked loop. If VSWP is zero, proceed to question 3. If VSWP is not zero, suspect the A58 sweep generator.

3. Is the YO Kick Pulse Correct?

Make sure the YO kick pulse is being generated on the A55 YO driver.

a. Check the LKICK signal by placing the channel A probe of an oscilloscope on A55P1-1. A TTL low-going signal should be seen. If LKICK is present, suspect a failure on the A55 YO driver.

   If LKICK is not present, or does not drop below 2 volts when active, check LKICK at A54TP2. If the signal is good at A54TP2, suspect a motherboard or connector problem. If the signal at A54TP2 is bad, suspect the A54 assembly.

4. Is HLEY High at Start of Sweep?

Check the HLEY (high lock enable YIG oscillator, A50TP5) voltage at the start of sweep. If it is low or intermittent, the YO loop will not lock – suspect the A59 digital interface assembly.

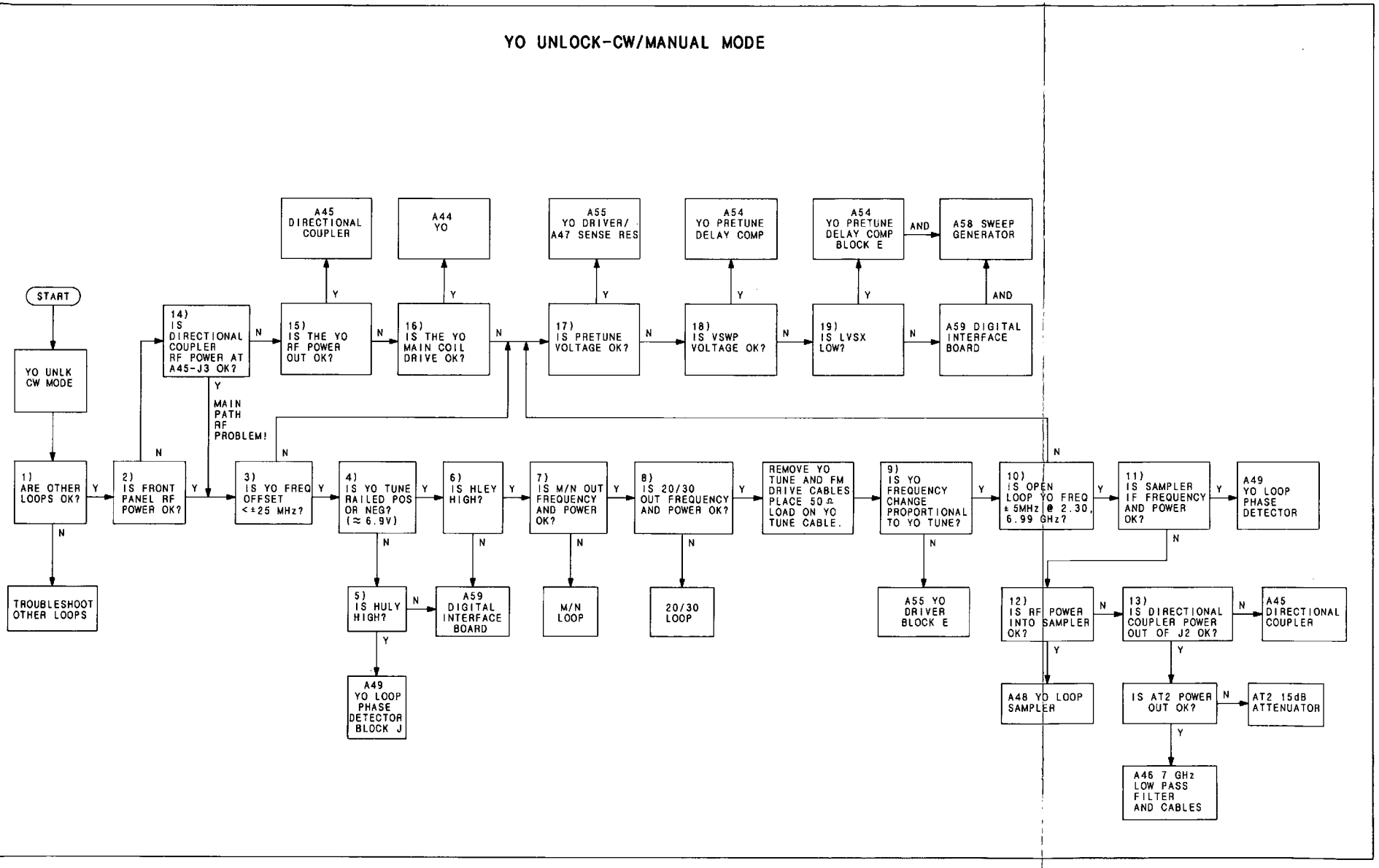


Figure D-5. YO Loop Troubleshooting Flowchart (1 of 2)

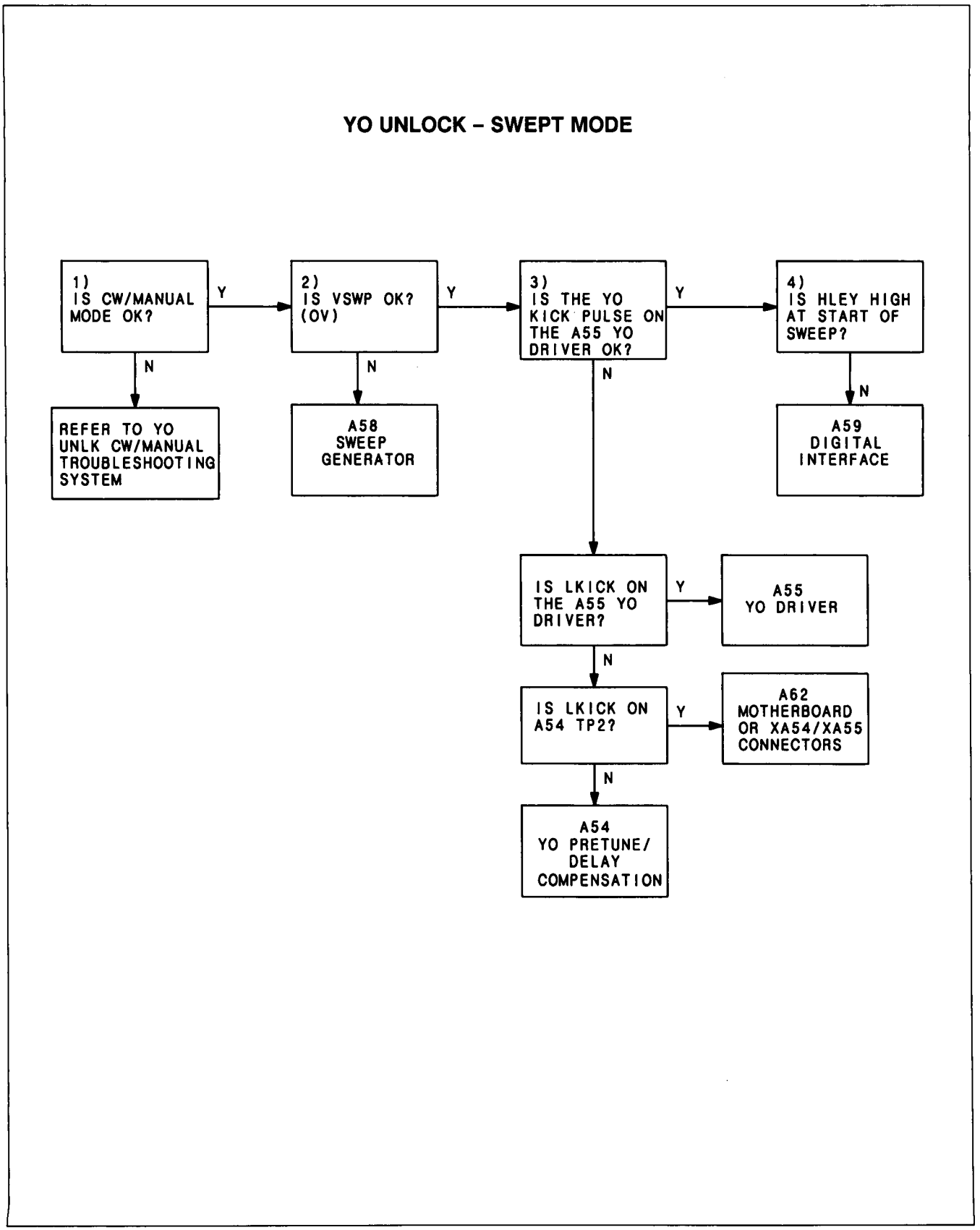


Figure D-5. YO Loop Troubleshooting Flowchart (2 of 2)

Sweep Generator
Assembly-Level Troubleshooting

INTRODUCTION

There are two basic failure modes that have to do with the sweep function of the instrument.

- The instrument is not sweeping.
- The instrument is sweeping, but the sweep is incorrect – the frequency limits of the sweep are wrong and/or bandcrossings are not occurring.

The first task is to get the instrument to do repetitive sweeps of any kind.

If the MARKER RAMP (A58 TP4) is sweeping zero to ten volts and the front panel sweep LED is blinking, the instrument is considered to be sweeping even though the output frequency may not be moving. If, on the other hand, MARKER RAMP is stuck and the front panel sweep LED is continuously on or off, the instrument is not considered to be sweeping. When looking at the LED, care must be taken because in fast sweeps it may appear to be on all the time, even though it is actually blinking.

NO SWEEP

Assuming that the instrument processor is functioning correctly, the only external lines that can prevent the A58 sweep generator from sweeping are HSP (high sweep, A58P1-13), LBX (low bandcross, A58TP6) and LRSP (low reset sweep, A58TP11). HSP and LRSP are standard TTL lines with HSP being driven by the A57 marker/bandcross assembly and LRSP being driven by the A59 digital interface assembly. LBX is an open collector line that can be driven by both the A58 sweep generator and A57 marker/bandcross boards. HSP is coupled to LBX on the A57 marker/bandcross assembly so that if LBX is pulled down, the A57 marker/bandcross assembly pulls down on HSP also.

If the instrument is in the continuous sweep mode and is not sweeping, remove the A57 marker/bandcross assembly. If the instrument now sweeps, the problem is most likely on the A57 marker/bandcross assembly (in the controller section). Note that in this mode, the frequency limits that the instrument is sweeping over will not be correct. This is because it is the A58 sweep generator that is pulling LBX low to stop the sweep when the MARKER RAMP reaches 12 volts.

If the instrument still will not sweep with the A57 marker/bandcross assembly removed, place the A58 assembly on an extender board and check the state of the HSP line, A58P1-13. Since only the A57 marker/bandcross assembly can pull down on this line, it should be high in this mode. If it is low, troubleshoot this problem. If HSP is high, check the state of LBX (A585TP6). If it is low, determine what is pulling it low by looking at HBX (A58TP5). If HBX is high, the A58 sweep generator is faulty, and is pulling down on LBX. If HBX is low, troubleshoot the A59 digital interface (in the Controller Section).

Finally, look at LRSP, A58TP11. If it is stuck low, check it at its source – the A59 digital interface assembly.

If the three lines just discussed, LBX, HSP and LRSP are all high, the problem is indeed on the sweep generator assembly. Reinstall the marker/bandcross assembly. Replace the A58 sweep generator assembly or consult the A58 troubleshooting section in the optional *Component Level Service Manual* set if component level repair is intended.

INCORRECT SWEEP

If the instrument sweeps, as defined above, but the YO does not sweep or the frequency limits are incorrect, check the two sweep ramps from the A58 sweep generator assembly, 20-30 SWP (TP8) and VSWP (TP10). The sensitivities of these lines are discussed below.

YO sweeps widths >5 MHz are derived from VSWP. Note that the instrument sweep width, delta F, is related to the YO sweep width by the harmonic number of the band being used. For example, if the instrument is sweeping from 8 to 10 GHz, the instrument sweep width is 2 GHz. However; this is the second harmonic of the YO − the YO is actually sweeping from 4 to 5 GHz; a sweep width of 1 GHz. The sensitivity of VSWP is +2 volts/GHz of YO sweep width. In the example above, VSWP should be a ramp starting at zero and going to +2 volts.

If VSWP is correct, look at PRETUNE (TP3) on the A54 pretune/delay compensation assembly. It has a sensitivity of −2.5 volts/GHz of YO frequency. In the foregoing example where the YO swept from 4 to 5 GHz, PRETUNE should go from −10 to −12.5 volts.

If PRETUNE is correct, look at SENSE (TP4) on the A55 YO driver assembly. This point has a sensitivity of about −2.34 volts/GHz of YO frequency. If this is correct, the problem is most likely in the A44 YIG oscillator assembly.

YO sweep widths ≤5 MHz are derived from 20-30 SWP. The sensitivity of 20-30 SWP is related to YO sweep width but changes depending upon the particular sweep width selected, as shown in Table D-2.

Table D-2. Sensitivity of 20-30 SWP Line

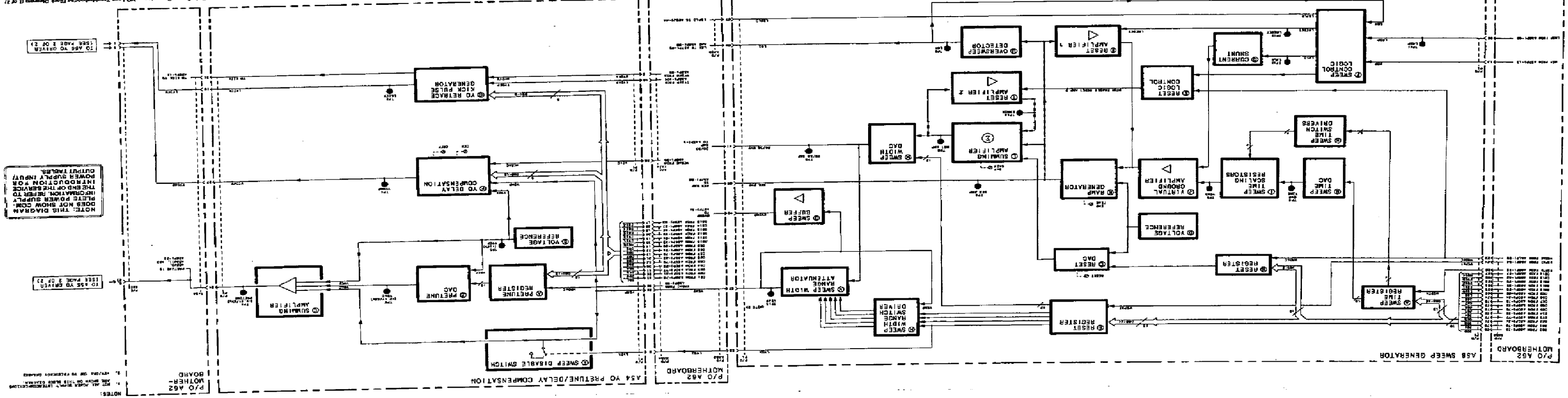
Sweep Width	Sensitivity
5 MHz ≥ YO sweep width > 500 KHz	500 KHz/volt
500 KHz ≥ YO sweep width > 100 KHz	50 KHz/volt
100 KHz ≥ YO sweep width > 10 KHz	10 KHz/volt
10 KHz ≥ YO sweep width > 1 KHz	1 KHz/volt
5 KHz ≥ YO sweep width > 500 Hz	500 Hz/volt
500 Hz ≥ YO sweep width > 100 Hz	50 Hz/volt

Verify that VSWP is not sweeping more than 0.0 to 15.0 mV and that 20-30 SWP is correct. If both of these are correct, the problem is most likely in the 20-30 loop.

A23 FM Driver
Assembly-Level Troubleshooting

Perform the FM accuracy and flatness test (4-16) in Section 4, Performance Tests, located in the *Calibration Manual*. If required, perform the FM accuracy and FM overmod adjustment (5-9) in Section 5, Adjustments, located in the *Calibration Manual*.

If the FM driver does not pass the performance test, perform the adjustment procedure. If it does not pass the performance test after being adjusted, repair or replace the assembly.



RF scale Opcns 003

Figure D-8. Sweep Generator — YO Loop Troubleshooting Block Diagram (1 of 3)
Sweep Generator - YO Loop Assembly-Level Troubleshooting D-27/D-28

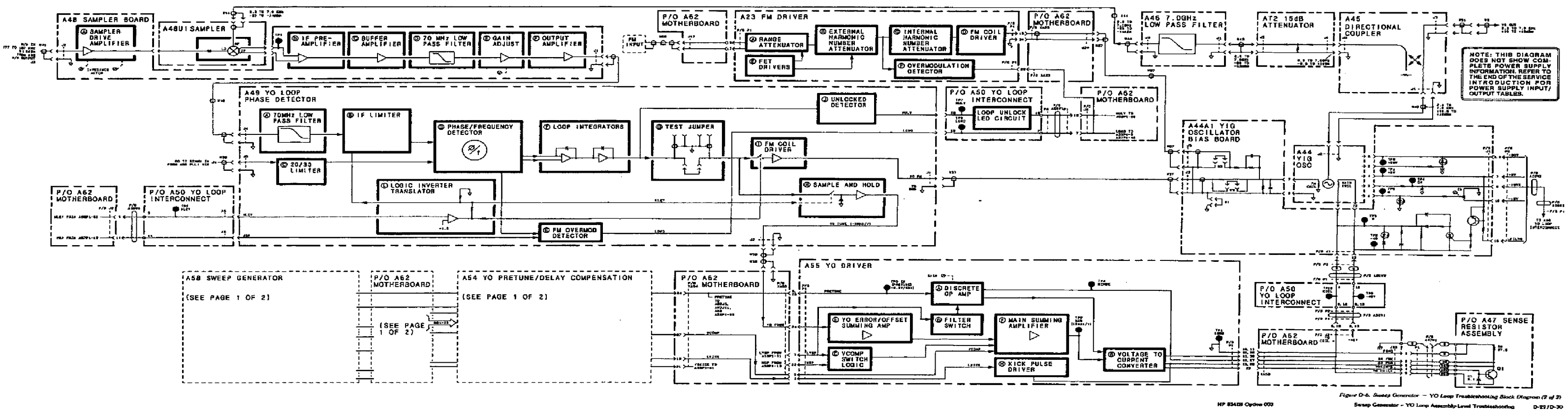


Figure D-6. Sweep Generator — YO Loop Troubleshooting Block Diagram (2 of 2)

TOP VIEW

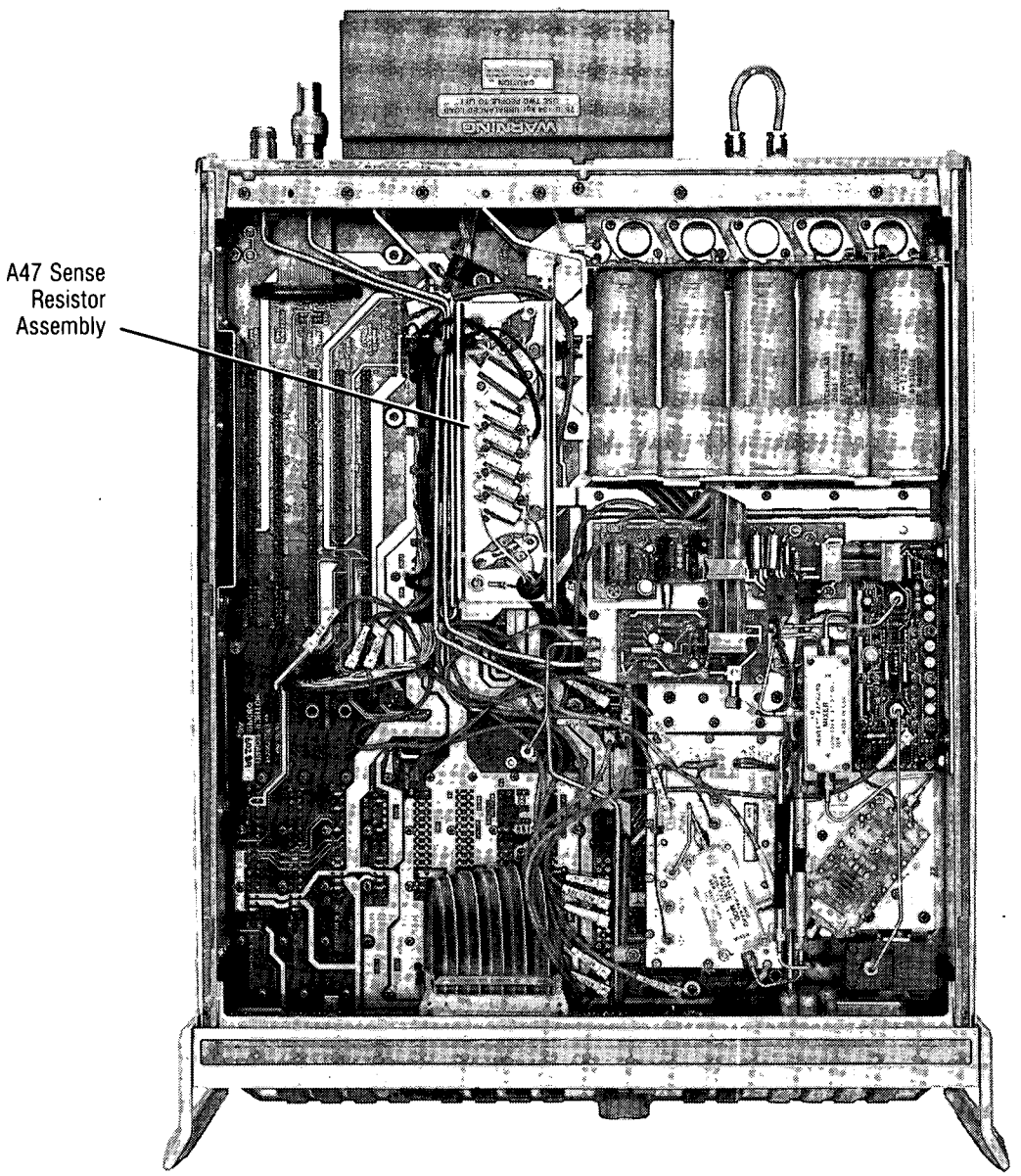


Figure D-7. Sweep Generator — YO Loop Major Assemblies Location (1 of 5)

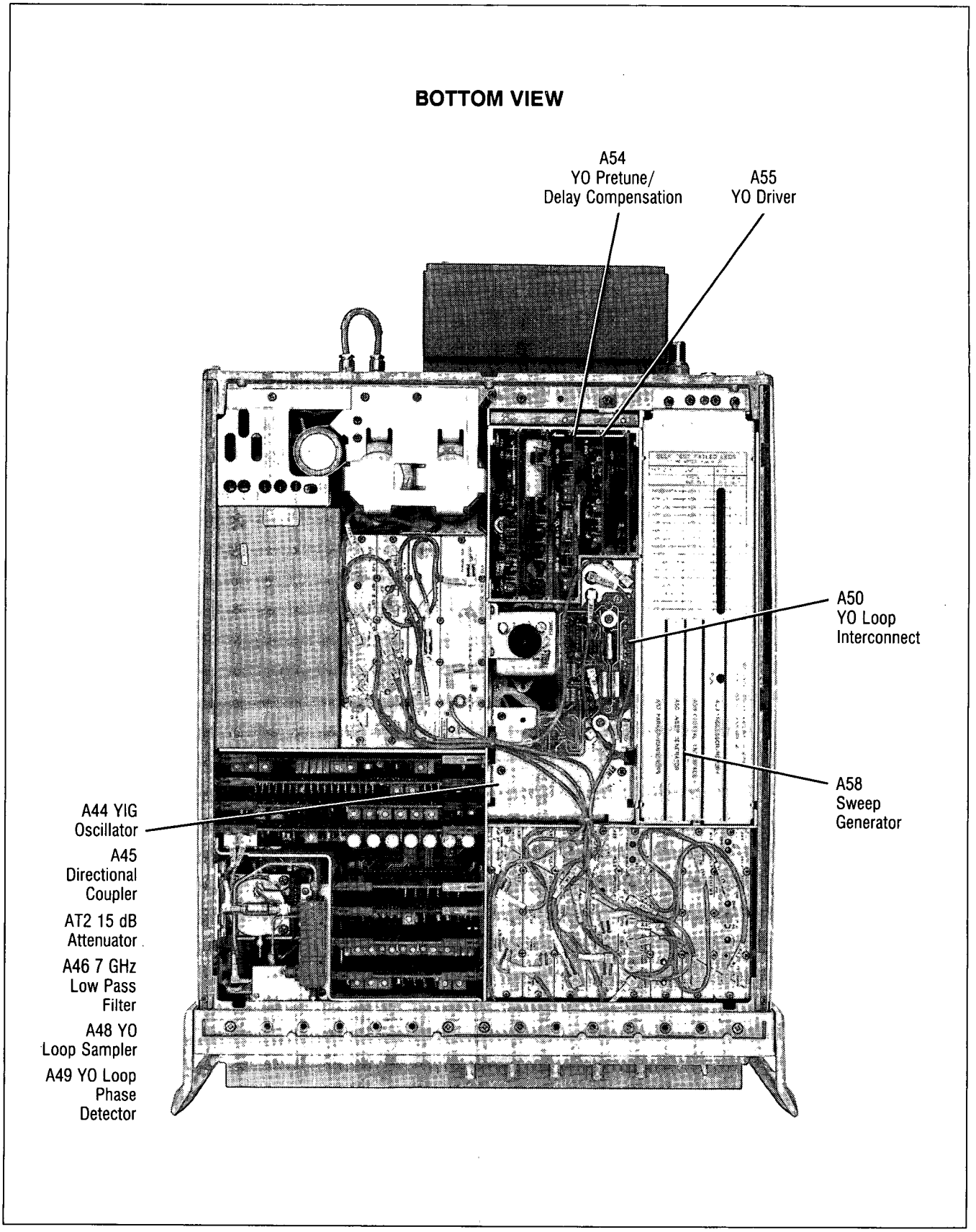
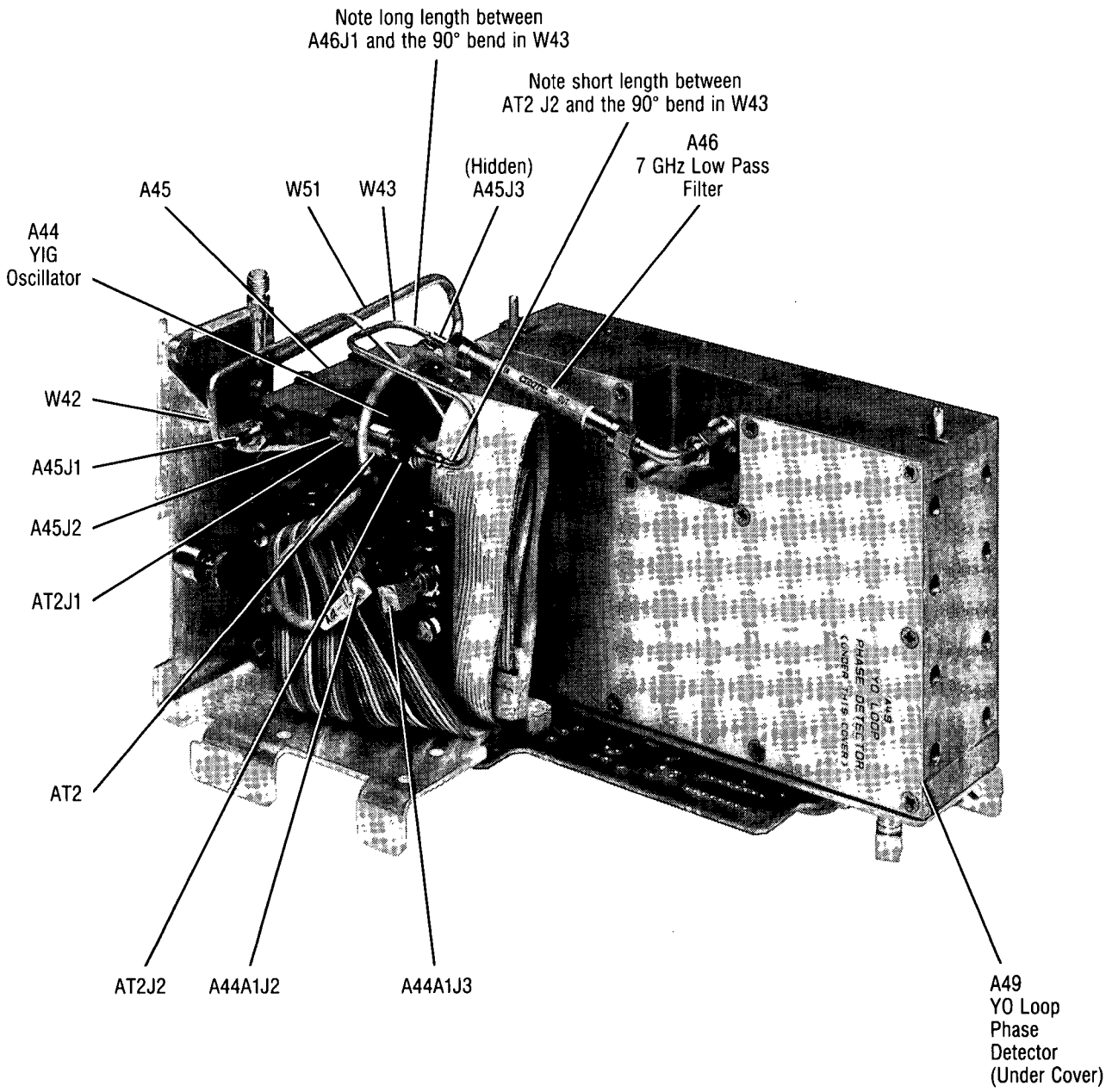


Figure D-7. Sweep Generator — YO Loop Major Assemblies Location (2 of 5)



CAUTION: W51 Must be disengaged from W3 before removing the YO Loop from the instrument or damage to these cables will result. Refer to Figure D-8.

Figure D-7. Sweep Generator — YO Loop Major Assemblies Location (3 of 5)

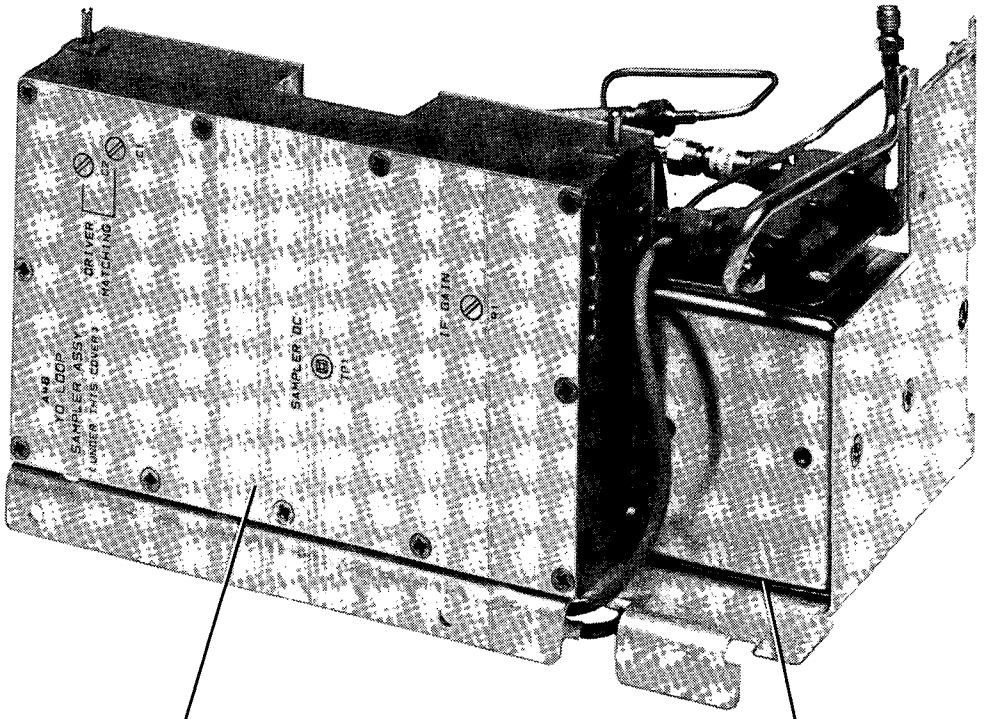


Figure D-7. Sweep Generator — YO Loop Major Assemblies Location (4 of 5)

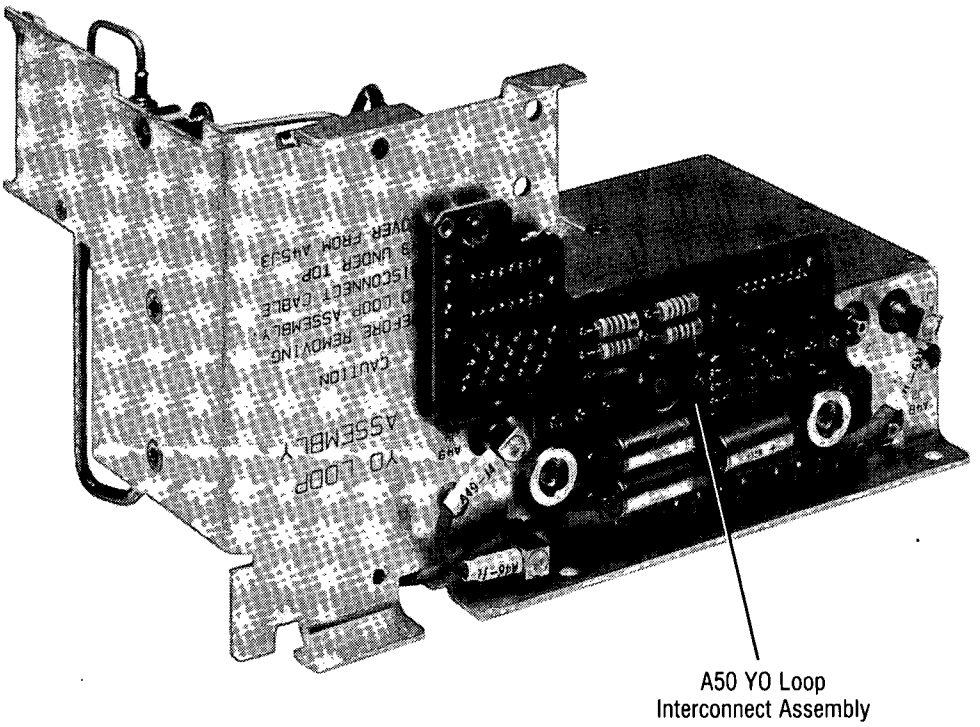


Figure D-7. Sweep Generator — YO Loop Major Assemblies Location (5 of 5)

Sweep Generator – YO Loop Repair Procedures

PLACING THE YO ASSEMBLY INTO THE SERVICE POSITION

Equipment Required

Pozidrive screwdriver
1/4 inch open end wrench
5/16 inch open end wrench

Procedure

1. Remove the top and bottom covers from the instrument. Place the instrument so that it is in its normal operating position. Refer to Figure D-8, W3 Connection.

2. Using the two wrenches listed above, disengage W3 from the cable coming from the other side of the motherboard.

CAUTION

It is critical that step 2 be performed before proceeding or damage to the instrument will result.

3. Turn the instrument upside-down. Refer to Figure D-9, YO Loop Removal. Remove the cables going to A49J2 and A49J3. Remove the three screws shown as item 1. Remove the screw shown as item 2. Item 1 screws are different from the item 2 screws, keep them separate.

4. Refer to Figure D-10, YO Loop in Service Position, before proceeding. Gently pull on the YO loop while moving it from side-to-side. Do not use excessive force. Remove the YO loop assembly and hold it upright. Set the retaining tabs over the adjacent aluminum divider. The locking screw can now be engaged to hold the YO loop securely in place. Replace the cables going to A49J2 and A49J3.

CAUTION

When replacing the YO loop assembly, be careful not to smash the ribbon connector, A50W1.

5. To reinstall the YO loop, reverse the above procedure.

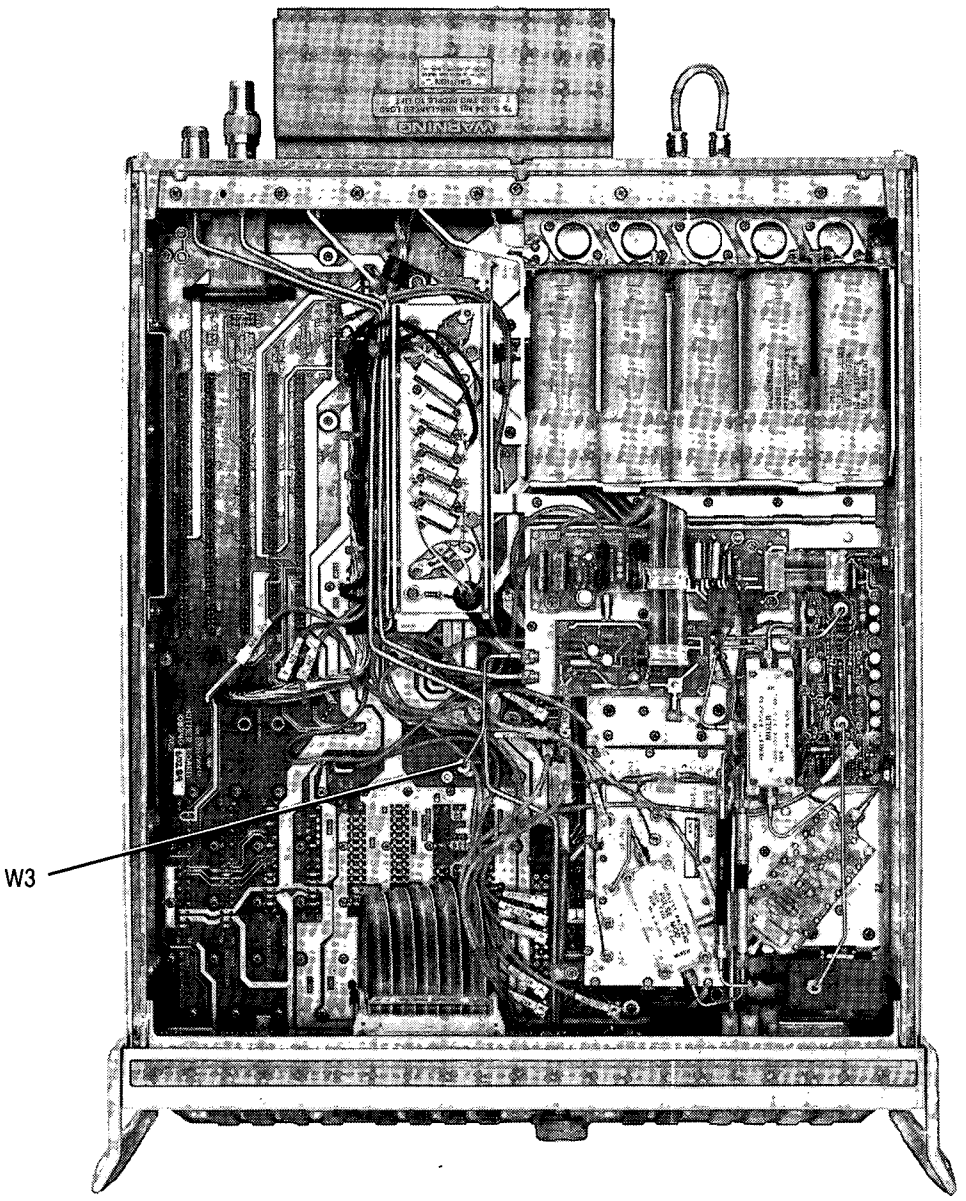


Figure D-8. W3 Connection

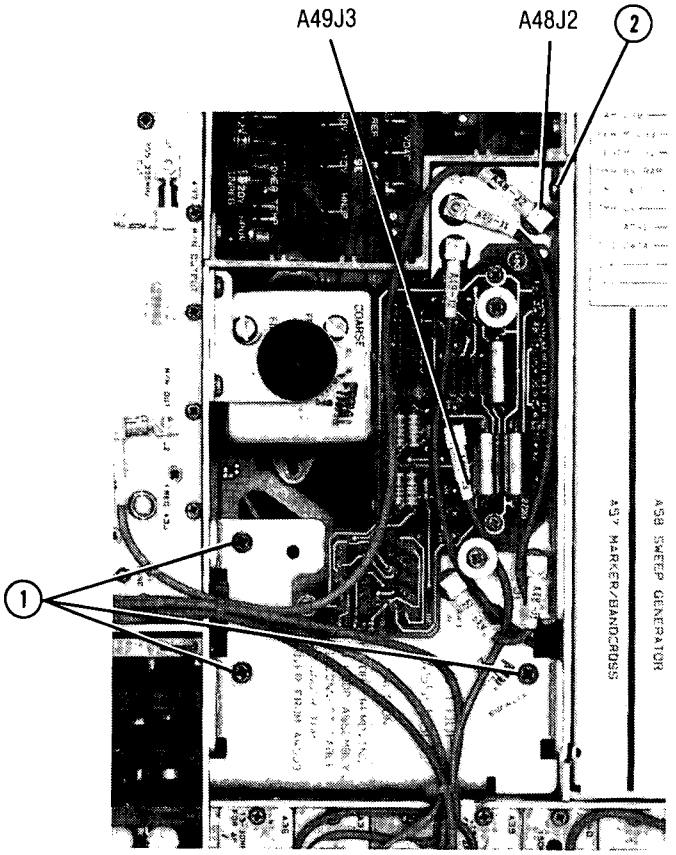


Figure D-9. YO Loop Removal

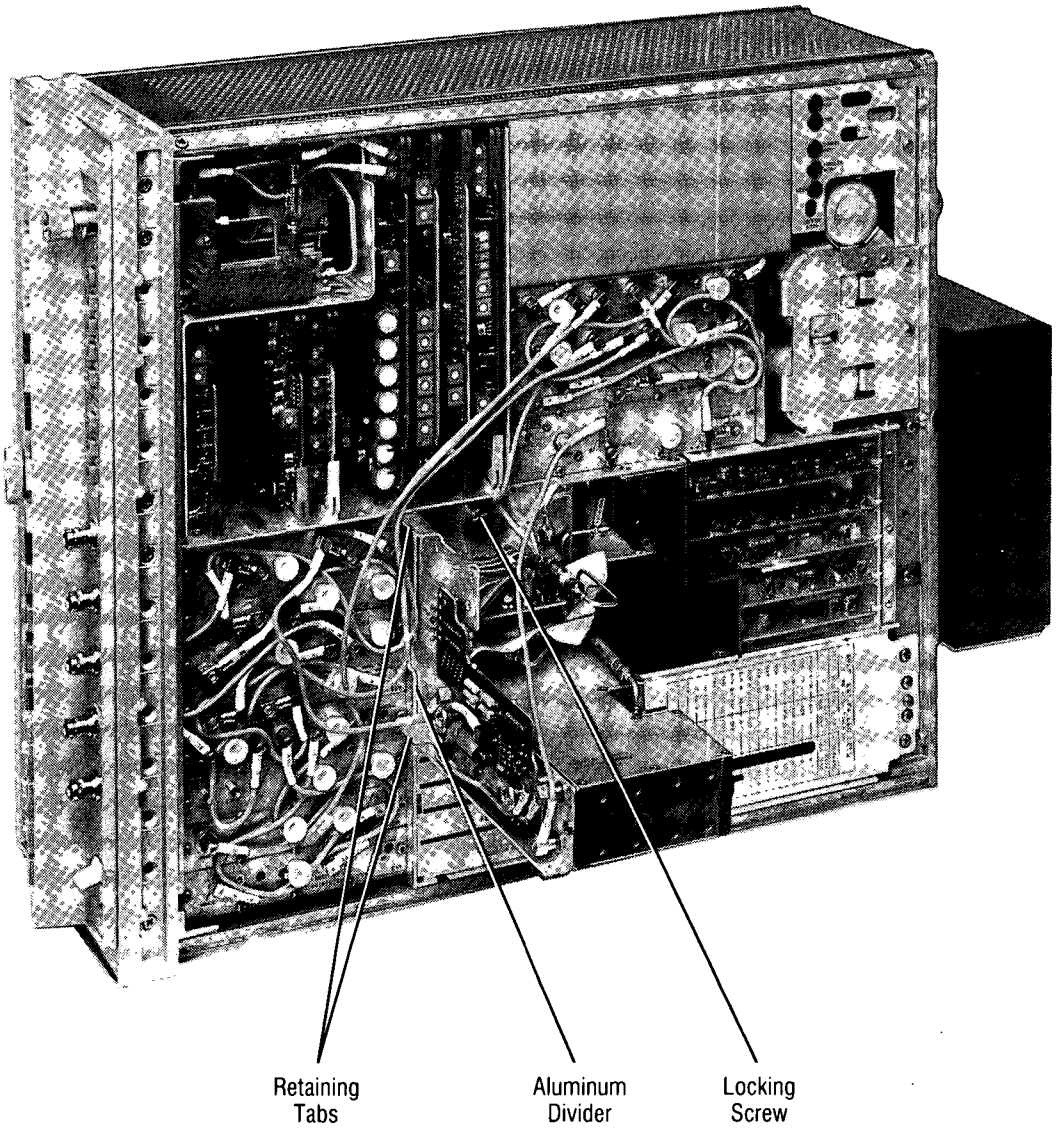


Figure D-10. YO Loop in Service Position

Table D-3. Sweep Generator — YO Loop Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
				SWEEP GENERATOR - YO LOOP		
A23	08340-60222	7	1	FM DRIVER ASSEMBLY	28480	08340-60222
A44/A44A1	5086-7430	1	1	NEW YIG OSCILLATOR 2.3 TO 7.0 GHz (Includes A44 YO microcircuit and A44A1 bias assembly, which are not separately replaceable.)	28480	5086-7430
	5086-6430	9		EXCHANGE YIG OSCILLATOR 2.3 TO 7.0 GHz (Includes Exchange YO microcircuit and A44A1 bias assembly, which are not separately replaceable.)	28480	5086-6430
A45	0955-0098	9	1	DIRECTIONAL COUPLER	28480	0955-0098
A46	9135-0165	4	1	7 GHz LOW PASS FILTER	28480	9135-0165
A47	08340-60094	1	1	SENSE RESISTOR ASSEMBLY	28480	08340-60094
A48/A49	08340-60260	3		A48 SAMPLER/A49 PHASE DETECTOR ASSEMBLY (Includes A48, A49, and housing, which are not separately replaceable.)	28480	08340-60260
A50	08340-60219	2	1	YO LOOP INTERCONNECT	28480	08340-60219
A54	08340-60217	0	1	YO PRETUNE/DELAY COMPENSATION ASSEMBLY	28480	08340-60217
A55	08340-60215	8	1	YO DRIVER ASSEMBLY	28480	08340-60215
A58	08340-60154	4	1	SWEEP GENERATOR ASSEMBLY	28480	08340-60154
				YO LOOP SECTION ATTACHING HARDWARE		
1	0360-0452	0	2	TERMINAL-SLDR LUG PL-MTG FOR-fi10-SCR	28480	0360-0452
2	0520-0164	1	2	SCREW-MACH 2-56 .25-IN-LG 82 DEG	00000	ORDER BY DESCRIPTION
3	1250-0258	2	2	A49J1,J2 CONNECTOR-RF MALE SMB	28480	1250-0258
4	1250-0691	7	4	A49J3,J4 A48J1,2- CONNECTOR-RF MALE SMB	28480	1250-0691
5	2190-0124	4	2	WASHER-LK INTL T NO. 10 .195-IN-ID	28480	2190-0124
6	2200-0103	2	13	SCREW-MACH 4-40 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
7	2200-0147	4	2	SCREW-MACH 4-40 .5-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
8	2200-0165	6	23	SCREW-MACH 4-40 .25-IN-LG 82 DEG	00000	ORDER BY DESCRIPTION
9	2360-0331	6	4	SCREW-MACH 6-32 .25-IN-LG PANHD POZI	28480	2360-0331
10	2360-0333	8	2	SCREW-MACH-6-32 .25-IN-LG 100 DEG	28480	2360-0333
11	2950-0078	9	2	NUT-HEX-DBL-CHAM 10-32-THD .067-IN-THK	28480	2950-0078
12	3050-0105	6	2	WASHER-FL MTLC NO. 4 .125-IN-ID	28480	3050-0105
13	3050-0907	6	4	WASHER-SHLDR NO. 10 .194-IN-ID	28480	3050-0907
14	08340-00075	2	1	DECK-YO LOOP	28480	08340-00075
15	08340-00049	0	1	COVER-SAMPLER	28480	08340-00049
16	08340-00050	3	1	COVER-PHASE LOCK	28480	08340-00050
17	08340-20204	1	1	HOUSING-YT P/L	28480	08340-20204
18	85660-20088	8	2	STUD-YTO LOOP	28480	85660-20088
19	85660-20100	5	2	EXTRACTOR	28480	85660-20100
20	86701-00054	8	1	SPACER-SAMPLER	28480	86701-00054
21	2190-0003	8	2	WASHER-LK HLCL NO. 4 .115-IN-ID	28480	2190-0003
22	1250-1142	5	1	WASHER-LK INTL T 1/2 IN .26-IN-ID	28480	1250-1142
23	1250-1143	6	1	NUT-RF CONNECTOR-SERIES SM A	28480	1250-1143

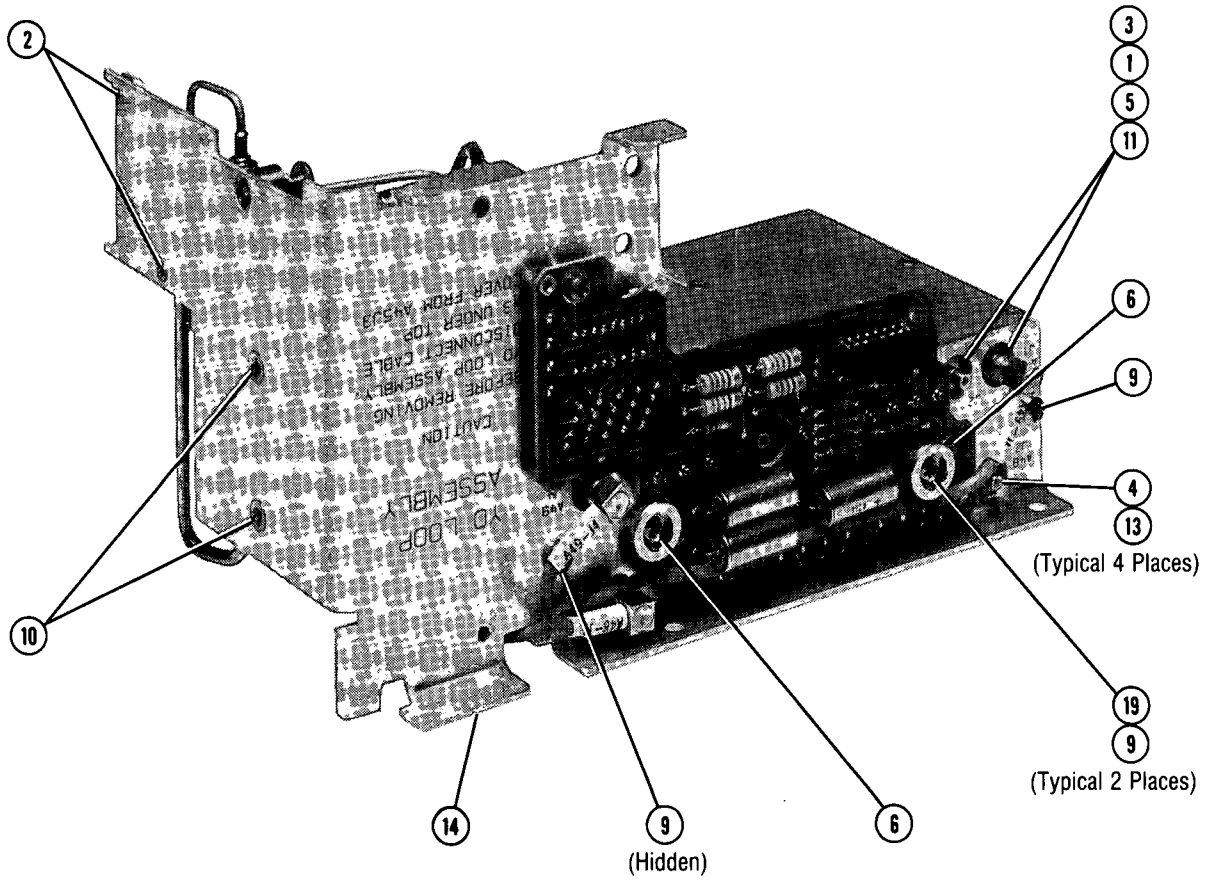


Figure D-11. YO Loop Attaching Hardware (1 of 3)

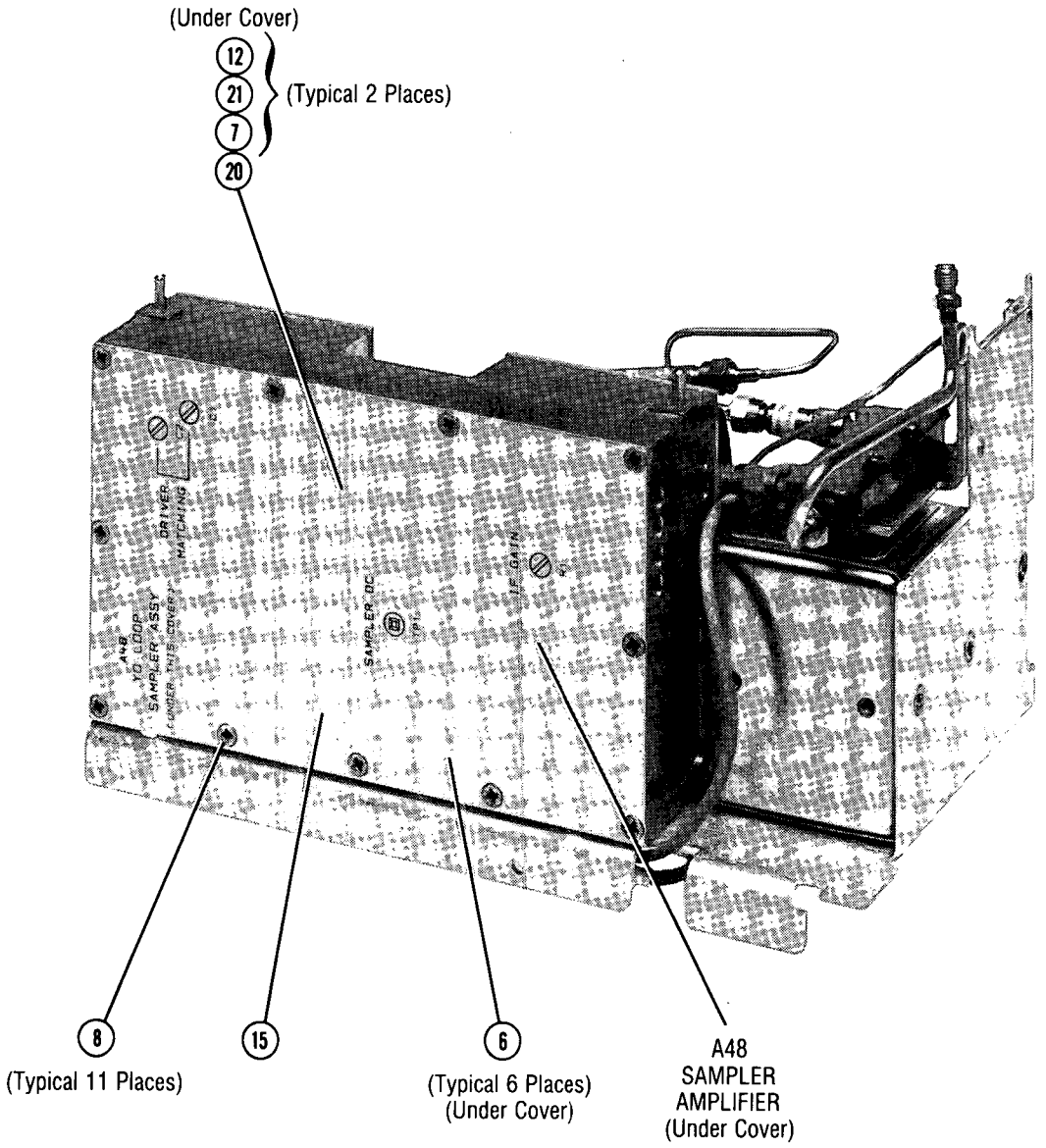
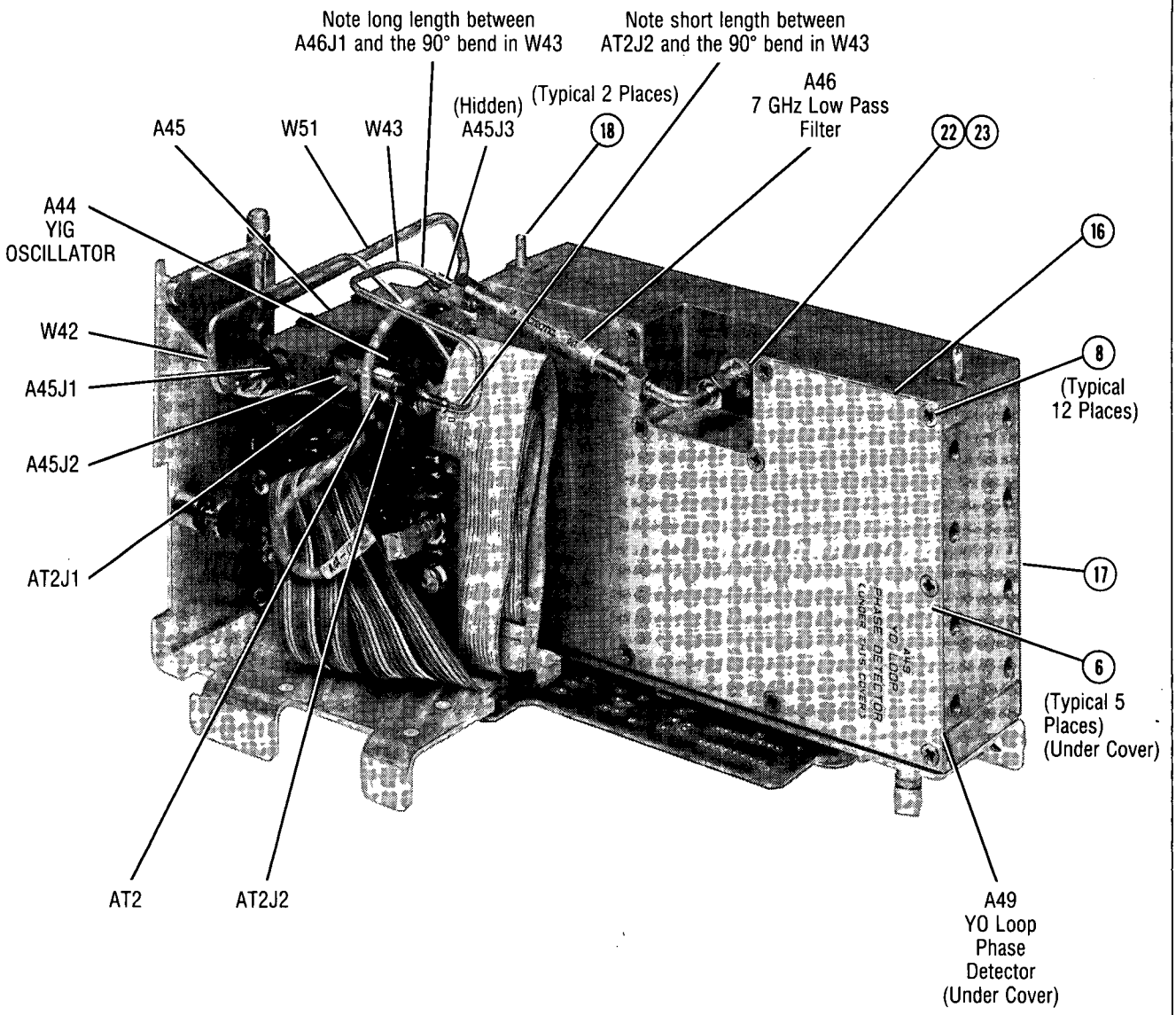


Figure D-11. YO Loop Attaching Hardware (2 of 3)



CAUTION: W51 must be disengaged from W3 before removing the YO Loop from the instrument or damage to these cables will result. W3 is attached to W51on the top side of the instrument.

Figure D-11. YO Loop Attaching Hardware (3 of 3)

Motherboard and Wiring List
Assembly-Level Service

CONTENTS

A62 Motherboard
Overall Description

ASSEMBLY PURPOSE

The A62 motherboard is the common board to which many other assemblies are connected and serves to route signals between these assemblies. The A62 motherboard also routes signal to and from the front/rear panel connectors.

GROUNDS

The A62 motherboard has several different grounds:

- **STAR GND** – is the single ground reference point for analog circuitry in all major assemblies. Each assembly block is referenced to STAR GND via individual traces, minimizing ground noise crosstalk between major assemblies. STAR GND is a screw terminal located between the A62XA57 marker bandcross connector and A62J3 connector and is visible with the instrument top cover removed.
- **GND** – designates individual analog ground traces connecting major assembly blocks to STAR GND. Many of these traces are physically large and are used for high current power supply applications.
- **GND PLANE** – Refer to Figure E-1.

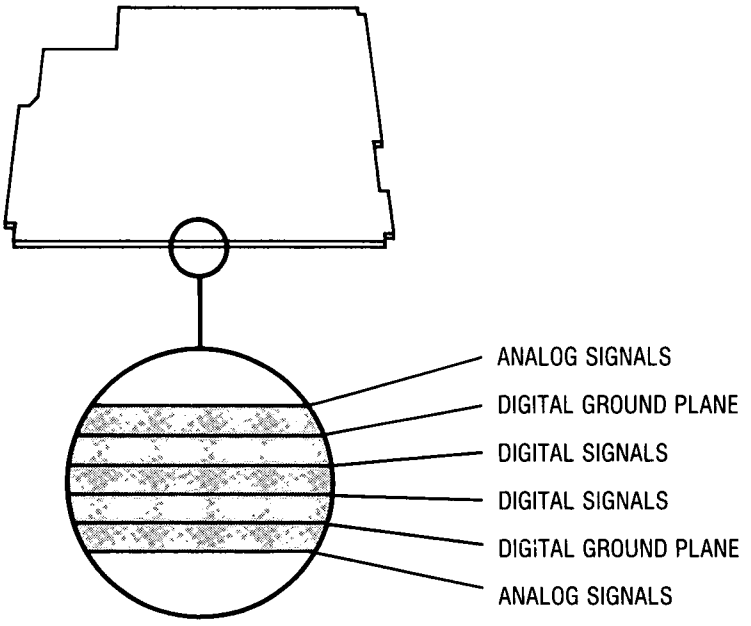


Figure E-1. A62 Motherboard Cross Section

As shown in Figure E-1, analog and digital trace layers are separated by ground plane layers. These layers were designed to disperse any digital noise into the ground planes and act as an electrostatic shield between the digital and analog signal traces. The ground planes extend to each edge of the motherboard and are connected to STAR GND. This provides isolation between analog and digital grounds while reducing signal crosstalk.

- **REFERENCE GND** – is connected to STAR GND and is used as a very stable low current reference for integrated circuits and cable shields.
- **MISCELLANEOUS GROUND PLANES:**

  A. The ground plane under the 20/30 Loops' aluminum casting completes a radio frequency interference (RFI) "box" comprised of the casting, assembly covers, and the 20/30 loops' ground plane. This ground plane is connected to STAR GND via a GND trace, and to chassis GND through the aluminum casting.

  B. A ground plane under the M/N Loop's aluminum casting connects to STAR GND and is used as an RFI shield.

- **CHASSIS GND** – All grounds and ground planes are mechanically secured to the chassis (CHASSIS GND) around the instrument's perimeter and to various other parts of the A62 motherboard.

MOTHERBOARD REPLACEMENT

The A62 motherboard is not customer/field replaceable. Direct any questions concerning motherboard replacement to your nearest HP service center for more specific instructions. Refer to the HP service center listing at the end of this manual.

Motherboard Wiring List
Introduction

This table lists all signals that are routed on the A62 motherboard assembly. Signals that exist only on other assemblies are not shown. To locate these, refer to the pin I/O tables and schematic diagrams of the respective assemblies.

The A62 motherboard wiring list is arranged so that signal mnemonic, description, type, and level information is on the left-hand page, and the source and destination information is on the right-hand page. All mnemonics are in alphabetical order, with power supplies listed at the end of the table.

Unless otherwise stated, all XA connector pins are assumed to be part of their respective connector. For example, XA58P1-38 is written XA58-38 for simplicity, with P1 assumed.

Table E-1. Motherboard Wiring List

Mnemonic	Description	Type	Levels
ADR0	INSTRUMENT I/O ADDRESS BUS BIT 0	DIGITAL	TTL
ADR1	INSTRUMENT I/O ADDRESS BUS BIT 1	DIGITAL	TTL
ADR2	INSTRUMENT I/O ADDRESS BUS BIT 2	DIGITAL	TTL
ADR3	INSTRUMENT I/O ADDRESS BUS BIT 3	DIGITAL	TTL
ADR4	INSTRUMENT I/O ADDRESS BUS BIT 4	DIGITAL	TTL
AM IN	AMPLITUDE MODULATION INPUT	ANALOG	±1V MAX.
AM RTN	AMPLITUDE MODULATION GROUND RETURN	GROUND	0V
ATN	IEEE 488 ATTENTION (ATN)	DIGITAL	TTL
ATNAT1	ATTENUATOR ATTENUATION CARD 1	DIGITAL	OPEN COLLECTOR
ATNAT2	ATTENUATOR ATTENUATION CARD 2	DIGITAL	OPEN COLLECTOR
ATNAT3	ATTENUATOR ATTENUATION CARD 3	DIGITAL	OPEN COLLECTOR
ATNAT4	ATTENUATOR ATTENUATION CARD 4	DIGITAL	OPEN COLLECTOR
ATN COIL +	ATTENUATOR SOLENOID COILS SUPPLY	POWER SUPPLY	+5V
ATNTH1	ATTENUATOR THROUGH CARD 1	DIGITAL	OPEN COLLECTOR
ATNTH2	ATTENUATOR THROUGH CARD 2	DIGITAL	OPEN COLLECTOR
ATNTH3	ATTENUATOR THROUGH CARD 3	DIGITAL	OPEN COLLECTOR
ATNTH4	ATTENUATOR THROUGH CARD 4	DIGITAL	OPEN COLLECTOR
BIAS S/H PULSE	BIAS SAMPLE AND HOLD PULSE	DIGITAL	TTL
BVSWP	BUFFERED 0 TO 10V SWEEP RAMP	ANALOG	10V/SWEEP
DAV	IEEE 488 DATA VALID (DAV)	DIGITAL	TTL
DB0	INSTRUMENT I/O DATA BUS BIT 0	DIGITAL	TTL
DB1	INSTRUMENT I/O DATA BUS BIT 1	DIGITAL	TTL
DB2	INSTRUMENT I/O DATA BUS BIT 2	DIGITAL	TTL
DB3	INSTRUMENT I/O DATA BUS BIT 3	DIGITAL	TTL
DB4	INSTRUMENT I/O DATA BUS BIT 4	DIGITAL	TTL
DB5	INSTRUMENT I/O DATA BUS BIT 5	DIGITAL	TTL

Table E-1. Motherboard Wiring List

Mnemonic	Source	Destination
ADR0	XA60-17	XA27-9, XA57-17, XA58-17, XA59-17, A62J1-23
ADR1	XA60-73	XA27-40, XA57-73, XA58-73, XA59-73, A62J1-24
ADR2	XA60-18	XA27-10, XA57-18, XA58-18, XA59-18, A62J1-25
ADR3	XA60-74	XA27-41, XA57-74, XA58-74, XA59-74, A62J1-26
ADR4	XA60-19	XA27-11, XA57-19, XA58-19, XA59-19, A62J1-27
AM IN	A62J15 CENTER	XA26-19
AM RTN	A62J15 SHIELD[a]	XA26-41, A62 SMC SHIELD AND GUARD TRACE AROUND AM IN
ATN	XA60-8	A62J7-21
ATNAT1	XA24-30	A62J20-2
ATNAT2	XA24-29	A62J20-9
ATNAT3	XA24-28	A62J20-5
ATNAT4	XA24-27	A62J20-10
ATN COIL+	XA24-7	A62J20-6
ATNTH1	XA24-12	A62J20-13
ATNTH2	XA24-11	A62J20-3
ATNTH3	XA24-10	A62J20-11
ATNTH4	XA24-9	A62J20-4
BIAS S/H PULSE	XA21-19	XA22-8
BVSWP	XA58-40	XA27-31
DAV	XA60-6	A62J7-11
DB0	XA60-20[b]	XA21-10, XA23-9, XA26-15, XA27-22, XA28-11, XA37-1, XA42-21, XA43-21, XA57-20, XA58-20, XA59-20, XA61-20[i], A62J1-3
DB1	XA60-76[b]	XA21-11, XA23-27, XA26-37, XA27-53, XA28-34, XA37-19, XA42-3, XA43-3, XA54-10, XA57-76, XA58-76, XA59-76, A62J1-4
DB2	XA60-21[b]	XA23-10, XA26-16, XA27-23, XA28-12, XA37-2, XA42-22, XA43-22, XA54-29, XA57-21, XA58-21, XA59-21, A62J1-5
DB3	XA60-77[b]	XA23-28, XA26-38, XA27-54, XA28-35, XA37-20, XA42-4, XA43-4, XA54-11, XA57-77, XA58-77, XA59-77, A62J1-6
DB4	XA60-22[b]	XA21-12, XA23-11, XA26-17, XA27-24, XA28-13, XA37-3, XA42-23, XA43-23, XA54-30, XA57-22, XA58-22, XA59-22, A62J1-7
DB5	XA60-78[b]	XA21-13, XA23-29, XA27-55, XA28-36, XA37-21, XA42-5, XA43-5, XA54-12, XA57-78, XA58-78, XA59-78, A62J1-8

[a] Multiple sources

[b] Open collector bus — multiple sources.

[i] The A61 board assembly is not included with the HP 8340B/41B. Traces connected to XA61 are included in this wiring list to keep signal destinations complete.

Table E-1. Motherboard Wiring List

Mnemonic	Description	Type	Levels
DB6	INSTRUMENT I/O DATA BUS BIT 6	DIGITAL	TTL
DB7	INSTRUMENT I/O DATA BUS BIT 7	DIGITAL	TTL
DB8	INSTRUMENT I/O DATA BUS BIT 8	DIGITAL	TTL
DB9	INSTRUMENT I/O DATA BUS BIT 9	DIGITAL	TTL
DB10	INSTRUMENT I/O DATA BUS BIT 10	DIGITAL	TTL
DB11	INSTRUMENT I/O DATA BUS BIT 11	DIGITAL	TTL
DB12	INSTRUMENT I/O DATA BUS BIT 12	DIGITAL	TTL
DB13	INSTRUMENT I/O DATA BUS BIT 13	DIGITAL	TTL
DB14	INSTRUMENT I/O DATA BUS BIT 14	DIGITAL	TTL
DB15	INSTRUMENT I/O DATA BUS BIT 15	DIGITAL	TTL
DETLVL	DETECTED LEVEL INPUT TO A.D.C.	ANALOG	−0.2V/dB, 0V=0dB
DETOUT	DETECTED LEVEL INPUT TO LINEAR MOD BOARD	ANALOG	−0.3VdB, 0V=0dB
DET S/H+	DETECTOR SAMPLE/HOLD CONTROL	DIGITAL	+4.5V/+3.5V
DET S/H−	DETECTOR SAMPLE/HOLD CONTROL	DIGITAL	+3.5V/+4.5V
DIV N2	500 KHZ DIVIDED OUTPUT FROM PLL2 DIVIDER	DIGITAL	TTL (LOW TRUE)
DIO1	IEEE 488 I/O DATA BUS BIT 1	DIGITAL	TTL
DIO2	IEEE 488 I/O DATA BUS BIT 2	DIGITAL	TTL
DIO3	IEEE 488 I/O DATA BUS BIT 3	DIGITAL	TTL
DIO4	IEEE 488 I/O DATA BUS BIT 4	DIGITAL	TTL
DIO5	IEEE 488 I/O DATA BUS BIT 5	DIGITAL	TTL
DIO6	IEEE 488 I/O DATA BUS BIT 6	DIGITAL	TTL
DIO7	IEEE 488 I/O DATA BUS BIT 7	DIGITAL	TTL
DIO8	IEEE 488 I/O DATA BUS BIT 8	DIGITAL	TTL
EOI	IEEE 488 END OR IDENTIFY (EOI)	DIGITAL	TTL
EXDET	EXTERNAL DETECTOR INPUT	ANALOG	0.5mV TO 2V
EXDETR	EXTERNAL DETECTOR INPUT GROUND RETURN	GROUND	0V

Table E-1. Motherboard Wiring List

Mnemonic	Source	Destination
DB6	XA60-23[b]	XA21-14, XA23-12, XA26-39, XA27-25, XA28-14, XA37-4, XA42-24, XA43-24, XA54-31, XA57-23, XA58-23, XA59-23, A62J1-9
DB7	XA60-79[b]	XA21-15, XA23-30, XA26-40, XA27-56, XA28-37, XA37-22, XA42-6, XA43-6, XA54-13, XA57-79, XA58-79, XA59-79, A62J1-10
DB8	XA60-24[b]	XA21-31, XA23-13, XA27-26, XA28-15, THRU A62R7 TO XA36-2, XA37-5, XA42-25, XA43-25, XA54-32, XA57-24, XA58-24, XA59-24, A62J1-11
DB9	XA60-80[b]	XA23-31, XA24-14, XA27-57, XA28-38, THRU A62R8 TO XA36-17, XA37-23, XA42-7, XA43-7, XA54-14, XA57-80, XA58-80, XA59-80, A62J1-12
DB10	XA60-25[b]	XA23-14, XA24-15, XA27-27, XA28-16, THRU A62R9 TO XA36-3, XA37-7, XA42-26, XA43-26, XA54-33, XA57-25, XA58-25, XA59-25, A62J1-13
DB11	XA60-81[b]	XA21-32, XA24-32, XA26-35, XA27-58, THRU A62R10 TO XA36-18, XA37-25, XA42-8, XA43-8, XA54-15, XA57-81, XA58-81, XA59-81, A62J1-14
DB12	XA60-26[b]	XA24-16, XA54-34, XA57-26, XA58-26, XA59-26, A62J1-15
DB13	XA60-82[b]	XA24-34, XA54-16, XA57-82, XA58-82, XA59-82, A62J1-16
DB14	XA60-27[b]	XA54-35, XA57-27, XA58-27, XA59-27, A62J1-17
DB15	XA60-83[b]	XA54-17, XA57-83, XA58-83, XA59-83, A62J1-18
DETLVL	XA25-33	XA27-29
DETOUT	XA25-32	XA26-10
DET S/H+	XA21-3	XA25-2
DET S/H−	XA21-21	XA25-24
DIV N2	XA42-27	XA41-19
DIO1	XA60-57	XA59-57, A62J7-1
DIO2	XA60-58	XA59-58, A62J7-3
DIO3	XA60-59	XA59-59, A62J7-5
DIO4	XA60-60	XA59-60, A62J7-7
DIO5	XA60-61	XA59-61, A62J7-2
DIO6	XA60-62	XA59-62, A62J7-4
DIO7	XA60-63	XA59-63, A62J7-6
DIO8	XA60-64	XA59-64, A62J7-8
EOI	XA60-7	XA59-7, A62J7-9
EXDET	A62J16 CENTER	XA25-44
EXDETR	A62J16 SHIELD[a]	XA25-43, GUARD TRACE AROUND EXDET

[a] Multiple sources.

[b] Open collector bus.

Table E-1. Motherboard Wiring List

Mnemonic	Description	Type	Levels
EXT TRIG	EXTERNAL TRIGGER INPUT	TTL/ANALOG	EXT SOURCE LVL
FAN1 FAN2 FAN3 FAN4	SWITCHED FAN POWER SWITCHED FAN POWER PRIMARY FAN POWER PRIMARY FAN POWER	AC LINE AC LINE AC LINE AC LINE	110 VAC 110 VAC 110 VAC 110 VAC
FM OUT	FREQUENCY MODULATOR OUTPUT	ANALOG	
FM DRVR SHIELD	FREQUENCY MODULATOR OUTPUT SHIELD	GROUND	0V
FM INPUT	FREQUENCY MODULATOR INPUT	ANALOG	−8V TO +8V
FM SHIELD	FREQUENCY MODULATOR INPUT SHIELD	GROUND	0V
FPNLSWP FPNLSWP RTN	FRONT PANEL SWEEP RAMP FRONT PANEL SWEEP RAMP GROUND RETURN	ANALOG GROUND	10V/SWEEP 0V
GND	ANALOG GROUND	GROUND	0V
GND HPIB GND PLANE	IEEE 488 GROUND DIGITAL GROUND	GROUND GROUND	0V 0V

Table E-1. Motherboard Wiring List

Mnemonic	Source	Destination
EXT TRIG	A62J31-4,22	XA57-106
FAN1 FAN2 FAN3 FAN4	A62K1-7 A62K1-10 A62P2 (SOLDER PAD) A62P1 (SOLDER PAD)	A62J30-3 A62J30-1 A62K1-5 A62K1-14, A62XA35
FM OUT	XA23-16	THRU A62J24 SMC CENTER TO A44J3
FM DRVR SHIELD	XA23-34	A62J24 SMC SHIELD
FM INPUT	XA23-18	A62J17 SMC CENTER
FM SHIELD	XA23-17	A62J17 SMC SHIELD
FPNLSWP FPNLSWP RTN	XA57-43 XA57-99	A62J9 SMC CENTER GUARD TRACE AROUND FPNLSWP, A62J9 SMC SHIELD
GND	NOTES [c,d,e,f]	XA19-10, 22, XA21-8, 26, XA22-5, 6, 23, 24, XA23-8, 26, XA24-8, XA25-9, 10, 31, XA26-6, 28, XA27-6, 37, XA28-6, 28, XA34P2-10, 11, XA35-4, 22, XA36-1, 5, 6, 7, 8, 10, 11, 14, 16, 19, 20, 21, 22, 26, 29, XA37-6, 9, 10, 13 THRU 17, 24, 27 THRU 35, XA38-1 THRU 11, 14 THRU 26, 29, 30, XA39-2 THRU 11, 13, 14, 17 THRU 26, 28; 29, XA40-2 THRU 6, 10, 14, 17, 21, 25, 29, XA41-1, 3, 6, 10, 11, 14, 16, 18, 21, 22, 25, 26, 29, XA42-10, 17, 20, 28, 35, XA43-11, 12, 13, 14, 17, 27, 29, 35, XA52-19, 43, XA53-14, 15, 16, 33, 34, 35, XA54-5, 23, XA55-5, 6, 20, 21, XA56-5, 20, A62J2-2, 19, A62J3-2, 4, A62J23 SHIELD, A62C2(−), A62C3(−), A62C5, A62C6(−), A62C7(−), A62R3, A62R14, CHASSIS, A62DS1 CATHODE M/N ASSY GND PLANE, T1 WHITE WIRE, ALL GROUNDS CONNECT TO THE 20/30 CASTING GND PLANE GROUNDED TO THE CHASSIS BY THE CASTING AND TO STAR GROUND
GND HPIB GND PLANE	CONNECTED TO REAR PANEL GND[h]	A62J7-12, 14, 16, 18, 20, 22, 23, 24 (NO CONNECTION − THESE ARE GROUNDED AT THE REAR PANEL) XA22-14, 32[g], XA23-6, 24, XA24-26, XA27-7, 19, 38, 50, XA57-1, 29, 30, 31, 34, 40, 55, 56, 70, 71, 72, 75, 84, 85, 86, 89, 110, XA58-1, 34, 44, 45, 46, 55, 56, 70, 71, 75, 89, 99, 101, 55, 110, XA59-1, 40 THRU 44, 55, 56, 75, 96, 97, 110, XA60-1, 40 THRU 44, 55, 56, 70, 71, 72, 75, 96 THRU 100, 110, XA61-1, 34, 40, 41, 42, 43, 44, 55, 56, 70, 71, 72, 75, 89, 96, 97, 98, 99, 100, 110[i], A62J1-1, 21, 29, 38, 39, 40, 41, 46, 48, 50, A62J20-1, A62J31-12, 35, A62J35-10, A62J19-1, 9, GND PLANE NEAR RF SECTION

[c] M/N assembly ground plane connected to Star Ground through W45.

[d] 20/30 loops casting.

[e] Star Ground connected to A47W3, and also to the M/N assembly ground plane through W45.

[f] Ground is connected to the chassis.

[g] Reserved for future expansion.

[h] Ground Plane is located near the RF Section.

[i] *The A61 board assembly is not* included with the HP 8340B/41B. Traces connected to XA61 are included in this wiring list to keep signal destinations complete.

Table E-1. Motherboard Wiring List

Mnemonic	Description	Type	Levels
HADCEN	A.D.C. CONVERT ENABLE	DIGITAL	TTL (HIGH TRUE)
HCEN	YO DELAY COMPENSATION ENABLE	DIGITAL	TTL (HIGH TRUE)
HENDKICK	YO AND YTM KICK PULSE COMPLETE	DIGITAL	TTL (HIGH TRUE)
HFILYO	FILTER YO ENABLE	DIGITAL	TTL (HIGH TRUE)
HINT	INTERNAL/EXTERNAL LEVELING CONTROL	DIGITAL	TTL (HIGH TRUE)
HIPMOD DRV	HIGH BAND PULSE MODULATOR DRIVE	ANALOG	PIN DIODE CURRENT
HLBW	ALC LOOP BAND WIDTH CONTROL	DIGITAL	TTL (HIGH TRUE)
HLB0	ENCODED BAND INFO BIT 0	DIGITAL	TTL (HIGH TRUE)
HLB1	ENCODED BAND INFO BIT 1	DIGITAL	TTL (HIGH TRUE)
HLB2	ENCODED BAND INFO BIT 2	DIGITAL	TTL (HIGH TRUE)
HLEY	LOCK ENABLE FOR YO LOOP	DIGITAL	TTL (HIGH TRUE)
HLE2	LOCK ENABLE TO PLL2	DIGITAL	TTL (HIGH TRUE)
HMRKR	MARKER ASSERTED	DIGITAL	TTL (HIGH TRUE)
HMTR	EXTERNAL METER LEVELING CONTROL	DIGITAL	TTL (HIGH TRUE)
HNUP	NEGATIVE POWER SUPPLIED UP SIGNAL	DIGITAL	TTL (HIGH TRUE)
HOVC	INTERNAL 10 MHZ STANDARD TEMP ERROR	ANALOG	+3V - OVEN WARM
HPLSEN	PULSE MODULATION ENABLED	DIGITAL	TTL L(HIGH TRUE)
HPUP	POSITIVE POWER SUPPLIES UP SIGNAL	DIGITAL	TTL (HIGH TRUE)
HRFON	RF OUTPUT POWER ON	DIGITAL	TTL (HIGH TRUE)
HSP	SWEEP IN PROGRESS	DIGITAL	TTL (HIGH TRUE)
HSTD	INTERNAL 10 MHZ STANDARD ENABLE	DIGITAL	TTL (HIGH TRUE)
HULH	3.7 GHZ OSCILLATOR UNLOCKED	DIGITAL	TTL (HIGH TRUE)
HULM	M/N OSCILLATOR UNLOCKED	DIGITAL	TTL (HIGH TRUE)
HULR	REFERENCE OSCILLATOR UNLOCKED	DIGITAL	TTL (HIGH TRUE)
HULY	YO 2-7 GHZ OSCILLATOR UNLOCKED	DIGITAL	TTL (HIGH TRUE)
HUL1	PLL1 OSCILLATOR UNLOCKED	DIGITAL	TTL (HIGH TRUE)
HUL2	PLL2 OSCILLATOR UNLOCKED	DIGITAL	TTL (HIGH TRUE)

Table E-1. Motherboard Wiring List

Mnemonic	Source	Destination
HADCEN	XA21-1	XA27-8
HCEN	XA59-67	XA55-14
HENDKICK	XA28-18	XA24-31
HFILYO	XA59-47,72	XA58-72, A62J2-5
HINT	XA26-42	XA21-28, XA25-42
HIPMOD DRV	XA21-36	A62J25 SMC CENTER
HLBW	XA26-33	XA21-6, XA25-11
HLB0	XA27-46	XA22-25, XA24-20, XA26-29, XA28-31
HLB1	XA27-16	XA22-26, XA24-21, XA26-30, XA28-32
HLB2	XA27-47	XA22-27, XA24-22, XA26-31, XA28-33
HLEY	XA59-51	A62J2-3
HLE2	XA59-53	XA41-2, XA42-2, XA43-2
HMRKR	XA57-2,12	XA26-43
HMTR	XA26-13	XA21-20, XA25-36
HNUP	XA53-17, XA56-1,16	XA52-44
HOVC	A62J3-3	XA59-10, XA61-85[i]
HPLSEN	XA26-2	XA21-9, XA25-3
HPUP	XA52-46	XA59-95, XA60-95, XA61-95[i], A62J1-22
HRFON	XA57-105	XA21-27, XA22-17, XA26-24
HSP	XA57-13	XA26-7, XA28-26, XA55-22, XA58-13, XA59-13, A62J2-14
HSTD	XA59-66	XA52-21
HULH	A62J19-16	XA57-49,104, XA59-105
HULM	XA34P1-8	XA59-104
HULR	XA34P2-14	XA59-49
HULY	A62J2-16	XA59-50
HUL1	XA37-26, XA39-1,16	XA59-106
HUL2	XA41-4	XA59-107

[i] The A61 board assembly is not included with the HP 8340B/41B. Traces connected to XA61 are included in this wiring list to keep signal destinations complete.

Table E-1. Motherboard Wiring List

Mnemonic	Description	Type	Levels
HXREF	EXTERNAL REFERENCE ENABLE	DIGITAL	TTL (HIGH TRUE)
IFC	IEEE 488 INTERFACE CLEAR (IFC)	DIGITAL	TTL (LOW TRUE)
L ADR HOLD	(USED FOR FACTORY PROGRAMMING ONLY)	DIGITAL	TTL (LOW TRUE)
LALTEN	ALTERNATE MODE ENABLED	DIGITAL	TTL (LOW TRUE)
LALTSEL	CURRENT INST. STATE (FORE/BACK GROUND)	DIGITAL	TTL (LOW TRUE)
LATTN	ATTENUATOR INSTALLED SENSING	DIGITAL	TTL (LOW TRUE)
LBX	BAND CROSS	DIGITAL	TTL (LOW TRUE)
LCHNG	INSTRUMENT STATE CHANGED	DIG. OPEN COLL.	TTL (LOW TRUE)
LCK1	DATA STROBE TO PLL2 COUNTERS (0, R2:)	DIGITAL	TTL (LOW TRUE)
LCK2	DATA STROBE TO PLL2 DIR. DIVIDER (0, R0:)	DIGITAL	TTL (LOW TRUE)
LCK3	DATA STROBE TO PLL2 PRETUNE DAC (0, R1:)	DIGITAL	TTL (LOW TRUE)
LCK4	DATA STROBE TO PLL1 VCO GAIN SWITCH (0, R3:)	DIGITAL	TTL (LOW TRUE)
LDETBW	DETECTOR LOW BAND WIDTH CONTROL	DIGITAL	TTL (LOW TRUE)
LHET	HETRODYNE BAND ENABLED	DIGITAL	TTL (LOW TRUE)
LHIBND	FUNDAMENTAL OR MULTIPLED BAND ENABLED	DIGITAL	TTL (LOW TRUE)
LHSOT	HEAT SINK OVER TEMPERATURE SENSOR	DIGITAL	TTL (LOW TRUE)
LHSOT RTN	HEAT SINK OVER-TEMP SENSOR BND RETURN	GROUND	0V
LINE TRIG	LINE TRIGGER SENSING 5V SECONDARY	RECTIFIED AC	LINE FREQ 7V TO −10V
LIPS	INSTRUMENT - PRESET	DIG. OPEN COLL.	TTL (LOW TRUE)
LKICKYO	LOW KICK PULSE	ANALOG	0 TO +5V
LMNE	M/N OSCILLATOR LOCK ENABLED	DIGITAL	TTL (LOW TRUE)
LMODHLD	LINEAR MODULATOR SAMPLE/HOLD	DIGITAL	TTL
LOMD	OVER-MODULATION DETECTED	DIG. OPEN COLL.	TTL (LOW TRUE)
LOPMOD DRV	LOW BAND PULSE MODULATOR DRIVE	ANALOG	CURRENT SOURCE
LPROG	(USED FOR FACTORY PROGRAMMING ONLY)	DIGITAL	TTL (LOW TRUE)

Table E-1. Motherboard Wiring List

Mnemonic	Source	Destination
HXREF	A62J31-21	XA58-108, XA59-98
IFC	A62J7-17	XA60-3
L ADR HOLD	XA60-45	XA61-45[i]
LALTEN	XA57-60	A62J31-9,27
LALTSEL	XA57-59	A62J31-10,28
LATTN	A62J20-14	XA27-39
LBX	XA57-69, XA58-69, XA59-69	
LCHNG	NOTE [b]	XA27-21, XA58-100, XA59-45
LCK1	XA59-54	XA42-19
LCK2	XA59-109	XA42-1
LCK3	XA59-108	XA43-19
LCK4	XA59-52	THRU A62R11 TO XA36-4, XA37-8
LDETBW	XA26-9	XA25-39, A62J34-2
LHET	XA27-20	XA21-29, XA22-12, XA25-37, A62J19-7,8
LHIBND	XA26-23	A62J19-15
LHSOT	A62J31-30	XA52-12
LHSOT RTN	A62J31-12	GND PLANE
LINE TRIG	A62CR1 CATHODE	XA57-57,68, THRU A62R1 TO PWR ON LED
LIPS	XA52-36, A62J1-19	XA57-14, XA58-14, XA59-14, XA60-14, XA61-14[i]
LKICKYO	XA54-19	XA55-1
LMNE	XA59-86	XA34P1-2
LMODHLD	XA21-2	XA26-1
LOMD	XA26-8, A62J2-7	XA27-48
LOPMOD DRV	XA21-16	A62J10 SMC CENTER
LPROG	XA60-101	XA61-101[i]

[b] Open collector bus – multiple sources.

[i] The A61 board assembly is not included with the HP 8340B/41B. Traces connected to XA61 are included in this wiring list to keep signal destinations complete.

Table E-1. Motherboard Wiring List

Mnemonic	Description	Type	Levels
LRETRACE	RETRACE	DIGITAL	TTL (LOW TRUE)
LRSP	RESET SWEEP CONTROL	DIGITAL	TTL (LOW TRUE)
LSBY	STANDBY CONTROL	DIGITAL	0V TO +22V
LSPLD	SWEEP L.E.D. CONTROL OFF/ON	DIGITAL	TTL
LSSP	STEP SWEEP	DIG. OPEN COLL.	TTL (LOW TRUE)
LSRQ	SERVICE REQUEST	DIG. OPEN COLL.	TTL (LOW TRUE)
LSTEPUP	STEP UP FOR EXTERNAL FOOT SWITCH	DIGITAL	TTL (LOW TRUE)
LSTP	PROCESSOR STOPPED	DIGITAL	TTL (LOW TRUE)
LUNLVL	INSTRUMENT UNLEVELED	DIG. OPEN COLL.	TTL (LOW TRUE)
LVLCOR	LEVELING CORRECTION	ANALOG	1.25 dB/V 0V=0dB
LVLREF	A.L.C. LEVEL REFERENCE	ANALOG	.2V/dB 0V=0dBm
LVSX	DISABLE YO SWEEPS	DIGITAL	TTL (LOW TRUE)
LYOKICK LYSP	YO SWEEP	DIGITAL	TTL (LOW TRUE)
MKR RMP	SWEEP RAMP TO MARKER BANDCROSS BOARD	ANALOG	0 TO 10V/SWEEP
MOD RTN	ALC MODULATORS GROUND RETURN	GROUND	0V
MODHI	HIGH BAND MODULATOR DRIVE	ANALOG	CURRENT SOURCE
MODLO	LOW BAND MODULATOR DRIVE	ANALOG	CURRENT SOURCE
MODLVL	MODULATOR LEVEL	ANALOG	0 TO −3 LEVELED
MUTE	PLOTTER MUTE CONTROL	DIGITAL	TTL (HIGH TRUE)
M1	M NUMBER TO M/N OSCILLATOR BIT 1	DIGITAL	TTL (HIGH TRUE)
M2	M NUMBER TO M/N OSCILLATOR BIT 2	DIGITAL	TTL (HIGH TRUE)
M3	M NUMBER TO M/N OSCILLATOR BIT 3	DIGITAL	TTL (HIGH TRUE)
M4	M NUMBER TO M/N OSCILLATOR BIT 4	DIGITAL	TTL (HIGH TRUE)
M5	M NUMBER TO M/N OSCILLATOR BIT 5	DIGITAL	TTL (HIGH TRUE)

Table E-1. Motherboard Wiring List

Mnemonic	Source	Destination
LRETRACE	XA57-58	A62J31-11,29
LRSP	XA59-85	XA58-85
LSBY	A62J1-20	XA52-45, A62CR2 ANODE
LSPLD	XA58-67	A62J1-44
LSSP	XA57-107	A62J31-5,23
LSRQ	NOTE [b]	XA57-54, XA58-54, XA59-89, XA60-89, A62J1-45
LSTEPUP	A62J31-14	A62J1-28
LSTP	XA59-65	XA60-65, A62J1-43
LUNLVL	XA26-36	XA27-52
LVLCOR	XA25-14	XA27-62
LVLREF	XA27-30	XA25-13
LVSX	XA58-68	XA54-9
LYOKICK	XA54-21	XA28-41
LYSP	XA59-11	XA55-7
MKR RMP	XA58-96	XA57-96
MOD RTN	XA26-21	A62J13 SMC SHIELD, A62J14 SMC SHIELD, GUARD TRACE AROUND MODHI AND MODLO
MODHI	XA22-34, XA26-20	A62J13 SMC CENTER
MODLO	XA26-22	A62J14 SMC CENTER
MODLVL	XA26-32	XA27-61
MUTE	XA57-61	A62J31-8,26
M1	XA59-33	XA34P1-5
M2	XA59-88	XA34P1-6
M3	XA59-32	XA34P1-3
M4	XA59-87	XA34P1-4
M5	XA59-31	XA34P1-1

[b] Open collector bus – multiple sources.

Table E-1. Motherboard Wiring List

Mnemonic	Description	Type	Levels
NDAC	IEEE 488 NOT DATA ACCEPTED (NDAC)	DIGITAL	TTL
NEG BLANK	NEGATIVE BLANKING SIGNAL	DIGITAL	0, −5V
NRFD	IEEE 488 NOT READY FOR DATA (NRFD)	DIGITAL	TTL
N1	N NUMBER TO M/N OSCILLATOR BIT 1	DIGITAL	TTL
N2	N NUMBER TO M/N OSCILLATOR BIT 2	DIGITAL	TTL
N2 TUNE	TUNING SIGNAL TO PLL2 VCO	ANALOG	0V TO +7V
N2 TUNE RTN	GROUND RETURN	GROUND	0V
N3	N NUMBER TO M/N OSCILLATOR BIT 3	DIGITAL	TTL
N4	N NUMBER TO M/N OSCILLATOR BIT 4	DIGITAL	TTL
N5	N NUMBER TO M/N OSCILLATOR BIT 5	DIGITAL	TTL
N6	N NUMBER TO M/N OSCILLATOR BIT 6	DIGITAL	TTL
PEN LIFT	PLOTTER PEN LIFT	OPEN COLLECTOR	CLAMP AT 56 V
PEN LIFT RTN	PLOTTER PEN LIFT GROUND RETURN	GROUND	0V
PH1	PLL1 PHASE DETECTOR OUTPUT	ANALOG	0V TO +5V
PH2	PLL2 PHASE DETECTOR OUTPUT	ANALOG	0V TO +5V
PINBIAS	SYTM P.I.N. DIODE BIAS	DIGITAL	−4V TO +12V
PLS IN	EXTERNAL PULSE INPUT	DIGITAL	TTL
PLS IN RTN	EXTERNAL PULSE GROUND RETURN	GROUND	0V
PMOD RTN	PULSE MODULATOR DRIVE GROUND RETURN	GROUND	0V
PRETUNE	YO PRETUNE	ANALOG	−2.5V/GHz 0 ≅ 2GHz
PWR ON LED	+5 Vac THROUGH CR1 AND R1 TO DSI	POWER SUPPLY	+.78V ANODE - ON
Q1B	TRANSISTOR Q1 BASE	ANALOG	
Q1E	TRANSISTOR Q1 EMITTER	ANALOG	

Table E-1. Motherboard Wiring List

Mnemonic	Source	Destination
NDAC NEG BLANK NRFD	XA60-4 XA57-41 XA60-5	A62J7-15 A62J31-1,19 A62J7-13
N1 N2	XA59-48 XA59-103	XA34P1-15 XA34P1-14
N2 TUNE N2 TUNE RTN	XA41-23 XA41-8	XA43-28 XA43-10
N3 N4 N5 N6	XA59-47 XA59-102 XA59-46 XA59-101	XA34P1-13 XA34P1-12 XA34P1-11 XA34P1-10
PEN LIFT PEN LIFT RTN	XA57-108 XA57-109	A62J31-6,24 A62J31-25
PH1	A62R12	XA36-24, THRU A62R12 TO XA37-11
PH2	A62R13	XA36-25, THRU A62R13 TO XA37-12
PINBIAS PLS IN PLS IN RTN	XA24-24 A62J26 CENTER NOTE [a]	A62J18-10 XA21-18 XA21-17, GUARD TRACE AROUND PLS IN, A62J26 SMC SHIELD
PMOD RTN	XA21-35	GUARD TRACE AROUND HIPMOD AND LOPMOD DRV, A62J25 SMC SHIELD, A62J10 SMC SHIELD
PRETUNE	XA54-24	XA55-8,23, A62J5 SMC CENTER THRU COAX TO A62J11 SMC CENTER, XA28-22
PWR ON LED	A62R1	A62DS1 ANODE, THRU A62R1 TO LINE TRIG
Q1B Q1E	XA53-4 XA53-7,8,25,26	Q1 BASE Q1 EMITTER

[a] Multiple sources.

Table E-1. Motherboard Wiring List

Mnemonic	Description	Type	Levels
Q2B	TRANSISTOR Q2 BASE	ANALOG	
Q2E	TRANSISTOR Q2 EMITTER	ANALOG	
Q3B	TRANSISTOR Q3 BASE	ANALOG	
Q3C	TRANSISTOR Q3 COLLECTOR	ANALOG	
Q3E	TRANSISTOR Q3 EMMITER	ANALOG	
Q4B	TRANSISTOR Q4 BASE	ANALOG	
Q4C	TRANSISTOR Q4 COLLECTOR	ANALOG	
Q4E	TRANSISTOR Q4 EMITTER	ANALOG	
REN	IEEE 488 REMOTE ENABLE (REN)	DIGITAL	TTL (LOW TRUE)
RFSWP	SWEEP RAMP TO RF OUTPUT SECTION	ANALOG	10V/SWEEP
RGND	REFERENCE GROUND	GROUND	0V
RPNLSWP	REAR PANEL SWEEP OUTPUT	ANALOG	10V/SWEEP
RPNLSWP RTN	REAR PANEL SWEEP GROUND RETURN	GROUND	0V
RSTAT	READ STATUS I/D STROBE (15, R3:)	DIGITAL	TTL (LOW TRUE)
SIOA	I/O STROBE (FIRST HALF ADDRESSES)	DIGITAL	TTL (LOW TRUE)
SIOB	I/O STROBE (SECOND HALF ADDRESSES)	DIGITAL	TTL (LOW TRUE)
SPARE 1	DB0 OUTPUT MISCELLANEOUS CONTROL	DIGITAL	TTL
SPARE 2	DB1 OUTPUT MISCELLANEOUS CONTROL	DIGITAL	TTL
SR FBK	YO SENSE RESISTOR FEEDBACK	ANALOG	−5 TO −17V
SR PWR	YO SENSE RESISTOR POWER	ANALOG	−5V TO −17V

Table E-1. Motherboard Wiring List

Mnemonic	Source	Destination
Q2B	XA53-21	Q2 BASE
Q2E	XA53-1,19	Q2 EMITTER
Q3B	XA52-7	Q3 BASE
Q3C	XA52-6,30	Q3 COLLECTOR
Q3E	XA52-8,32	Q3 EMITTER
Q4B	XA52-3,27	Q4 BASE
Q4C	XA52-1,2,25,26	Q4 COLLECTOR
Q4E	XA52-4,5,28,29	Q4 EMITTER
REN	A62J7-10	XA60-2
RFSWP	XA57-42	XA27-17
RGND	A62 STAR GROUND POINT	XA22-36, XA23P1-6, 24, XA24-36, XA25-12, 34, XA26-11, 34, XA27-18, 28, 49, 60, XA28-21, 43, XA43-20, XA54-7, 25, XA55-10, 11, 25, 26, XA57-45, 46, 101 XA58-42, 43, 98, A62J4 SMC SHIELD, A62J5 SMC SHIELD, A62J6 SMC SHIELD, A62J11 SMC SHIELD A62J18 SMC SHIELD, A62J27 SMC SHIELD, A62J29-1 AND LUG NEXT TO A62J29, A62J32-1, GROUND TRACE NEXT TO 20/30 SWP, GROUND TRACE NEAR VSWP, GUARD TRACE AROUND PRETUNE, GUARD TRACE NEAR YO TUNE, GUARD TRACE AROUND PRETUNE, GUARD TRACE AROUND SYTMRES
RPNLSWP	XA57-44	A62J8 CENTER
RPNLSWP RTN	XA57-100	GUARD TRACE AROUND RPNL SWP, A62J8 SMC SHIELD
RSTAT	XA27-45	XA23-32, XA24-23, XA28-10
SIOA	XA60-15	XA27-42, XA57-15, XA58-15, XA59-15, A62J1-49
SIOB	XA60-16	XA57-16, XA58-16, XA59-16, A62J1-47
SPARE 1	A62J35-8	XA59-71
SPARE 2	A62J35-6	XA59-70
SR FBK	XA55-12,27	A62J29-2
SR PWR	XA55-13,28	A62J29-3

Table E-1. Motherboard Wiring List

Mnemonic	Description	Type	Levels
SRD BIAS	STEP RECOVERY DIODE BIAS	ANALOG	−10V/2K TO +5V
SRD BIAS CONT	STEP RECOVERY DIODE BIAS CONTROL	DIGITAL	0 TO −5 LEVELED
SRQ	IEEE 488 SERVICE REQUEST (SRQ)	DIGITAL	TTL
STAT10	STATUS WORD INPUT BIT 10	DIGITAL	TTL (LOW TRUE)
SW1	PLL1 15-30 MHZ ON/OFF CONTROL	DIGITAL	TTL
SW2	PLL1 .15 TO .3 MHZ/3-6 MHZ CONTROL	DIGITAL	TTL
SYTM COIL +	POSITIVE INPUT TO SYTM COIL	ANALOG	−40V TO −25V
SYTM COIL −	NEGATIVE INPUT TO SYTEM COIL	ANALOG	−40V
SYTM GND	SYTM GROUND	GROUND	0V
SYTMDB	SYTM DRIVE TRANSISTSOR BASE	ANALOG	−22 TO −39
SYTMDC	SYTM DRIVE TRANSISTOR COLLECTOR	ANALOG	−.6 TO −6V
SYTMHTR	REGULATOR HEATER DRIVE TO SYTM	ANALOG	0 TO +20V
SYTMRES	SYTM CURRENT SENSE FEED BACK	ANALOG	−.9V LOW BND CW
SYTM TEMP	SYTM TEMPERATURE COIL	ANALOG	100 mv/c°
SYTMTHRM	TEMP FEED BACK THERMISTOR IN SYTM	ANALOG	APPROX −5V
TCREF	ALC TEMP COMPENSATED REFERENCE	ANALOG	−.2V/dB 0V=0dBM
THERM1	LOW BAND DETECTOR THERMISTOR	ANALOG	−1V TO −8V
THERM2	LOW BAND DETECTOR THERMISTOR	ANALOG	−10V
TYOKP	TRIGGER YO KICK PULSE	DIGITAL	TTL (LOW TRUE)
VCOMP	YO DELAY COMPENSATION VOLTAGE	ANALOG	−26 MHZ/VOLT
VIDEO DET	VIDEO DETECTOR OUTPUT	ANALOG	0 TO 1.6V
VIDEO DET RTN	VIDEO DETECTOR GROUND RETURN	GROUND	0V
VSWP	YO SWEEP RAMP	ANALOG	0V TO 10V/SWEEP
WBAND	BAND INFO I/O STROBE (10, R2:)	DIGITAL	TTL (LOW TRUE)
WCDAC	DELAY COMPENSATION DAC DATA STROBE (5, R3:)	DIGITAL	TTL (LOW TRUE)
WLEVEL	ALC REFERENCE DAC DATA STROBE (10, R1:)	DIGITAL	TTL (LOW TRUE)
WMOD	MODULATION DATA STROBE (10, R0:)	DIGITAL	TTL (LOW TRUE)
WPDAC	PRE-TUNE DAC DATA STROBE (3, R2:)	DIGITAL	TTL (LOW TRUE)
WRDAC	RESET DAC DATA STROBE (1, R2:)	DIGITAL	TTL (LOW TRUE)

Table E-1. Motherboard Wiring List

Mnemonic	Source	Destination
SRD BIAS	XA22-31	A62J18-2
SRD BIAS CONT	XA26-18	XA24-13
SRQ	A62J7-19	XA60-9
STAT10	XA23-22	XA24-4
SW1	XA42-32	XA36-23, XA40-24
SW2	XA42-14	XA40-22
SYTM COIL +	XA28-42	A62J18-4, A62J32-3
SYTM COIL −	A62J18-12	XA28-5,27
SYTM GND	A62J18-13,14,15	XA22-35
SYTMDB	XA28-19	A62J32-2
SYTMDC	XA28-20	A62J32-4
SYTMHTR	XA24-19	A62J18-8
SYTMRES	XA28-44	A62J32-5
SYTM TEMP	A62J18-5	A22P1-7, XA27-13
SYTMTHRM	A62J18-9	XA24-2
TCREF	XA25-35	XA26-12
THERM1	A62J34-3	XA25-4
THERM2	A62J34-1	XA25-26
TYOKP	XA59-100	XA54-18, XA58-30
VCOMP	XA54-27	XA55-9
VIDEO DET	A14J21 - SMC CENTER	XA22-11, A62J21 SMC CENTER
VIDEO DET RTN	A14J21 - SMC SHIELD	XA22-29, A62J21 SMC SHIELD
VSWP	XA58-97	A62J27 SMC CENTER THRU COAX TO A62J4 SMC CENTER, XA54-26
WBAND	XA27-43	XA28-29
WCDAC	XA59-30	XA54-28
WLEVEL	XA27-12	XA24-33
WMOD	XA27-59	XA21-33, XA23-33, XA26-44
WPDAC	XA59-68	XA54-36
WRDAC	XA59-29	XA58-29

Table E-1. Motherboard Wiring List

Mnemonic	Description	Type	Levels
WSPAT	SWEEP ATTENUATOR DATA STROBE (1, R0:)	DIGITAL	TTL (LOW TRUE)
WSPTM	SWEEP TIME DAC DATA STROBE (1, R1:)	DIGITAL	TTL (LOW TRUE)
WYOKW	YO KICK PULSE WIDTH DATA STROBE (5, R1:)	DIGITAL	TTL (LOW TRUE)
WYTMCTL	YTM CONTROL SIGNALS STROBE (11, R1:)	DIGITAL	TTL (LOW TRUE)
WYTMSLP	YTM DRIVE SLOPE DAC DATA STROBE (11, R1:)	DIGITAL	TTL (LOW TRUE)
W11R2	EXTRA I/O STROBE (11, R2:)	DIGITAL	TTL (LOW TRUE)
YO COIL +	POSITIVE INPUT TO YO COIL	ANALOG	−40V TO −20V
YO COIL −	NEGATIVE INPUT TO YO COIL	POWER SUPPLY	−40V
YO TUNE	LOW FREQ PHASE LOCK TO YO DRIVER	ANALOG	0V TO ±6V
YOXISTB	YO DRIVE TRANSISTOR BASE	ANALOG	−30V TO −39V
Z-AXIS BLANK	2-AXIS BLANKING/MARKER	DIGITAL	+5V/−5V
1.4V/GHZ	1.4V PER GHZ REFERENCE	ANALOG	+1.4V/GHZ
20/30 SWP	20/30 MHZ REFERENCE OSCILLATOR SWEEP	ANALOG	0V TO +10V
500 KHZ REF	PLL2 500 KHZ REFERENCE	DIGITAL	TTL
8410 TRIG	SYNCHRONIZING TRIGGER TO 8410B INTERFACE	DIGITAL	TTL
+1.0 V/GHZ	+1.0V/GHZ FREQUENCY REFERENCE	ANALOG	1.0V/GHZ
+1.0 V/GHZ RTN	+1.0V/GHZ FREQUENCY REFERENCE GROUND RETURN	GROUND	0V
+5V AC1	+5V TRANSFORMER SECONDARY	TI SEC.	7 VAC
+5V AC2	+5V TRANSFORMER SECONDARY (GREEN)	TI SEC.	7 VAC
+5V SENSE (+)	+5.2 VOLT SUPPLY POSITIVE SENSE	POWER SUPPLY	+5.2V
+5V SENSE (−)	+5.2 VOLT SUPPLY POSITIVE SENSE	POWER SUPPLY	0V
+5V UNREG	UNREGULATED SUPPLY TO +5V	POWER SUPPLY	+7V TO +9V
+5.2V	REGULATED +5.2 VOLT SUPPLY	POWER SUPPLY	+5.2V

Table E-1. Motherboard Wiring List

Mnemonic	Source	Destination
WSPAT	XA59-84	XA58-84
WSPTM	XA59-28	XA58-28
WYOKW	XA59-99	XA54-6
WYTMCTL	XA27-14	XA28-8
WYTMSLP	XA27-44	XA28-30
W11R2	XA27-15	XA23-15
YO COIL+	XA55-15,30	A62J2-6,15, A62J29-5
YO COIL−	A62J2-8,13	SEPARATE TRACE TO −40V SENSE POINT
YO TUNE	XA55-24	A62J6 SMC CENTER
YOXISTB	XA55-29	A62J29-4
Z-AXIS BLANK	XA57-97	A62J31-2,20
1.4V/GHZ	XA28-7	XA22-30
20/30 SWP	XA58-41	XA43-1
500 KHZ REF	XA42-9	XA41-20
8410 TRIG	XA57-62	A62J31-7
+1.0 V/GHZ	XA28-17	A62J31-31,32
+1.0 V/GHZ RTN	XA28-39	A62J31-13
+5V AC1	A62 LUG 5	XA35-8,9,10,26,27,28, T1 GREEN WIRE
+5V AC2	A62 LUG 5	XA35-12,13,14,30,31,32, T1 GREEN WIRE, A62CR1 ANODE
+5V SENSE(+)	XA52-15	TO TRACE ON A62 NEAR XA52-17, +5.2 VOLT SENSE POINT
+5V SENSE(−)	XA52-39	TO A62 STAR GROUND[c]
+5V UNREG	XA35-1, 2, 3, 19, 20, 21	XA52-13,14,37,38, A62C2(+), A62C3(+), THRU A62R3 TO GND
+5.2V	XA52-17,18,41,42	XA21-5,23, XA22-2,20, XA23-3,21, XA24-3, XA25-6,28, XA26-4,26, XA27-3,34, XA28-2,24, XA34P2-4,5, THRU A62L1 TO XA36-15,30, THRU A62L3 TO XA37-18,36, THRU A62L7 TO XA39-15,30, XA40-15,30, XA41-15,30, XA42-18,36, XA43-18,36, XA54-2,20, XA55-2,17, XA57-36,37,92, XA58-36,37,92, XA59-36,37,92, XA60-36,37,92, XA61-36,37,92[i], A62J1- 31 THRU 37, A62J2-4,17, A62J19-3,11, A62J31-3

[c] M/N assembly ground plane connected to Star Ground through W45.

[g] Reserved for future expansion.

[i] The A61 board assembly is not included with the HP 8340B/41B. Traces connected to XA61 are included in this wiring list to keep signal destinations complete.

Table E-1. Motherboard Wiring List

Mnemonic	Description	Type	Levels
+12V	REGULATED +12 VOLT SUPPLY	POWER SUPPLY	+12V
+12V UNREG	UNREGULATED SUPPLY TO +12V	POWER SUPPLY	+20V
+12V U1 ADJ	+12V REGULATOR ADJUSTMENT TERMINAL	POWER SUPPLY	+10.5V
+20V	REGULATED +20 VOLT SUPPLY	POWER SUPPLY	+20V
+20V AC1	TRANSFORMER SECONDARY FOR +20V SUPPLY	POWER SUPPLY	26.4 VAC
+20V AC2	TRANSFORMER SECONDARY FOR +20V SUPPLY	POWER SUPPLY	26.4 VAC
+20V REF OSC	SWITCHED +20V SUPPLY TO 10 MHZ REF.	POWER SUPPLY	0V/+20V
+20V UNREG	UNREGULATED SUPPLY TO +20V	POWER SUPPLY	+31.2V
+22V	REGULATED +22 VOLT SUPPLY	POWER SUPPLY	+22V
−.25V/GHZ	−.25 VOLTS/GHZ OUTPUT FREQUENCY	POWER SUPPLY	−.25V/GHZ
−5.2V	REGULATED −5.2 VOLT SUPPLY	POWER SUPPLY	−5.2V
−7V REF	−7V REFERENCE SUPPLY	POWER SUPPLY	−7V
−10V	REGULATED −10 VOLT SUPPLY	POWER SUPPLY	−10V
−10V AC1	TRANSFORMER SECONDARY FOR −10V SUPPLY	POWER SUPPLY	13.9 VAC
−10V AC2	TRANSFORMER SECONDARY FOR −10V SUPPLY	POWER SUPPLY	13.9 VAC
−10V RTN	−10V SUPPLY SERIES PASS COLLECTOR	POWER SUPPLY	+6.4V AT 13.3 GHZ
−10V UNREG	UNREGULATED SUPPLY TO +10V	POWER SUPPLY	−10V

Table E-1. Motherboard Wiring List

Mnemonic	Source	Destination
+12V	XA52-9,33	XA23-2,20, XA57-91, XA58-91, XA59-91, XA60-91, XA61-91[i], A62J1-2, A62CR3 CATHODE, A62U1 CASE
+12V UNREG	XA52-11,35	A62U1-1, A62C7(+)
+12V U1 ADJ	XA52-10	A62C6(+), A62CR3 ANODE, THRU A62R4 TO GND, A62U1-2
+20V	XA52-16,40	XA21-4,22, XA22-1,19, XA23-1,19, XA24-1, XA25-5,27, XA26-3, XA27-2,33, XA28-1,23, XA34P2-2,3, THRU A62L2 TO XA36-13,28, THRU A62L5 TO XA38-13,28, XA40-13,28, XA41-13,28, XA42-16,34, XA43-16,34, XA52-16,40 (+20V SENSE POINT), XA53-29, XA54-1, XA55-1,16, XA57-35,90, XA58-35,90, XA59-35,90, XA60-35,90, XA61-35[i], A62J2-9,12, A62J18-6, A62J19-2,10
+20V AC1	A62 LUG 2	XA19-1,13, T1 RED WIRE
+20V AC2	A62 LUG 2	XA19-2,14, T1 RED WIRE
+20V REF OSC	XA52-20	A62J3-1
+20V UNREG	XA35-7,25	XA19-9,21, XA52-23,24,47,48
+22V	XA35-18,36	XA60-88, XA61-90[i], A62CR2 CATHODE, A62J1-30, A62J3-5, A62K1-2
−.25 V/GHZ	XA28-40	XA25-38, XA27-51
−5.2V	XA53-18,36	XA23-4, XA27-1,32, XA34P2-12,13, XA52-22, XA57-93, XA58-93, XA59-93, XA60-93, XA61-93[i], A62J1-42, A62J2-1,20, A62J19-4,12
−7V REF	XA43-9	XA41-7
−10V	XA53-12,13,31,32	XA21-7,25, XA22-4,22, XA23-5,23, XA24-5, XA25-7,29, XA26-5,27, XA27-4,35, XA28-3,25, XA34P2-8,9, THRU A62L8 TO XA36-12,27, THRU A62L4 TO XA38-12,27, THRU A62L6 TO XA39-12,27, XA40-12,27, XA41-12,27, XA42-15,33, XA43-15,33, XA54-4,22, XA55-4,19, XA56-4,19, XA57-39,94, XA58-39,94, XA59-39,94, XA60-39,94, XA61-39,94[i], A62J2-10,11, A62J18-7, A62J19-5,13
−10V AC1	A62 LUG 6	XA19-3,4,15,16, T1 BLUE WIRE
−10V AC2	A62 LUG 6	XA19-5,6,17,18, T1 BLUE WIRE
−10V RTN	XA53-2,20	XA19-7,8,19,20, A62Q1 COLLECTOR
−10V UNREG	XA19-11,12,23,24	XA53-9,10,27,28

[g] Reserved for future expansion.

[i] The A61 board assembly is not included with the HP 8340B/41B. Traces connected to XA61 are included in this wiring list to keep signal destinations complete.

Table E-1. Motherboard Wiring List

Mnemonic	Description	Type	Levels
−15V	REGULATED −15V SUPPLY	POWER SUPPLY	−15V
−40V	REGULATED −40V SUPPLY	POWER SUPPLY	−40V
−40V AC1	TRANSFORMER SECONDARY FOR −40V SUPPLY	POWER SUPPLY	42.8 VAC
−40V AC2	TRANSFORMER SECONDARY FOR −40V SUPPLY		42.8 VAC
−40V RTN	−40V SUPPLY SERIES PASS COLLECTOR	POWER SUPPLY	12.7V AT 13.3 GHZ
−40V SENSE (+)	−40V SUPPLY POSITIVE SENSE	POWER SUPPLY	0V
−40V SENSE (−)	−40V SUPPLY NEGATIVE SENSE	POWER SUPPLY	−40V
−40V UNREG	UNREGULATED SUPPLY TO −40V	POWER SUPPLY	−40V

Table E-1. Motherboard Wiring List

Mnemonic	Source	Destination
−15V	XA56-15,30	XA27-5,36, XA28-4, XA54-8, XA57-38, XA58-38, XA59-38, XA60-38, XA61-38[i]
−40V	XA53-11,30	XA22-3,21[g], XA23-7,25, XA28-5,27, XA34P2-6,7, XA40-11,26, XA53-11,30, XA54-3, XA55-3,18, XA56-3,18, A62J2-8,13, A62J19-6, A62C5
−40V AC1	A62 LUG 4	XA35-15,33, T1 YELLOW WIRE
−40V AC2	A62 LUG 4	XA35-16,34, T1 YELLOW WIRE
−40V RTN	XA53-3,22	XA35-5,23, A62C1(+), A62R2, A62Q2 COLLECTOR
−40V SENSE(+)	XA53-5	A62 STAR GROUND
−40V SENSE(−)	XA53-23	A62 −40V SENSE POINT
−40V UNREG	XA35-6,24	XA53-6,24, A62C1(−), A62R2

[g] Reserved for future expansion.

[i] The A61 board assembly is not included with the HP 8340B/41B. Traces connected to XA61 are included in this wiring list to keep signal destinations complete.

Table E-2. HP 8340B Motherboard Coaxial Cables

Cable	Mnemonic/ Description	Type	Signal Level	Source	Destination
A62J12 CENTER A62J12 SHIELD	NOT USED NOT USED				XA23-36 XA23-35
A62J17 CENTER A62J17 SHIELD	FM INPUT A62 STAR GND	ANALOG GROUND	±8V 0V	J22 J22	XA23-18 XA23-17
A62J21 CENTER A62J21 SHIELD	VIDEO DET VIDEO DET RTN	ANALOG GROUND	0 TO 1.6V 0V	A14J21 A14J21	XA22-11 XA22-29
A62J22 CENTER A62J22 SHIELD	NOT USED NOT USED				XA22-10 XA22-28
A62J23 CENTER A62J23 SHIELD	NOT USED NOT USED				XA22-9 XA22-27
A62J24 CENTER A62J24 SHIELD	FM OUT FM OUT SHIELD	ANALOG GROUND	CURRENT SOURCE 0V	XA23-16 XA23-34	A44J3 A44J3

Controller Section
Assembly-Level Service

CONTENTS

Controller Section Introduction

The controller assemblies perform all digital data transfer and control functions for instrument operation. Interface circuitry provides communication with the rest of the instrument. Digital information is exchanged between the instrument processor and other sections of the instrument on a bidirectional data bus.

Rear panel interface signals (e.g. HP-IB, sweep output) are routed through or generated in the controller functional group. Sweep control signals initiated by the controller section start and stop the sweep generator. Sweep events (e.g. bandcrossings, end of sweep, markers) are monitored by the controller section and specific instructions are executed according to the type of sweep event.

ASSEMBLIES

The controller functional group consists of three assemblies:

- A57 marker/bandcross assembly
- A59 digital interface assembly
- A60 instrument processor assembly

The A60 processor will operate with the other two assemblies removed from the instrument.

Controller Section
Theory of Operation

THE ADDRESS BUS AND DATA BUS

The instrument has a 16-bit I/O data bus (DB 0-15) and a 5-bit I/O address bus (ADR 0-4) that runs throughout the instrument. The I/O data bus is bidirectional, sending and receiving data from various digital circuits.

LOW INSTRUMENT PRESET (LIPS)

When you turn the instrument on, or press **[INSTR PRESET]**, LIPS (low instrument preset) is generated. This signal initiates several events in the controller section:

- Overrides the A59 assembly's ability to shut down the processor
- Disables access to RAM
- Resets the instrument processor and the display processor
- Activates all front panel LEDs
- Activates the 16 self test LEDs on the A60 assembly

When LIPS is released, the instrument controller performs a self test that:

- Checks the instrument processor internal registers
- Partially checks RAM
- Checks ROM
- Checks the I/O address bus (ADR 1-5)
- Checks the I/O data bus (DB 0-15)
- Verifies the calibration data check sum (see service introduction)
- Checks the analog-to-digital converter

  This circuit, located on the A27 level control assembly, is essentially an internal voltmeter that allows the instrument processor to monitor several DC levels in the instrument (e.g. modulation level, sweep voltage, ALC level).

If the self test is initiated by an instrument preset, the instrument sets all front panel functions to a preset condition, and is ready to begin operation.

HIGH POWER UP (HPUP)

When you turn the power switch on, HPUP remains low until the power supplies stabilize, then it goes high, resetting the instrument processor to restore previous instrument settings (stored in RAM) after self test completes.

A57 MARKER/BANDCROSS ASSEMBLY

The A57 marker/bandcross assembly generates the z-axis signal required to place intensity markers on an external CRT. If enabled, amplitude markers are generated by sending a marker signal to the leveling circuits. The same circuits that detect markers are used to detect band crossings or the end of sweep. These circuits both cause the sweep to stop and activate the instrument processor. Other circuits interface with the rear panel connections. During self test, hardware on this assembly verifies that the instrument processor data bus is operating.

Sweep Event Memory

The sweep-event memory stores numbers that correspond to voltages on the 0-10V sweep signal. Each number stored in the memory represents a single sweep event. Sweep events are detected by the sweep comparator, which compares them against the 0-10V sweep ramp. Sweep events include:

- Turning markers on and off
- Stopping the sweep for a bandcrossing
- Stopping the sweep for the end-of-sweep and retrace

The sweep comparator also finds the current sweep position when you make changes in frequency parameters during an analog sweep longer than 300 ms.

Manual Sweep DAC

The manual sweep DAC generates the sweep-out signal when the instrument is in CW or manual mode.

Sweep Control Block

The sweep control block allows the sweep to be stopped either from the rear panel, or by the sweep comparator. With the CRT Z-axis control circuits, the sweep can be blanked on a display for bandcrossing or retrace, and markers can be intensified.

Low Bandcross (LBX)

The A57 marker/bandcross assembly uses the LBX (low bandcross) signal to stop the analog sweep at positions previously loaded in the sweep event memory by the instrument processor. When LBX is low, the A59 digital interface causes the instrument processor to run, allowing the instrument processor to perform the tasks necessary for the sweep to proceed. This happens either at a bandcrossing, or at retrace at the end of a sweep.

A59 DIGITAL INTERFACE ASSEMBLY

The digital interface links the instrument processor to the sweep generator, the reference M/N oscillator, and the 20-30 synthesizer.

Read/Write Strobes

The instrument processor read/write strobes enable buffers that either send data to the instrument processor, or clock registers that store data sent from the instrument processor. Several strobes also operate registers on other assemblies.

Low Stop (LSTP) and Low Service Request (LSRQ)

The digital interface assembly connects to the 16-bit data bus (DB0 to DB15). Using the LSTP (low stop) signal, this assembly can stop all instrument processor operations when all current tasks are completed. When the instrument processor stops, the RUN LED on the processor assembly turns off. LSTP stops the instrument processor when it is not needed, or when it is necessary to eliminate all potential sources of digital noise (e.g. during forward sweeps).

When the LSTP signal releases the instrument processor to perform a task, the instrument processor defers processing until it determines that the LSRQ (low service request) signal is low. LSRQ can be sent low by the digital interface, by the front panel interface, or by LBX (low bandcross). Once LSRQ is sensed low, it can go high again; the instrument processor finishes all pending tasks before checking this signal again.

Controller Response

Using the change detectors and the processor service request block, the instrument processor responds to the following:

- Changes in the UNLOCK or OVEN indicators
- Changes in OVERMOD or UNLEVELED conditions
- Changes in the EXTERNAL REFERENCE switch position
- Sweep events as indicated by the marker/bandcross assembly

The instrument processor also distinguishes between power on and instrument preset.

A60 PROCESSOR ASSEMBLY

The A60 processor assembly performs all instrument data processing. This assembly consist of:

- A microprocessor
- Memory
- An HP-IB interface
- The necessary circuitry for:
  clock generation
  address and memory decoding
  buffering
  interrupt handling

The microprocessor interfaces directly with memory, which consists of:

- 32K words of Ultra Violet Erasable Programmable Read Only Memory (UVEPROM)

  The instrument software program (firmware) is stored in this section of memory, with the default calibration data.

- 2K words of Electrically Erasable Programmable Read Only Memory (EEPROM)

  Protected calibration data is stored here.

- 8K words of Random Access Memory (RAM)

  Working calibration data and SAVE/RECALL register values are stored here. Battery backup provides power to RAM when AC power is disconnected. If the backup power fails, working calibration data and SAVE/RECALL information is lost. When AC power is restored, the EEPROM calibration data is loaded in RAM, and the front panel displays CALIBRATION RESTORED.

NOTE: 1 word = 2 bytes; 1 byte = 8 bits.

The microprocessor is controlled by the firmware stored in memory. With this program, the microprocessor can transfer data (I/O addressing) and internally process data it has accessed. All data transfers go through the microprocessor.

The A60 processor assembly communicates with the rest of the instrument by means of the internal address and data busses. External communication is through the HP-IB connection on the rear panel. The HP-IB interface circuitry provides the link between the internal instrument bus and the external HP-IB interface.

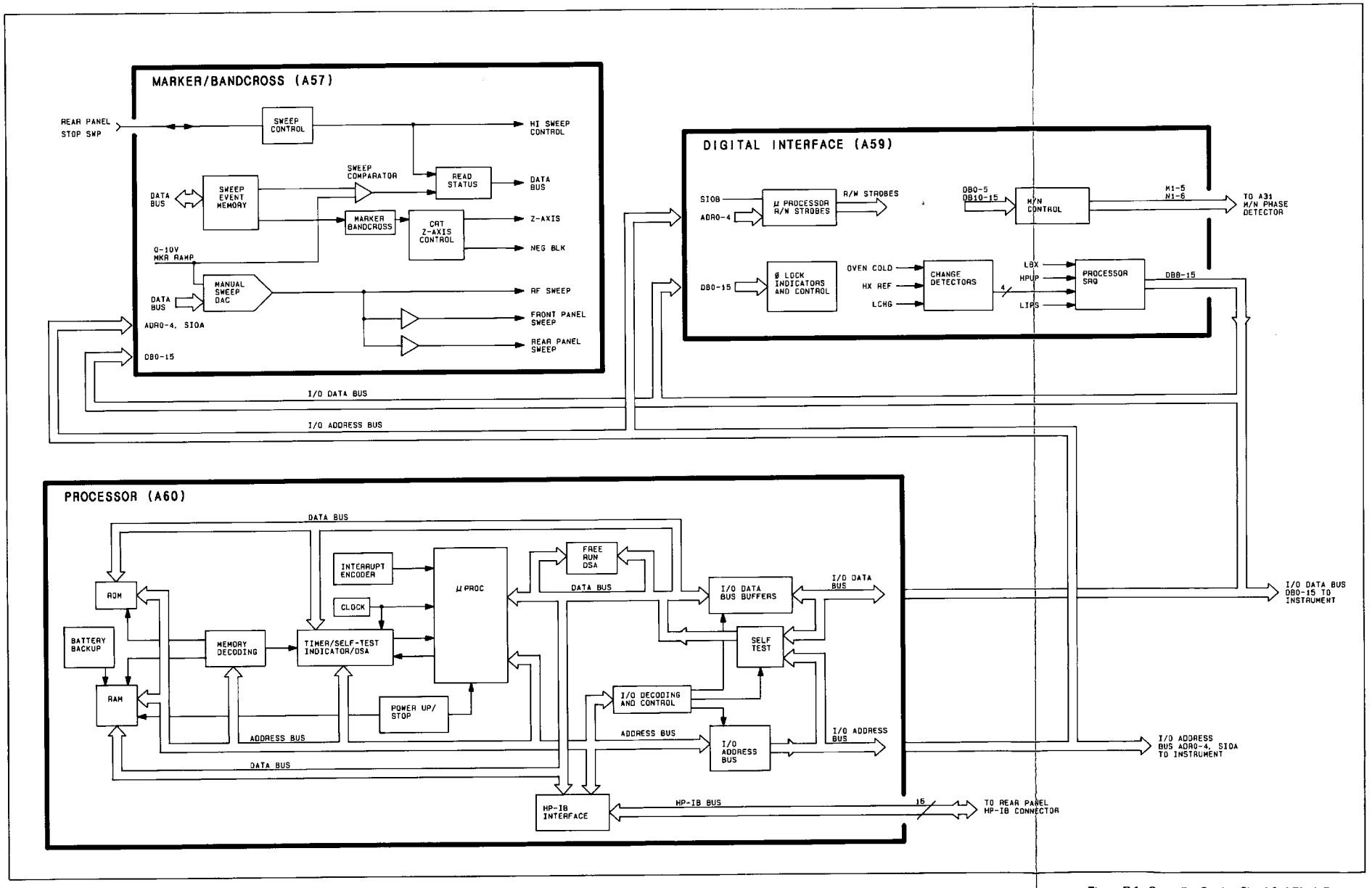


Figure F-1. Controller Section Simplified Block Diagram

Controller Section
Overall Assembly-Level Troubleshooting

Because problems on either the A57 assembly or the A59 assembly can show up indirectly in other areas of instrument operation, it is particularly important that you begin A57 and A59 troubleshooting in the overall instrument troubleshooting, located in the service introduction of this manual.

The majority of controller functional group assembly level troubleshooting is associated with the A60 processor assembly. Consequently, some A57 and A59 diagnostics and troubleshooting are included in the A60 information.

There are two levels of diagnostics and troubleshooting for the controller group:

- Self Test

  At power on and at instrument preset, self tests perform diagnostic checks on some controller group circuitry. The tests performed are diagnostic routine SHIFT M4 tests 0 through 13, and 20. Two front panel LEDs (CHECK I and II) provide a visual indication of the self test results, and are explained in the A60 assembly troubleshooting.

- Assembly Isolation

  Verify individual assembly faults by removing the assembly and observing instrument behavior. Once an assembly is suspect, its replacement verifies the cause of the problem.

Self tests, diagnostic tests, and assembly isolation procedures are described in each assembly troubleshooting section.

CAUTION

Before you remove an assembly, disconnect line power and wait several minutes for the A19 power-on safety indicator to go out.

A57 Marker/Bandcross Assembly-Level Troubleshooting

DIAGNOSTICS

The SHIFT M4 diagnostic can isolate a problem to specific circuitry on the A57 assembly. This service diagnostic tests DACs and control circuitry, and isolates the problem to individual sections of the A57 assembly. Table F-1 lists the A57 assembly circuitry tested by the SHIFT M4 routines.

Refer to the A60 processor assembly troubleshooting section for full details on the SHIFT M4 tests, their interdependence, and display results.

Table F-1. Diagnostic SHIFT M4 Tests – A57 Assembly

Number	Name	Description
9	Marker/RAM RD/WR	Verifies operation of the address register, sweep event memory, Read/Write RAM and Read/Write strobes from the A60 processor assembly.
16	Manual Sweep DAC	Verifies operation of the manual sweep DAC.
20	Bandcross DAC	Verifies operation of the sweep comparitor and the read status buffer.

The SHIFT M4 diagnostic tests approximately 50% of the A57 marker/bandcross assembly circuitry.

ASSEMBLY ISOLATION

To help verify that a problem is on the A57 assembly, remove the assembly and observe the instrument. With the A57 assembly removed, you should see the following:

1. Following power on or instrument preset, observe the instrument check LEDs:

   CHECK II should stay on, and CHECK I should go off.

2. All 16 self test LEDs on the A60 processor assembly should remain on.

3. When sweeping, the sweep ramp should stop at 12V before resetting.

NOTE: Check the sweep ramp (VSWP) at A58 TP10. Because the buffers for the sweep signal are on the A57 assembly (which you have removed), you cannot measure the sweep at either the front or rear panel connectors.

4. The instrument should work properly in CW or manual mode, and perform normally, except for the absence of sweep output and display blanking.

5. In multi-band sweep, bandcrossings all occur when the sweep ramp reaches 12V, rather than the correct voltages, because the sweep comparator DAC circuitry is located on the A57 assembly.

A59 Digital Interface Assembly-Level Troubleshooting

DIAGNOSTICS

The A60 processor responds to inputs from the A59 assembly using the processor service request and change detector circuitry for the following conditions:

- oven or unlock changes
- overmod or unleveled condition changes
- external reference switch changes
- sweep events from the A57 marker/bandcross assembly

CHANGE DETECTORS

Verify the Change Detector Circuitry

1. Connect a logic probe or storage oscilloscope to A59TP8.
2. Change the rear panel frequency standard INT/EXT switch and verify that this generates an active low pulse.

   Verify that the front panel EXT REF LED lights when the switch is in the EXT position.
3. Press **[CW]** and disconnect one of the snap-on cables in the phase lock loop (e.g. A39W1 at A40J3). Verify that the front panel UNLOCK indicator on the front panel lights.

   Verify a pulse at TP8.
4. To check HOVC, disconnect the instrument from line power for five minutes, then quickly reconnect line power and turn the power switch on. Verify that the OVEN light goes on for a few minutes, and then goes off.

SERVICE REQUEST

Verify the Processor Service Request

1. Press **[INSTR PRESET] [CW]** and verify that the RUN light on the A60 processor assembly is off. If not, the LSRQ line is pulled down, and the reset circuitry is faulty.

ASSEMBLY ISOLATION

To help verify that a problem is on the A59 assembly, remove the assembly and observe the instrument. With the A59 assembly removed, you should see the following:

1. Following power on or instrument preset, both instrument check LEDs should go off.
2. All 16 self test LEDs on the A60 processor assembly should go off.
3. Turn the line switch to standby, and then on. The instrument should preset rather than restoring the prior state.
4. Verify that the:
   - OVEN annunciator is on
   - EXT REF is annunciator is off
   - UNLOCKED annunciator is off
   - SRQ annunciator is off
   - REMOTE annunciator is off

A60 Processor Assembly-Level Troubleshooting

TYPES OF TROUBLESHOOTING

There are several types of troubleshooting for the A60 processor assembly:

- **Input Signal Verification**. This test checks several processor assembly input signals and should be performed prior to doing any in-depth troubleshooting.
- **Self Test**. Self test runs when you turn the instrument on or when you press **[INSTR PRESET]**. Two front panel LEDs (INSTR CHECK I and INSTR CHECK II) provide a visual indication of the self check results.
- **SHIFT M4**. When you initiate this diagnostic, you can check the operation of specific circuitry on the A60 processor assembly.

INPUT SIGNAL VERIFICATION

When to Use Input Signal Verification

Use input signal verification prior to in-depth troubleshooting of the A60 assembly. Verification consists of measuring all input signals to the A60 assembly, in addition to a few key signals that are required to run self test.

Equipment Required

A DVM and/or an oscilloscope.

Procedure

NOTE: The A60 processor is a static sensitive assembly. Work only at an anti-static work station.

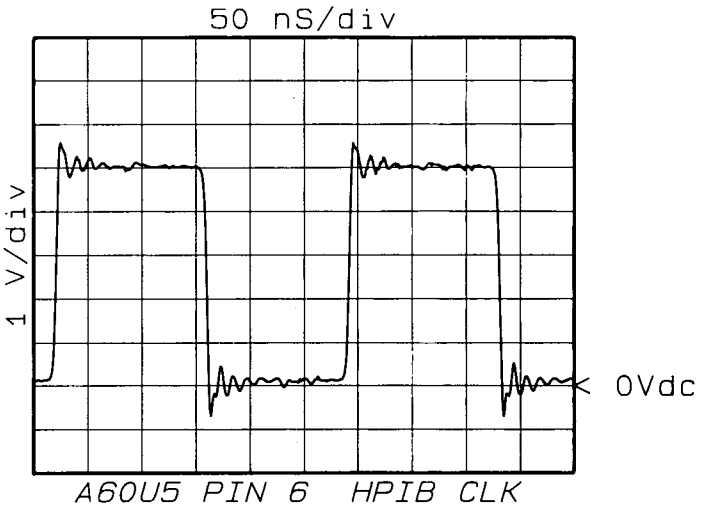
1. Turn line power off. Place the A60 processor assembly on an extender.
2. Turn line power on.
3. Using A60TP7 or A60TP17 as ground, verify the voltages in Table F-2.

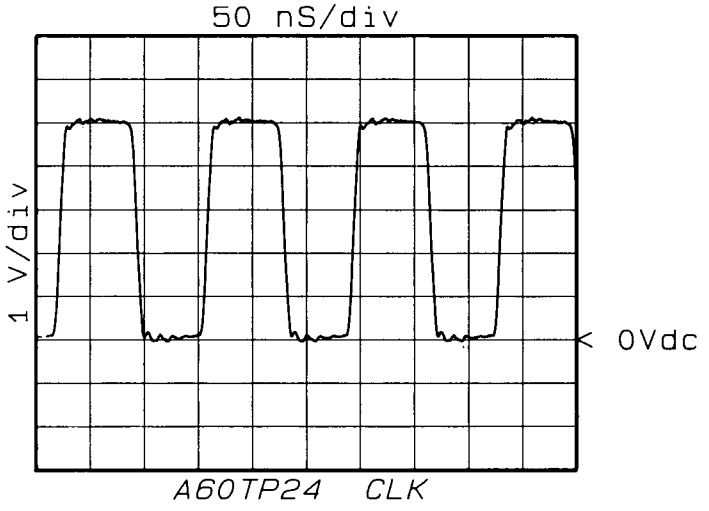
Table F-2. Input Signal Voltages

Measurement Point	Voltage
A60TP11 (LSTP)	+5V*
A60TP21 (+5V)	+5V
A60TP22 (HRAMPUP)	+5V
A60TP23 (LRESET)	+5V
A60P1-33 (Vpp)	+4.5V
A60U38 Pin 23 (VRAM)	+5V
A60U1 Pin 8 (VREF)	+1.2V
+5PF (anode of A60CR1 or A60CR4)	+5V

* A microprocessor failure can cause LSTP to be low.

4. Verify the following waveforms:





SELF TESTS

At power on and at instrument preset, self test performs diagnostic checks on some of the instrument circuitry. The tests performed are the SHIFT M4 tests 0 through 8, and 10 through 13 (described under **SHIFT M4**).

Figure F-2 shows the instrument self test flow chart.

How to Check the Results of Self Test

You can check the results of instrument self test in 3 ways:

- On the INSTR CHECK LEDs I and II
- Using the A60 Processor Self Test LEDs
- Using the diagnostic SHIFT M4

NOTE: The most accurate failure indication is given by the A60 processor self test LEDs. A failure can occur that invalidates the indication of the INSTR CHECK LEDs and SHIFT M4.

Instrument CHECK LEDs I and II

The INSTR CHECK LEDs I and II are the easiest failure indicators to check because they are located on the front panel, adjacent to the **[INSTR PRESET]** key.

Procedure

1. Switch on power or press **[INSTR PRESET]**.

   Both INSTR CHECK LEDs turn on.

   LED I turns off when the processor, memory, and peripheral interface timer (on the A60 assembly) pass self test (SHIFT M4 tests 0 through 6, 10, and 11).

   LED II turns off when the I/O address bus, I/O data bus, and marker RAM pass self test (SHIFT M4 tests 9, 12, and 13).

If no failure occurs, both LEDs are off after approximately 1 second. If either LED remains on, check the 16 LEDs on the A60 assembly. Remember that it is possible for a failure to occur that causes both INSTR CHECK LEDs to go off when they shouldn't.

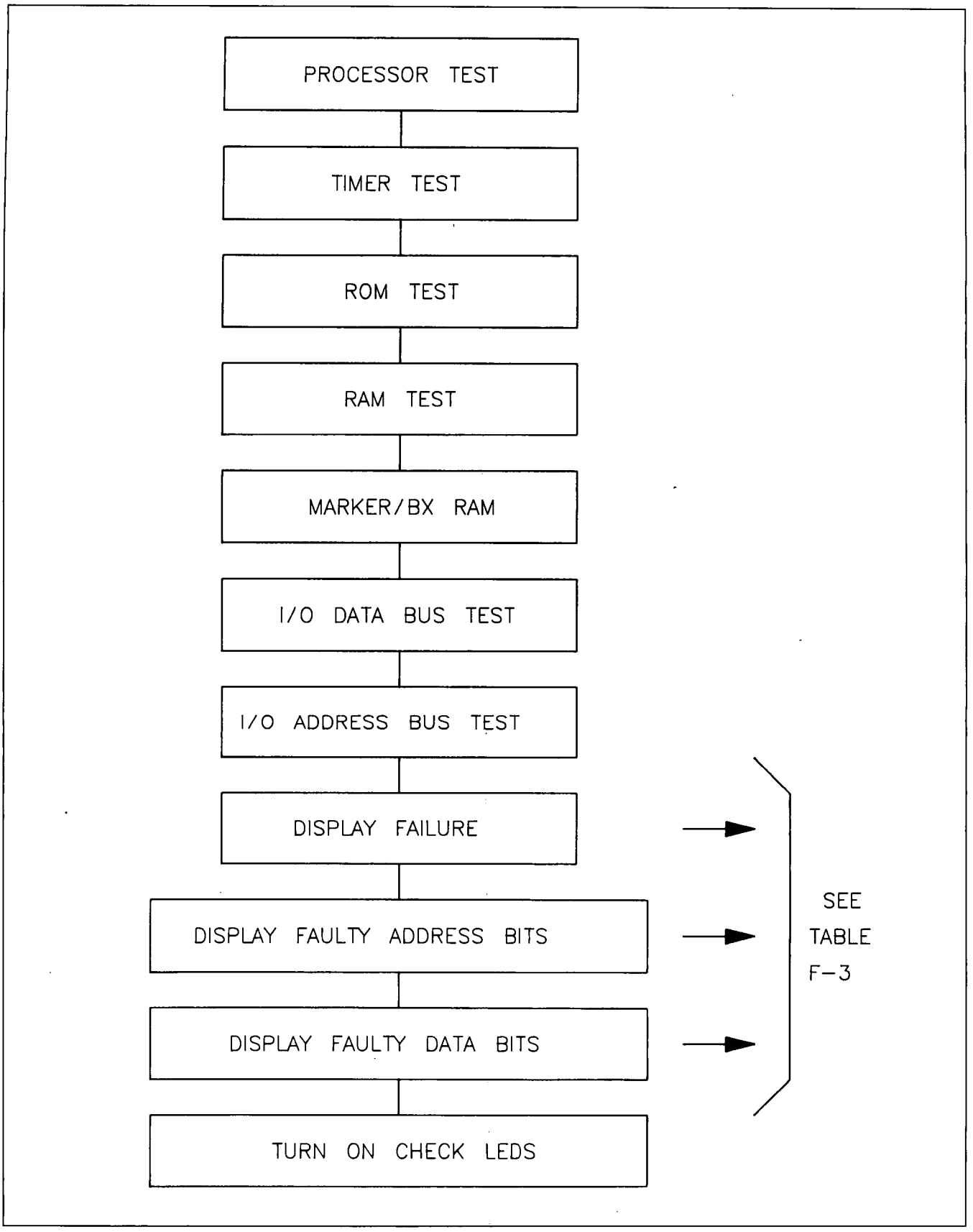


Figure F-2. Self Test Flow Chart

A60 PROCESSOR SELF TEST LEDs

There are 16 self test LEDs at the top of the A60 assembly that turn on when you switch the power on or press **[INSTR PRESET]**. If there is no failure, all 16 LEDs light and approximately 1 second later, turn off.

1. If self test fails, cycle the line power or press **[INSTR PRESET]** and observe the processor self test LEDs.

   All 16 LEDs turn on.

After 2 seconds:

A60DS15 and A60DS16 (the LEDs closest to the front panel) turn off.

A60DS1 through A60DS14 indicate the failure (see Table F-3).

After 4 seconds:

A60DS9 through A60DS15 turn off and A60DS16 turns on.

A60DS1 through A60DS8 then indicate which I/O address bus line failed (see Table F-3).

After 6 seconds:

If an I/O data bus line fails, A60DS1 through A60DS16 indicate which failed (see Table F-3).

Table F-3. A60 Self Test LEDs — Failure Indications

A60 Processor Self Test LEDs (Time After Power On or [INSTR PRESET])				
A60 Processor LED	First 2 Seconds		Second 2 Seconds	Afterward
	SHIFT M4 Test #	Test Name	I/O Address Bus Test	I/O Data Bus Test
DS1	0	PROCESSOR	ADR0	DB0
DS2	1	ROM U37	ADR1	DB1
DS3	2	ROM U36	ADR2	DB2
DS4	3	ROM U35	ADR3	DB3
DS5	4	ROM U34	ADR4	DB4
DS6	5	RAM U39	SIOA	DB5
DS7	6	RAM U38	SIOB	DB6
DS8	7	EEPROM U33	SIOA	DB7
DS9	8	EEPROM U32	OFF	DB8
DS10	9	MKR BX RAM	OFF	DB9
DS11	10	TMR LEDS U4	OFF	DB10
DS12	11	TMR U4	OFF	DB11
DS13	12	I/O ADRS	OFF	DB12
DS14	13	I/O DATA	OFF	DB13
DS15		OFF	OFF	DB14
DS16		OFF	ON	DB15

SHIFT M4

When to Use SHIFT M4

After you have determined the failure mode (using the processor self test LEDs and Table F-3), you can use the SHIFT M4 diagnostic to further isolate the failure. This service diagnostic tests DACs and control circuitry in the instrument, and allows the results of the self test to be displayed in the front panel ENTRY DISPLAY.

What SHIFT M4 Does

SHIFT M4 does not perform exhaustive DAC tests, but provides an indication to direct your troubleshooting to a specific device or circuit path.

Table F-4 lists all the tests performed when you press **[SHIFT] [M4]**. As you can see, this service diagnostic tests more than just the A60 assembly. All of the tests are listed because only one test (0) is not dependent on the test results of one or more of the other tests.

The Interdependence of the SHIFT M4 Tests

Table F-5 illustrates the interdependence of the SHIFT M4 tests. The vertical axis (Test Number) lists the tests, 0 through 31. The horizontal axis (Dependent On) lists the test numbers and indicates which test(s) must pass for a given test result to be valid. An **X** in a Dependent On column indicates that a given test is valid only if the test in that column also passes.

Example:

Test 11 is only valid if tests 0, 5, and 6 pass. If test 11 fails, verify that tests 0, 5, and 6 have passed **before** troubleshooting the assembly exercised in test 11.

SHIFT M4 Test Procedure

1. Press **[SHIFT] [M4]**.

   While the tests are running, the ENTRY DISPLAY shows **DIAGNOSTIC TESTS IN PROGRESS**.

   When the tests are through, the instrument displays **TEST:?FULL DIAGNOSTIC** and then displays **PASS** or **FAIL**. PASS indicates that all of the tests related to this diagnostic have passed. FAIL indicates that one or more of the tests failed.

2. If the display indicates FAIL, use the RPG or the step keys to move through the test results and determine which test(s) failed.

Table F-4. Diagnostic SHIFT M4 Tests (1 of 2)

Number	Name	Description
0	PROCESSOR TST	Verifies the operation of the A60 assembly processor, the Free Run DSA, the processor's data and address bus, and a portion of the UV-EROM.
1	ROM 1 CKSUM	Verifies the operation (checksum) of the UVPROM.
2	ROM 2 CKSUM	Verifies the operation (checksum) of the UVPROM.
3	ROM 3 CKSUM	Verifies the operation (checksum) of the UVPROM.
4	ROM 4 CKSUM	Verifies the operation (checksum) of the UVPROM.
5	RAM 1 RD/WR	Verifies the operation (read/write) of the RAM.
6	RAM 2 RD/WR	Verifies the operation (read/write) of the RAM.
7	EEROM 1 RD/WR	Verifies the operation (read/write) of the EEPROM, and a portion of A69U29. Note that this test is only performed if A60TP1 RAM is grounded.
8	EEROM 2 RD/WR	Verifies the operation (read/write) of the EEPROM and a portion of A60U29. Note that this test is only performed if A60TP1 RAM is grounded.
9	MKR RAM RD/WR	Verifies the operation (read/write) of the Address Register, the Sweep Event Memory, the Read/Write RAM Buffer, and the Microprocessor Read/ Write Strobes.
10	PIT (LED Registers)	Verifies the operation of the timer/self test section.
11	PIT RESPONDS	Verifies the operation of the timer/self test section.
12	I/O ADDR BUS	Verifies the operation of the I/O address Bus, the I/O Address bus, and a portion of the I/O Decoding and Control.
13	I/O DATA BUS	Verifies the operation of the I/O Data Bus Buffers, the I/O Data Bus, and a portion of the I/O Decoding and Control.
14	A-D CONVERTER	Verifies the operation of the A27 assembly ADC Control Latch, the ADC Clock/Control, the ADC Input Multiplexer, the Test ADC, the ADC Window Comparator, the Conversion Complete Timer/SRQ Latch, and the Status Buffer. The Address Decoding is partially verified.
15	LEVEL REF DAC	Verifies the operation of the A27 assembly ALC Reference Generator and a portion of Address Decoding. Monitors LVL to determine the test results.
16	MAN SWP DAC	Verifies the operation of the A57 assembly Manual Sweep Dac and a portion of the Microprocessor And Read Write Strobes. Monitors LVL SWP to determine the test results.
17	MARKER RAMP	Verifies the operation of the A58 assembly. Monitors BVSWP to determine the test results.
18	RESET DAC	Verifies the operation of the A58 assembly. This test specifically exercises the Reset DAC and monitors BVSWP to determine the test results.

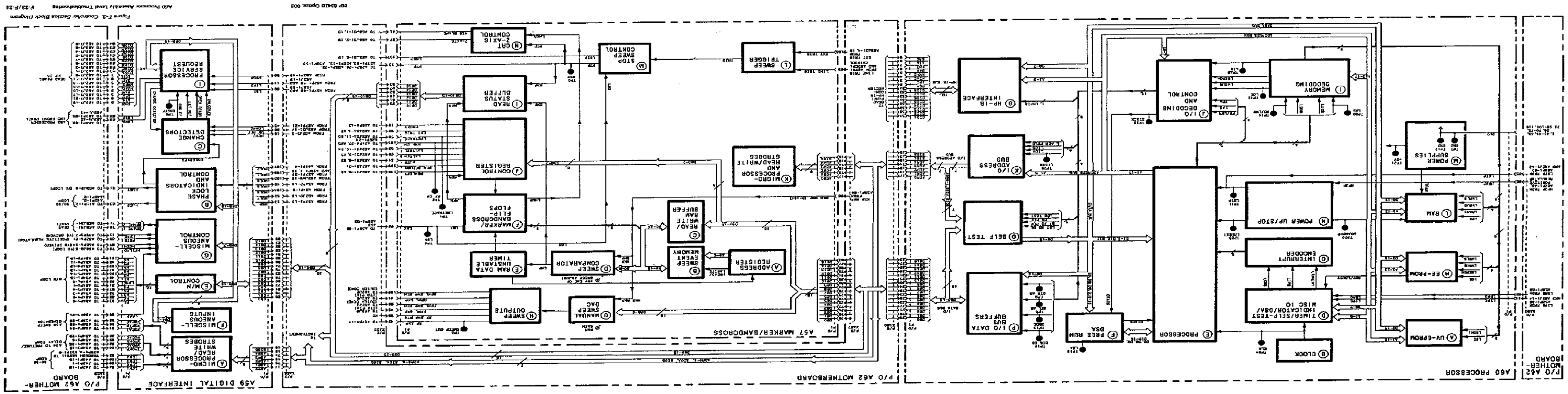
Table F-4. Diagnostic SHIFT M4 Tests (2 of 2)

Number	Name	Description
19	LEVEL SWP DAC	Verifies the operation of the A27 assembly Power Sweep Generator and a portion of Address Decoding. Monitors LVL SWP to determine the test results.
20	BND CROSS DAC	Verifies the operation of the A57 assembly Sweep Comparator. Monitors CMP to determine the test results.
21	SWP WIDTH DAC	Verifies the operation of the A58 assembly. This test specifically exercises the Sweep Width DAC and monitors BVSWP to determine the test results.
22	SWP RANGE ATN	Verifies the operation of the A58 assembly. This test specifically exercises the Sweep Width Register and monitors BVSWP to determine the test results.
23	V/GHz CIRCUIT	Verifies the operation of the A28 assembly −0.25 V/GHz circuitry and a portion of the Programmable Scalar and the Digital Control. Monitors −.25 V/GHz to determine the test results.
24	V/GHz BND ATN	Verifies the operation of the A28 assembly Programmable Scalar. Monitors −.25 V/GHz to determine the test results.
25	BRK PNT 1 DAC	Verifies the operation of the A27 assembly 9 GHz Breakpoint Slope Compensation, the Compensation Summing Amplifier, and a portion of the Address Decoding. Monitors LVL COR to determine the test results.
26	BRK PNT 2 DAC	Verifies the operation of the A27 assembly 20 GHz Breakpoint Slope Compensation, the Compensation Summing Amplifier, and a portion of the Address Decoding. Monitors LVL COR to determine the test results.
27	ATN SLOPE DAC	Verifies the operation of the A27 assembly Attenuator Slope Compensation, the Compensation Summing Amplifier, and a portion of the Address Decoding. Monitors LVL COR to determine the test results.
28	YO PRETUN DAC	Verifies the operation of the A54 assembly Pretune Register, the Pretune DAC, and the Summing Amplifier. Monitors −.25 V/GHz to determine the test results.
29	SWEEPTIME DAC	Verifies the operation of the A58 assembly. This test specifically exercises the Sweep Time DAC and uses the A57 Marker Bandcross assembly and the PIT to determine the test results.
30	NOT USED	
31	A27 INSTALLED	Verifies that the A27 Level Control Assembly is installed.

Table F-5. SHIFT M4 Test Interdependence

Test Number	Dependent On Test Number											
	0	5	6	9	11	12	13	14	15	17	20	31
0												
1	X											
2	X											
3	X											
4	X											
5	X											
6	X											
7	X	X	X									
8	X	X	X									
9	X	X	X			X	X					
10	X	X	X									
11	X	X	X									
12	X	X	X									
13	X	X	X									
14	X	X	X			X	X	X				
15	X	X	X			X	X	X				X
16	X	X	X			X	X	X	X			X
17	X	X	X			X	X	X	X			X
18	X	X	X			X	X	X	X			X
19	X	X	X			X	X	X	X			X
20	X	X	X			X	X	X				X
21	X	X	X			X	X	X	X			X
22	X	X	X			X	X	X	X			X
23	X	X	X			X	X	X	X			X
24	X	X	X			X	X	X	X			X
25	X	X	X			X	X	X	X			X
26	X	X	X			X	X	X	X			X
27	X	X	X			X	X	X	X			X
28	X	X	X			X	X	X	X			X
29	X	X	X	X	X	X	X	X		X	X	X
30												
31	X											

Figure F-3. Controller Section Block Diagram



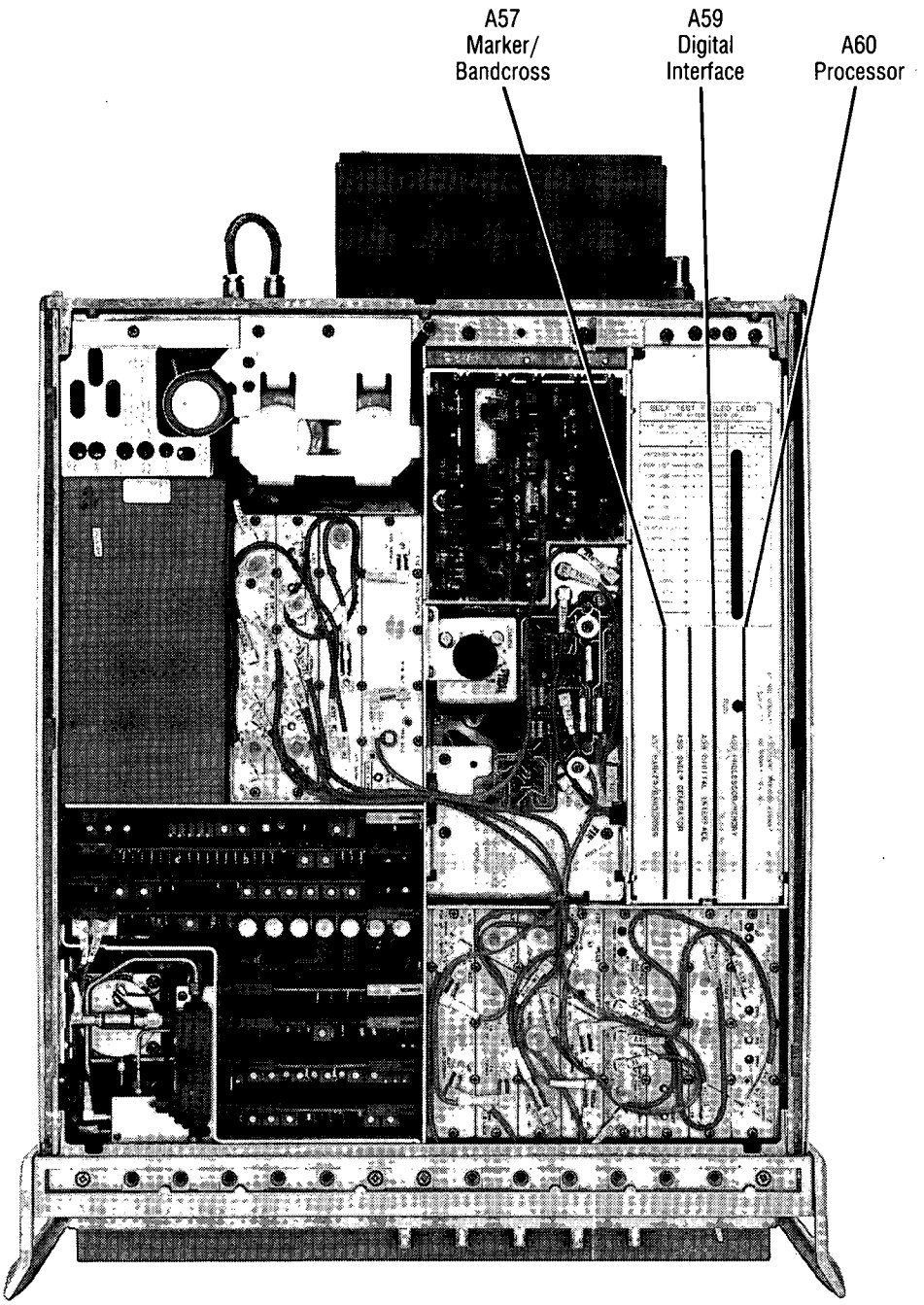


Figure F-4. Controller Section Major Assemblies Location Diagram

Controller Section Repair Procedure

BATTERY REPLACEMENT

What the Battery Does

The processor assembly battery (A60B1) provides backup power to RAM, which holds the working calibration data and the SAVE/RECALL register values.

How Calibration Data is Restored

If the battery is defective, or is replaced, the calibration data and the register values are lost. If RAM does lose its information, the next time you turn the instrument on, protected calibration data stored in EEPROM loads into RAM and the instrument displays **CALIBRATION RESTORED**. Note, however, that register values are not restored.

How Long the Battery Should Last

The battery provides at least two years of back up power, and has a shelf life exceeding 10 years. It is not rechargeable.

WARNING

Although the battery has a strong outer case, do not abuse it mechanically, electrically, or thermally. This battery contains lithium and thionyl chloride ($SOCL_2$) and can be a fire, explosion, and severe burn hazard if abused.

Lithium can burn or explode on contact with moisture.

Thionyl chloride is highly toxic. On contact with air, it partially breaks down into hydrochloric acid and sulfur dioxide fumes, which are toxic, extremely repulsive, strongly irritating, and corrosive to eyes, skin, lungs, and mucous membranes. If a person comes in contact with or breathes this material, CONTACT A POISON CONTROL CENTER OR DOCTOR IMMEDIATELY.

Do not try to charge this battery; it may rupture.

Do not attempt to open the battery, heat it above 212° F (100° C), expose its contents to water, or incinerate it.

Your local laws may require the disposal of thionyl chloride or lithium in a chemical waste disposal site. You can return the battery to: Hewlett-Packard, 1400 Fountaingrove Parkway, Santa Rosa, California 95401, Attention: Environmental Engineering Department.

Dead batteries have converted most of the lithium and thionyl chloride into not-toxic chemicals.

How to Replace the Battery

CAUTION

This assembly contains static sensitive components. Work at a bench equipped with an anti-static surface, and wear a grounding strap that provides a path to earth ground of between 1 and 2.5 MΩ. Always handle a printed circuit board by the edges; never touch the finger contacts.

Do not set the A60 assembly on bare metal; this can short out and cause damage to a good battery.

1. Turn the line switch off and disconnect the instrument power cord. Wait 3 minutes.
2. Remove the A60 processor assembly.
3. Remove the battery and dispose of it properly (see WARNING, above).
4. Check the new battery before installing it; place a 10K ohm resistor across the battery and measure the voltage across the resistor. The voltage should be at least 3.4V (typically 3.6V).
5. If the voltage is correct, install the new battery in the processor assembly.
6. Reinstall the processor assembly in the instrument. Reconnect the power cord, and turn the instrument on. The front panel ENTRY display reads **CALIBRATION RESTORED**.
7. Verify that TP26 (IBATT) is less than 3 mV. A larger voltage indicates excessive battery drain.
8. Replace the top cover.

Controller Section Replaceable Parts

This section provides controller section assembly-level replaceable parts.

Table F-6. Controller Section Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A57	08340-60014	5	1	MARKER/BANDCROSS ASSEMBLY	28480	08340-60014
A59	08340-60226	1	1	DIGITAL INTERFACE ASSEMBLY	28480	08340-60226
A60	08340-60273	8	1	PROCESSOR ASSEMBLY	28480	08340-60273
A60BT1	1420-0331	3	1	BATTERY 2.4V 1.75A-HR LITHIUM THIONYL	28480	1420-0331

Front Panel – Rear Panel Assembly-Level Service

CONTENTS

CONTENTS (Cont'd)

Front Panel – Rear Panel Introduction

The front panel — rear panel functional group contains the user interface to the instrument via the keyboards, displays, and external connections. The front panel contains the keyboards and displays, with a dedicated display processor to update and refresh the displays. The keyboards communicate directly with the instrument processor for normal operation and troubleshooting.

ASSEMBLIES

The front panel — rear panel functional group consists of six assemblies:

- A1 alpha display assembly
- A2 display driver assembly
- A3 display processor assembly
- A5 keyboard assembly
- A6 keyboard interface assembly
- A7 lower keyboard assembly

Front Panel
Theory of Operation

FRONT PANEL MICROPROCESSOR

The front panel assembly contains a microprocessor that is used to refresh the displays. The main instrument microprocessor sends data to the front panel processor via the instrument data bus and instrument address bus. The front panel processor stores the data in an internal RAM (random access memory) buffer. The front panel processor has 2K of internal ROM (read only memory) that contains a program to generate the necessary control signals to display and refresh data.

DISPLAYS

The synthesizer has two types of displays:

- Entry display

  Includes twenty-eight 5 X 7 dot matrix characters, and can display both alpha and numeric data.

- Frequency and power displays

  Seven-segment displays that usually display only numeric data.

The front panel processor determines the segments and/or dots to be illuminated and outputs the appropriate digital signals to the appropriate circuitry, continually refreshing the displays.

LED ANNUNCIATORS

The main instrument microprocessor controls the LED annunciators via the instrument data bus and instrument address bus.

KEYBOARDS

The two keyboard assemblies (A5 and A7), and the RPG (rotary pulse generator) communicate with the main instrument microprocessor via the A6 keyboard interface assembly. Pressing a key generates an active low column signal and an active low row signal that are encoded by the keyboard interface assembly. A service request is generated to the main instrument microprocessor, which reads the encoded signal via the instrument data bus.

RPG

Rotating the RPG (rotary pulse generator) increments or decrements a counter, and generates a service request, with the main instrument microprocessor reading the counter output.

POWER STANDBY/ON SWITCH

The front panel power standby/on switch is an open circuit in the on position. In standby, a ground is supplied to the yellow standby LED, and to the fan relay. This ground is also LSBY (low standby).

In standby, the fan relay is energized, and the power to the fan is removed. The LSBY signal is fed to the +20V regulator, which shuts down the +20V supply. Because the +20V supply is a reference for all other regulated supplies, all regulated supplies are shut down as well. In the standby mode, line power is still applied to the power transformer primary and to the unregulated supplies.

A1 ALPHA DISPLAY ASSEMBLY

The A1 alpha display assembly provides the physical mounting for the seven 4-character dot matrix display elements. The assembly is mounted on the front panel bezel, and interfaces to the A2 display driver assembly via a multi-pin connector.

A2 DISPLAY DRIVER ASSEMBLY

The A2 display driver assembly contains the 7-segment displays and the instrument annunciators, and it provides an interface with the A1 alpha display assembly.

A3 DISPLAY PROCESSOR ASSEMBLY

The A3 display processor assembly provides the communication link for interfacing the main instrument microprocessor to the instrument displays. The instrument microprocessor sends display data to the A3 display processor via the instrument data and address busses. The A3 display processor stores the data in internal RAM (random access memory), and processes the data into the necessary control signals to display the information. The display processor has 2K of internal ROM (read only memory) that contains the program for display control.

The A3 display processor assembly outputs control signals to the A2 display driver assembly for the power/frequency 7-segment displays, the entry display 5X7 dot matrix displays, and the instrument LED annunciators.

A5 KEYBOARD ASSEMBLY AND A7 LOWER KEYBOARD ASSEMBLY

The A5 keyboard and the A7 lower keyboard assemblies provide the mechanical mounting for all instrument key assemblies. The key annunciators are also located on these assemblies. The keyboard assemblies communicate with the instrument microprocessor via the A6 keyboard interface assembly.

A6 KEYBOARD INTERFACE ASSEMBLY

The A6 keyboard interface assembly provides the communications link between the instrument microprocessor, the front panel rotary pulse generator (RPG), and A5 and A7 keyboards. The interface contains all data buffers, annunciator latches, and interrupt circuitry to monitor the front panel keyboards and annunciators. RPG control circuitry (counters/timers) and the instrument preset circuitry are also located on the A6 assembly.

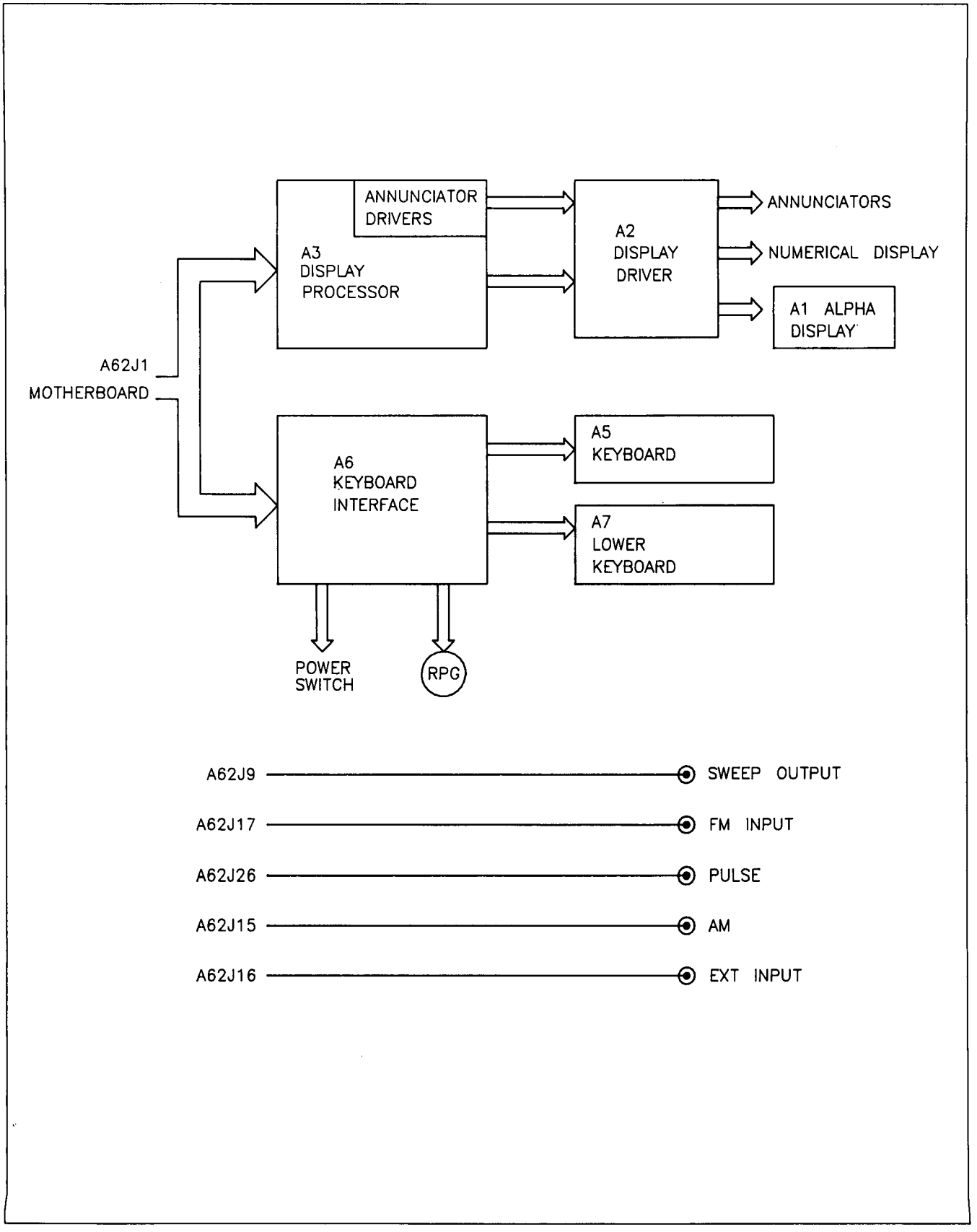


Figure G-1. Front Panel Simplified Block Diagram

Front Panel
Overall Assembly-Level Troubleshooting

INSTRUMENT PRESET

1. Disconnect **all** cables from the SOURCE.
2. To cycle the power, turn the power switch to standby, wait several minutes for all power supply capacitors to discharge, and turn the power switch to on.
3. Press **[INSTR PRESET]** and compare the instrument configuration with the following:

Start Frequency:	10 MHz
Stop Frequency:	20.0 GHz
Power Level:	0.0 dBm (factory set value) Can be changed with calibration constant 56.
Sweep Time:	AUTO (33.316; press **[SWEEP TIME]** to verify)
Sweep:	CONT
Trigger:	FREE RUN
RF:	On
Leveling:	INT
INSTR CHECK LEDs:	Off

Either or Both INSTR CHECK LEDS are On

If either or both of the INSTR CHECK LEDs stay on after power on or an instrument preset, refer to the overall instrument troubleshooting in the service introduction of this manual.

Front Panel Diagnostic Mode Activates

If, at power on, the front panel goes into the front panel diagnostic mode (the same as pressing **[SHIFT] [FREE RUN]**), suspect the main instrument processor.

At power on, the instrument microprocessor should initiate a self test. One of the first things the self test does is send data to the front panel processor. If the front panel processor does not receive the data from the instrument microprocessor, it automatically goes into the diagnostic mode.

All Front Panel LEDs are On

If, at power on, all front panel LEDs are on (similar to holding **[INSTR PRESET]**), check the negative power supplies. The main instrument processor requires both the positive and negative supplies (and will suspend instrument functions if one is inoperative). The front panel LEDs require only the positive supplies.

LED AND ANNUNCIATOR TEST

1. Turn the power switch to on.
2. Press and hold **[INSTR PRESET]**.

3. All LEDs and annunciators should light and remain on as long as you press **[INSTR PRESET]**.
4. If any LED or annunciator fails to light, use Figure G-2 to identify the appropriate assembly.

ALPHANUMERIC DISPLAY TEST

1. To activate the display self test diagnostic mode, press **[SHIFT] [FREE RUN]**.
2. You should see the following:
   a. For three seconds, the ENTRY display shows **DISPLAY RAM TEST PASSED**.
   b. For the next three seconds, the ENTRY display shows **DISPLAY CHECKSUM = 3A**.
   c. For six seconds, all numeric display segments light, and all ENTRY display dots flash.
   d. The entire available character set scrolls across the displays, and continues to scroll until the diagnostic routine is terminated with **[SHIFT] [M5]**.
3. If you note any discrepancies, refer to the A1, A2, and A3 assembly-level troubleshooting procedures.

KEY AND RPG TEST

1. With the power switch set to STANDBY (no fan noise), check the mechanical action of each key.

   Check for height differences, unusual sounds when pressed, and differences in the force required to depress each key.
2. Check that the front panel knob rotates smoothly.
3. Turn the power switch on and press each front panel key. Check for the proper ENTRY display message, and that the appropriate LEDs and annunciators light.

NOTE: Some keys require that other keys are pressed first (e.g. the GHz and dBm terminators).

4. Press **[INSTR PRESET] [POWER LEVEL]** and slowly rotate the front panel knob in both directions. Watch for a 0.05 dB increment (clockwise) and decrement (counter-clockwise) in the power level.
5. Rotate the front panel knob rapidly one quarter turn in either direction. This should cause a large change in power level.
6. If a keyboard has a problem, disassemble the front panel (refer to **FRONT PANEL REPAIR PROCEDURES**), and refer to either the A3 processor troubleshooting or the A5 and A7 keyboard troubleshooting.

FRONT PANEL CONNECTORS

1. Examine all connectors for contamination or deformation.

A3 Display Processor Assembly-Level Troubleshooting

EQUIPMENT REQUIRED

Oscilloscope ..... 100 MHz

PROCEDURE

1. Connect the oscilloscope ground to GROUND (TP10) and check the −5.2V (TP11), +5.2V (TP13) and +12V (TP14) supplies for proper voltages.
2. If the supplies are correct, refer to Figure G-4 and remove the front panel, separate the display assembly from the keyboard, and reattach the keyboard to the frame.
3. Remove eight screws from the display assembly that hold the A3 display processor. Turn the display processor over and reinsert the other end of P1 through P5 into the same sockets they came out of. Install two screws to hold it in place.
4. To place the display into the self-test mode, press **[SHIFT] [FREE RUN]**.

Display RAM Test Fails

Replace A3U1.

Display Checksum is Not Equal to 3A

The display checksum is shown in the ENTRY display during the front panel diagnostics. Press **[SHIFT] [FREE RUN]** and determine if the checksum is equal to 3A. If not, replace A3U1.

Numeric And ENTRY Displays Are Dim

Using an oscilloscope, check the display supply voltage (A3P5 pin 1,2). This voltage should be 4.0V with 430 Hz 0.6V P-P ripple. If this voltage is low (< 3.2V), the displays are likely to be dim; if this voltage is less than about 2.0V the displays will be blank. If this voltage is not correct, the trouble is in the A3 display supply.

Both Numeric and ENTRY Displays are Blank

1. Check LRESET (A3TP12) and CLR (A3P1 pin 1). If either is low, the trouble is in the A3 preset circuitry.
2. Using an oscilloscope, check the display supply voltage (A3P5 pin 1). This voltage should be 4.0V with 430 Hz 0.6V P-P ripple. If this voltage is low (< 3.2V), the displays are likely to be dim; if this voltage is less than 2.0V the displays will be blank. If this voltage is not correct, the trouble is in the A3 display supply.
3. If both LRESET and CLR are high, and the display supply voltage is 4.0V or greater, proceed to **All Numeric Displays are Blank**, and **ENTRY Display is Blank** troubleshooting procedures.

All Numeric Displays are Blank

1. Connect the oscilloscope to the CLK test point (A2TP6), and set it to 0.5 μs/div, 1 V/div (0V = center screen). The waveform displayed should be low for 2.5 to 3.0 μs, with levels between +2V and approximately − 2.5V. If this signal is not present, the trouble is the NUM CLK on the A2 assembly.

2. Troubleshoot the A2 assembly.

Entry Display Is Blank

1. Connect oscilloscope to ALPHA CLK (A2TP2), and set it to 0.5 μS/div, 1V/div (0V=Center screen). The waveform displayed should be TTL low-going pulses, 0.3 μS wide, with a period of 1.4 μs. If this signal is not present, the trouble is the alpha display clock control in the A3 assembly.

2. Connect the oscilloscope to DATA (A2TP1), set as in step 1. The waveform display should indicated both high and low signal levels approximately 1.4 μs wide. If the DATA signal is always low, all LEDs in the ENTRY display will be off. If this signal is not present, the trouble is the A3 assembly alpha display shift register.

3. Troubleshoot the A2 assembly.

The Same Segment(s) is Missing In Each Numeric Digit

Troubleshoot the A2 assembly.

The Same Column is Missing in Each ENTRY DISPLAY Character

Troubleshoot the A2 assembly.

One Entire Numeric Display is Blank

Troubleshoot the A2 assembly.

The Display Goes into Self Test When the Instrument is Turned ON and Does Not Respond to Normal Instrument Functions

The trouble is the A3 instrument bus interface.

A5 Keyboard and A7 Lower Keyboard Assembly-Level Troubleshooting

ANNUNCIATORS

1. If one of the front panel LEDs stays on all the time, the trouble is the A6 annunciator latches.
2. If one of the front panel LEDs never comes on, even when **[INSTR PRESET]** is pressed, the cause is most likely a bad LED.

A6 Keyboard Interface Assembly-Level Troubleshooting

EQUIPMENT REQUIRED

Oscilloscope ..... 100 MHz

PROCEDURE

1. Refer to Figure G-6 and remove the front panel assembly from the instrument.
2. Disconnect the display from the keyboard and reattach the display to the frame.
3. Lay the keyboard down in front of the instrument to allow access to the keyboard interface.

One Or More LEDS Do Not Light When [INSTR PRESET] is Pressed

The trouble is the A6 annunciator latches or the A5/A7 assemblies.

None of the Annunciators Light When [INSTR PRESET] is Pressed

Troubleshoot the A6 instrument preset buffer or annunciator latches.

All of the Annunciators Except SWP Remain On After Power Up or After [INSTR PRESET]

Troubleshoot the A6 address decoder or instrument preset buffer.

Check LED I Or II Remain On After [INSTR PRESET]

The instrument processor self test has failed. Refer to the A60 processor assembly troubleshooting in the controller section functional group.

Pressing a Key Gives No Response (Display Does Not Change and the Instrument State Does Not Change)

With the oscilloscope, probe HI KEY DN SRQ (A6 TP3), at 5 ms/Div. This signal should be low. When you press a key, it should go high for a period of time that is equal to the instrument microprocessor SRQ response time. This varies between 100 µs and 25 ms. If HI KEY DN SRQ is correct, the trouble is the SRQ buffer. If HI KEY DN SRQ is incorrect, the trouble is the key down timer.

Pressing a Key Produces Several of the Same Characters in the Display

Probe LOW KEY DISABLE (A6TP13). This signal should go low and remain low until after the key is released. If LOW KEY DISABLE is working, the trouble is the key down timer. If LOW KEY DISABLE is always high, the trouble is the key up timer.

Sometimes Keystrokes are Missed by the Instrument

The problem is in the A6 key down timer.

The instrument Responds Only to Keystrokes and/or the Front Panel Knob when in a Swept Mode

The problem is in the A6 SRQ buffer.

No Response when the Front Panel Knob is Turned

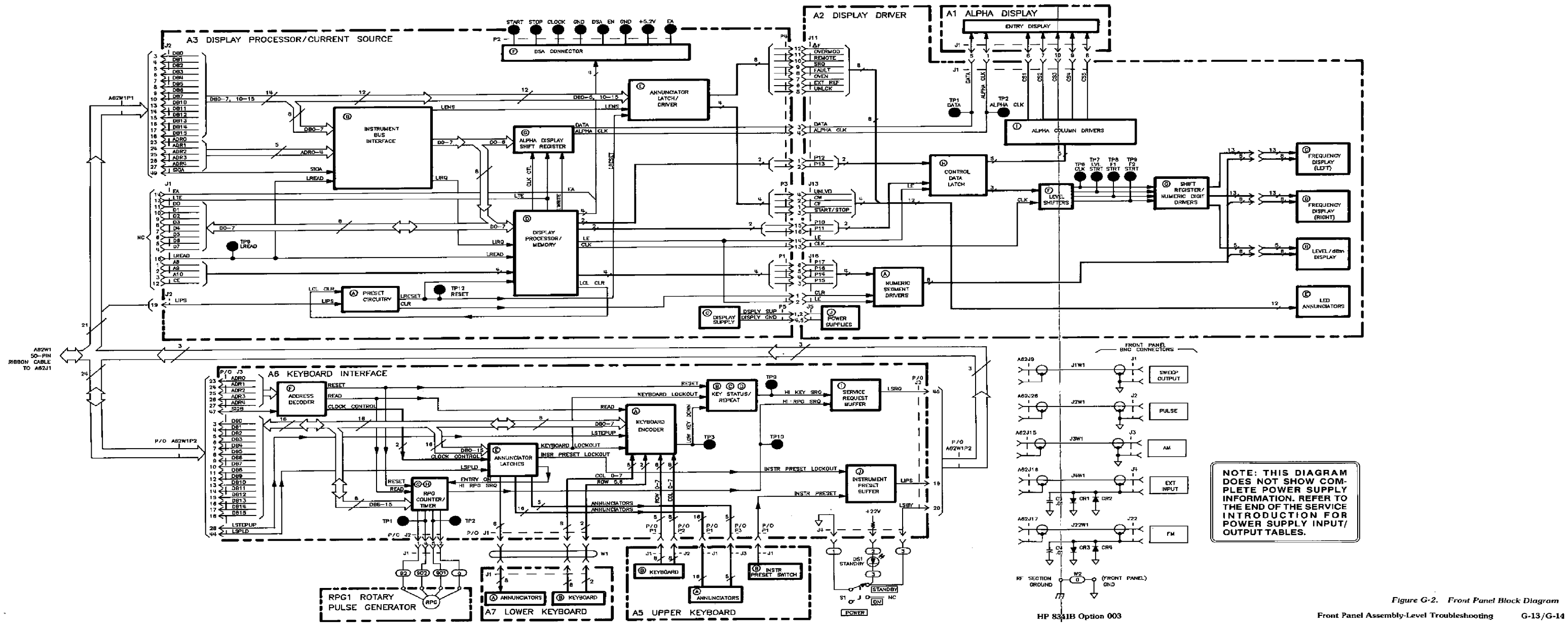
1. Press a function key and verify that the ENTRY ON LED lights. If this LED does not light, the trouble is the annunciator latches.
2. If the ENTRY ON LED is on, probe CLK (A6TP1) with an oscilloscope set to 5 ms/Div. You should see low going pulses as you turn the front panel knob, and the pulse width should vary with the speed of rotation. If CLK is bad, the trouble is in the RPG (rotary pulse generator) or the RPG counters/data buffers.
3. Probe HI RPG SRQ (A6TP8). You should find high going pulses that vary in width depending on the response time of the instrument processor to an SRQ. These pulses should be between 100 µs and 25 ms. If HI RPG SRQ is correct, the trouble is the SRQ buffer or the RPG counters/data buffers. If HI RPG SRQ is not correct, the trouble is the RPG count window timer.

Turning the RPG Causes Either Very Small or Very Large Changes in the Active Function in the ENTRY DISPLAY

The problem is in the A6 RPG count window timer.

The Instrument Does Not Preset when [INSTR PRESET] is Pressed

The problem is in the A6 instrument preset buffer.



NOTE: THIS DIAGRAM DOES NOT SHOW COMPLETE POWER SUPPLY INFORMATION. REFER TO THE END OF THE SERVICE INTRODUCTION FOR POWER SUPPLY INPUT/ OUTPUT TABLES.

Figure G-2. Front Panel Block Diagram

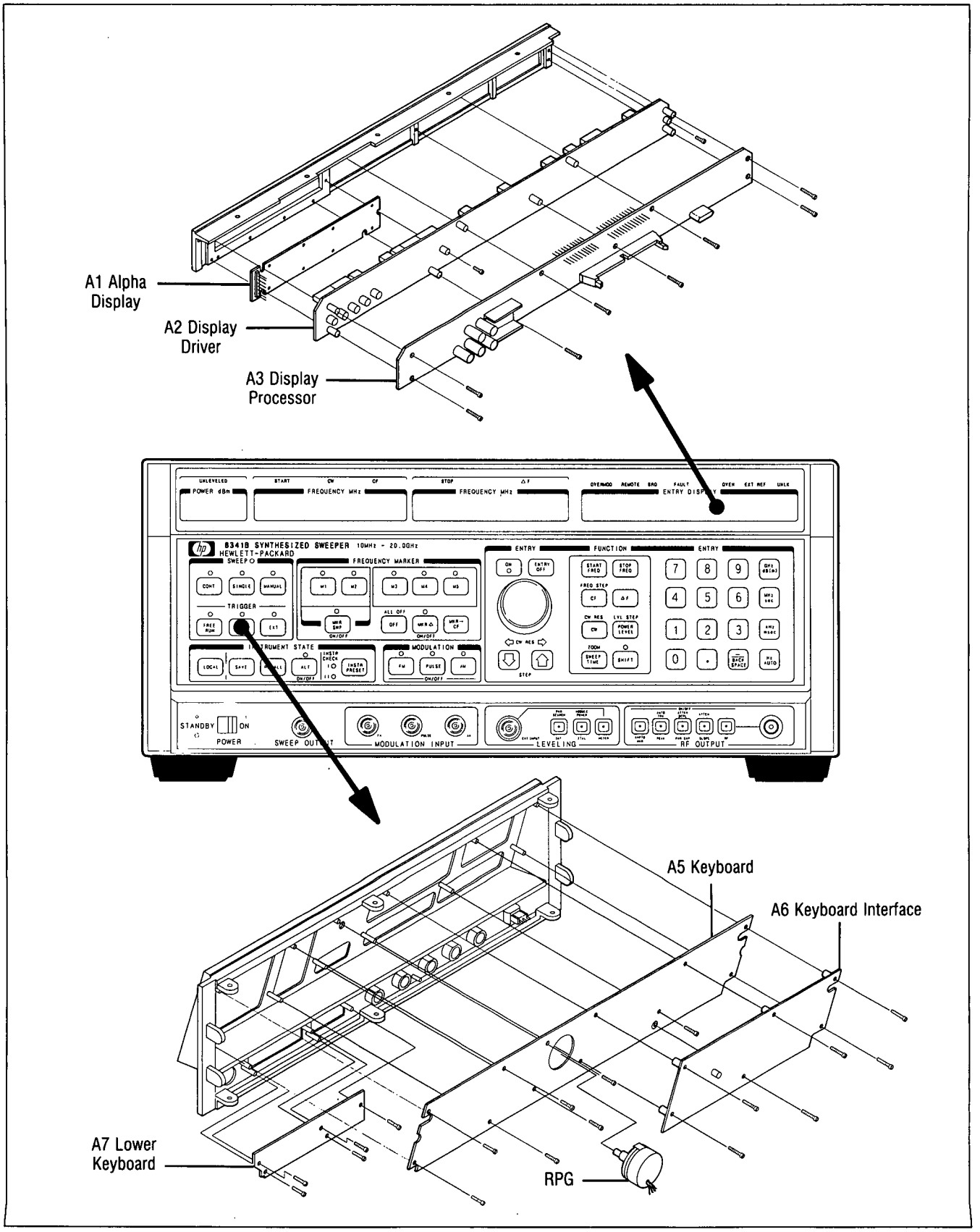


Figure G-3. Front Panel Major Assemblies Location Diagram

Front Panel
Repair Procedures

FRONT PANEL DISASSEMBLY

Figure G-4 illustrates the following procedure.

1. Disconnect the AC power line cord.
2. Remove the instrument top cover.
3. Remove the vinyl trim from the top, front edge of the instrument (pry a corner loose and gently peel the trim from the bezel).
4. Remove all five screws under the trim.

NOTE: The length of these five screws is important (see **REPLACEABLE PARTS**). Longer screws protrude through the display casting and can damage the display driver assembly.

5. Remove either front foot (instructions are on the foot) to release the information cards tray, and remove the tray.
6. Remove three of the five screws on the lower, front frame edge (see Figure G-4), and loosen a fourth, if necessary.

NOTE: The loosened screw centers the RF connector in the front panel opening. Be sure the connector is recentered and secured during front panel reassembly.

7. Gently pry the front panel and display assembly from the frame. You may have to apply pressure from behind, against the display assembly.
8. If you intend to remove the entire front panel, you must disconnect the five coaxial cables that connect the front panel BNC connectors to the motherboard SMB connectors, and the two 50-wire ribbon cables.

   If you intend to only troubleshoot the display and/or keyboard assemblies, you must disconnect only the ribbon cable attached to the display assembly.
9. Separate the keyboard assembly from the display assembly by removing the three screws between the panel castings.
10. To troubleshoot the keyboard, reconnect the ribbon cables and attach the display to the top of the front casting for support.
11. To troubleshoot the display, configure the display assemblies in the service position (Figure G-6), reconnect the ribbon cables, lay the display assembly on the reinstalled top cover, and attach the keyboard to the front panel for support.

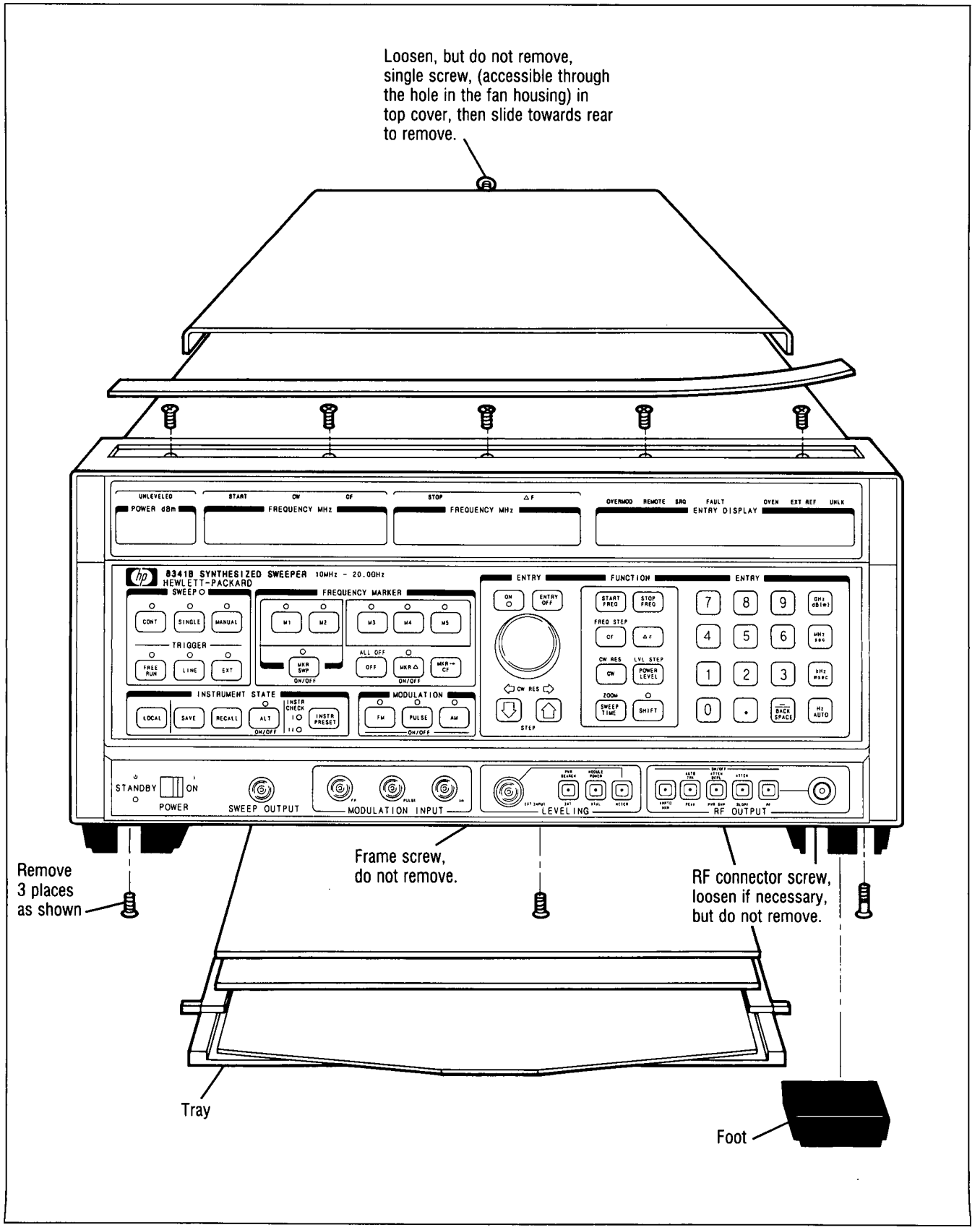


Figure G-4. Front Panel Disassembly

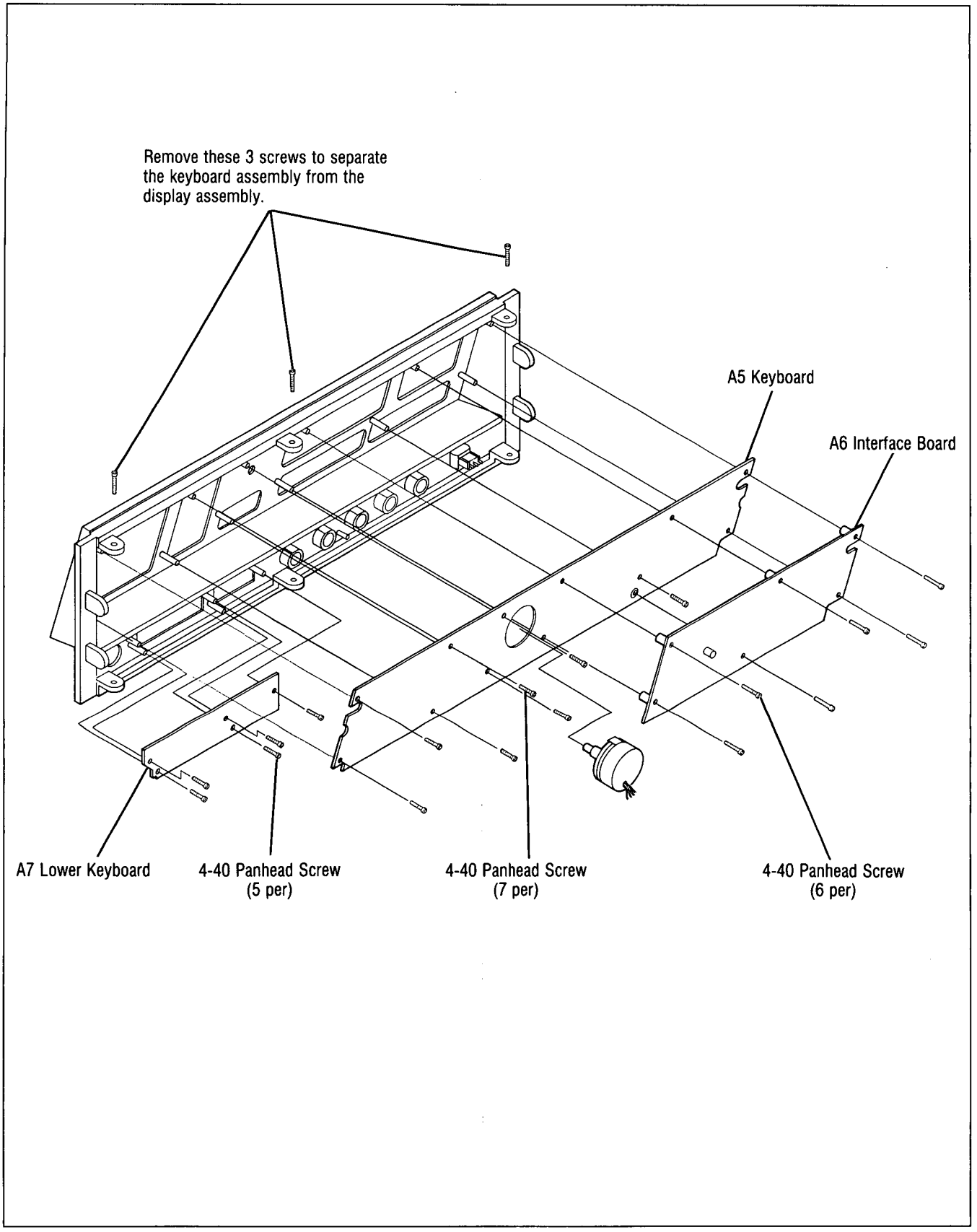


Figure G-5. A5, A6, A7 Disassembly

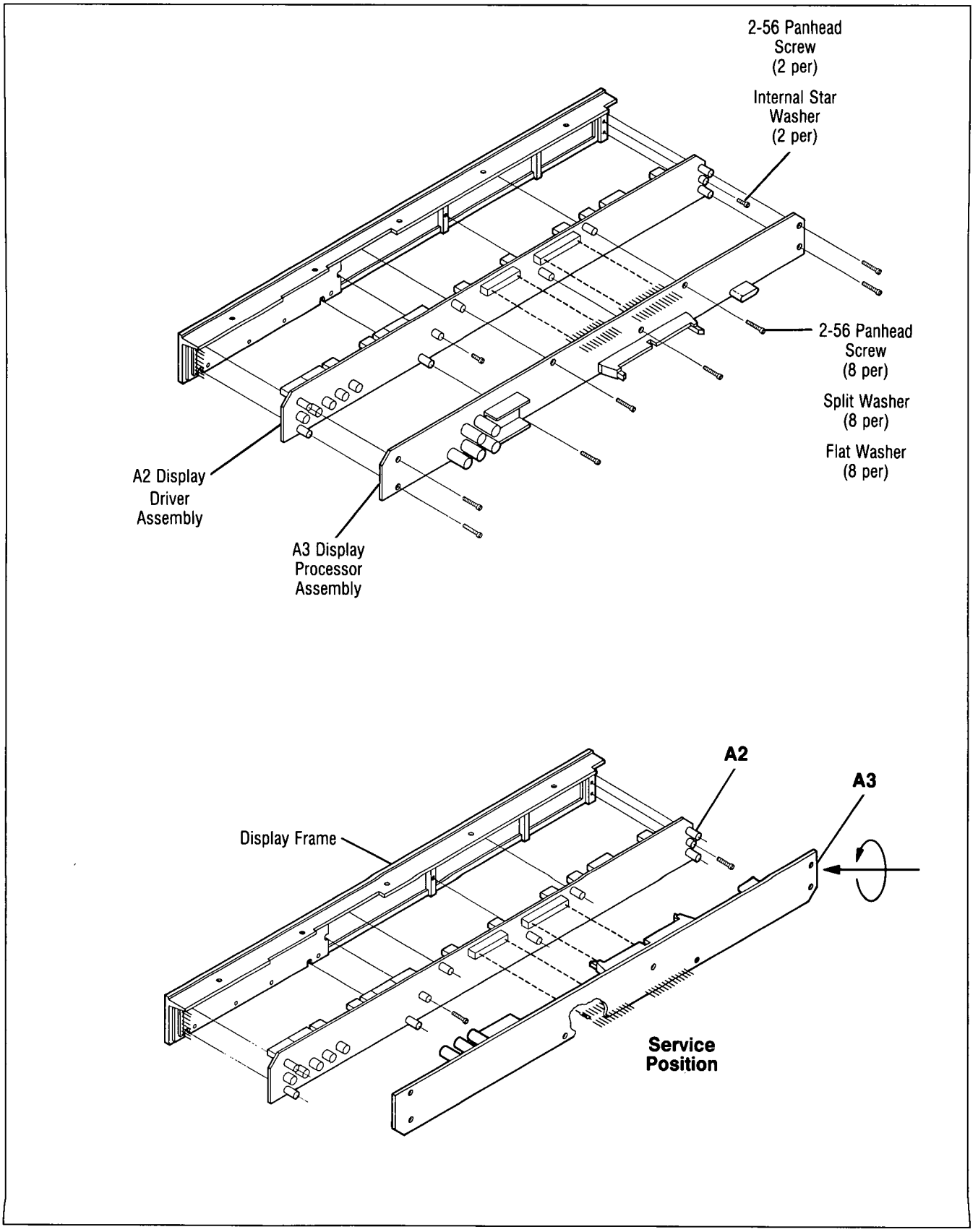


Figure G-6. A2, A3 Disassembly

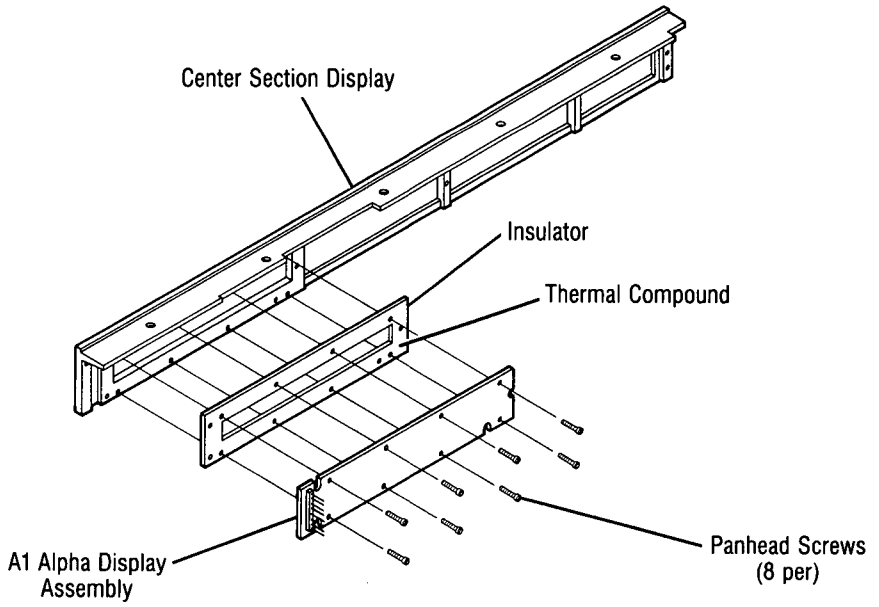


Figure G-7. A1 Disassembly

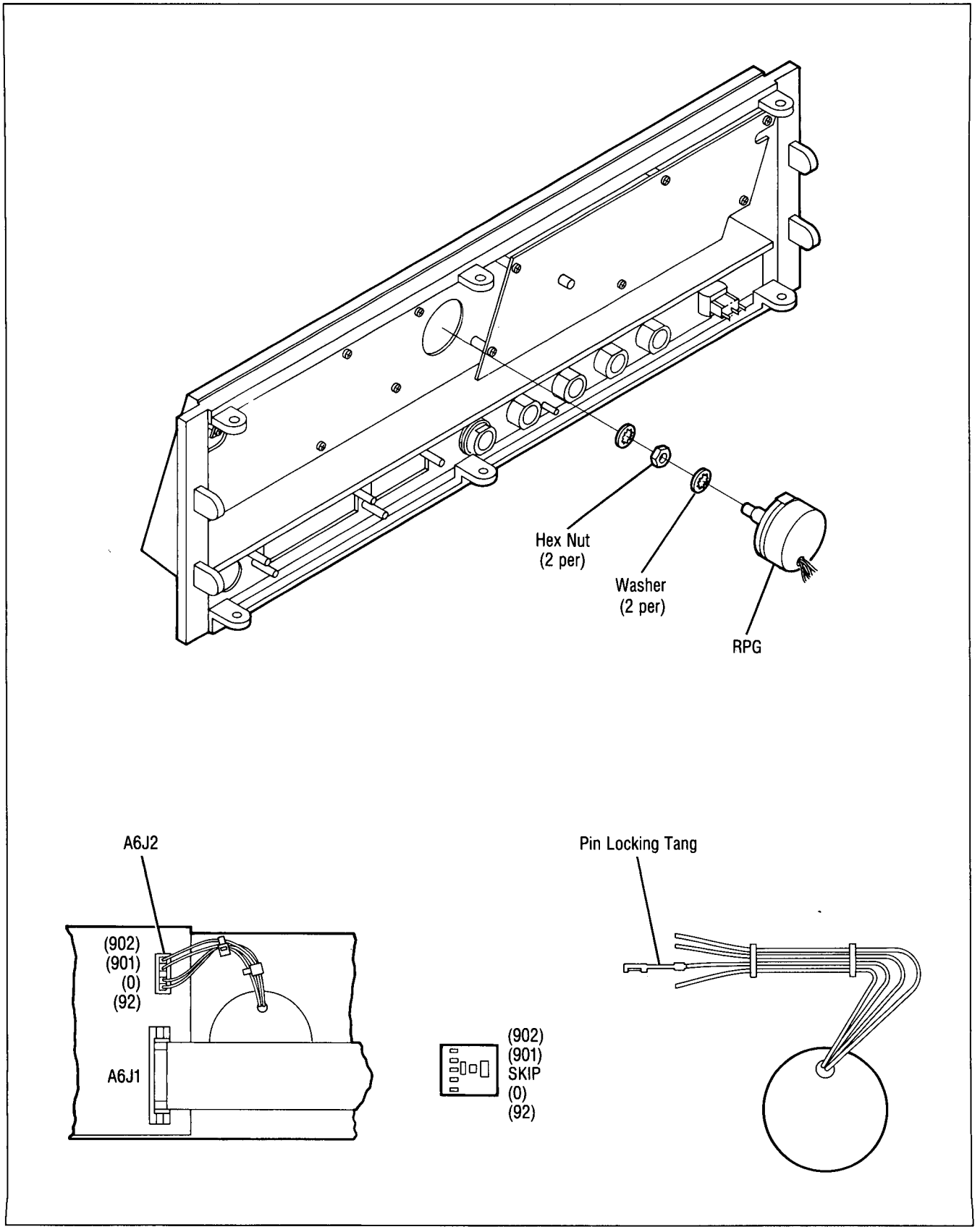


Figure G-8. RPG Disassembly

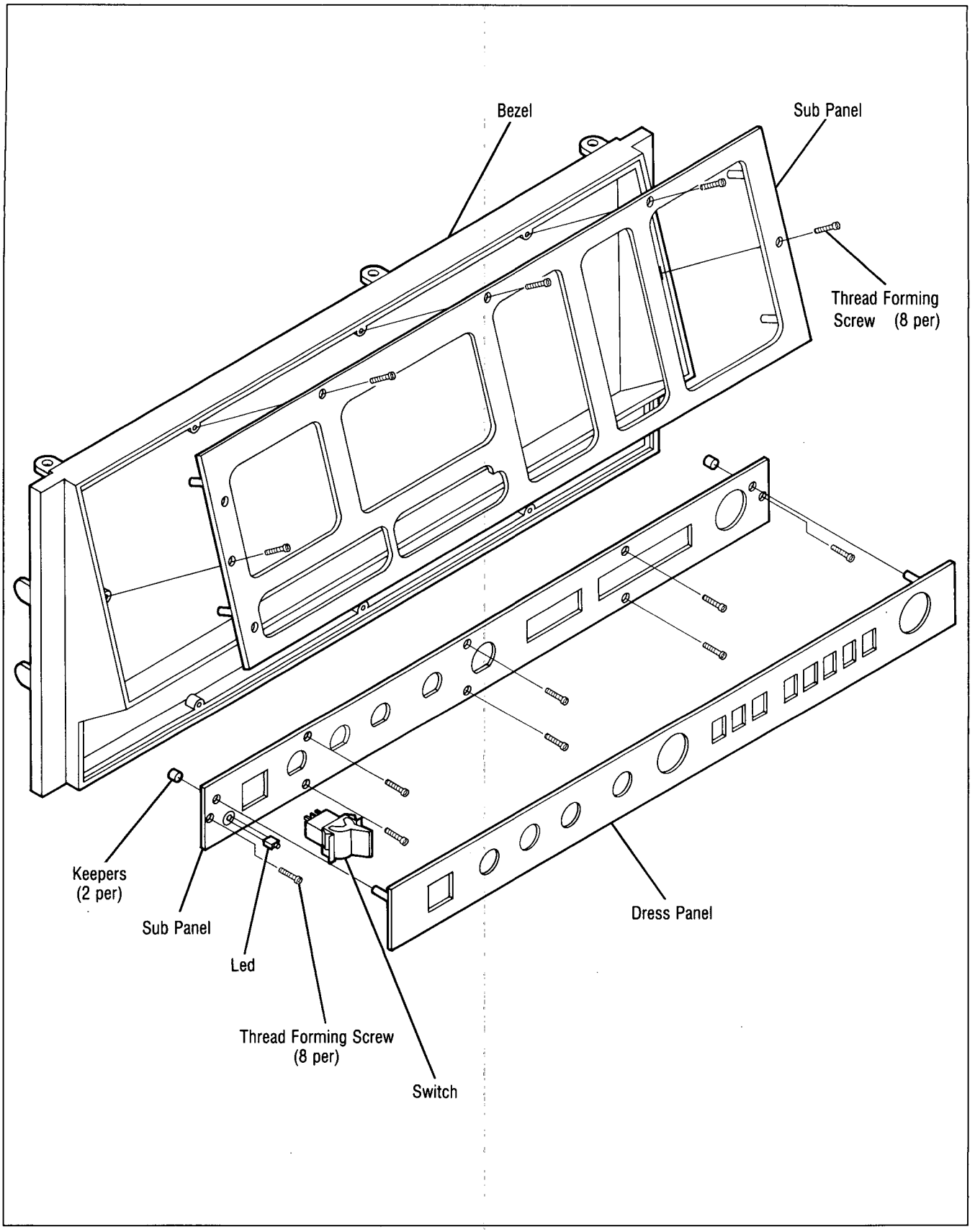


Figure G-9. Panels, Switch, and Connectors Disassembly (1 of 3)

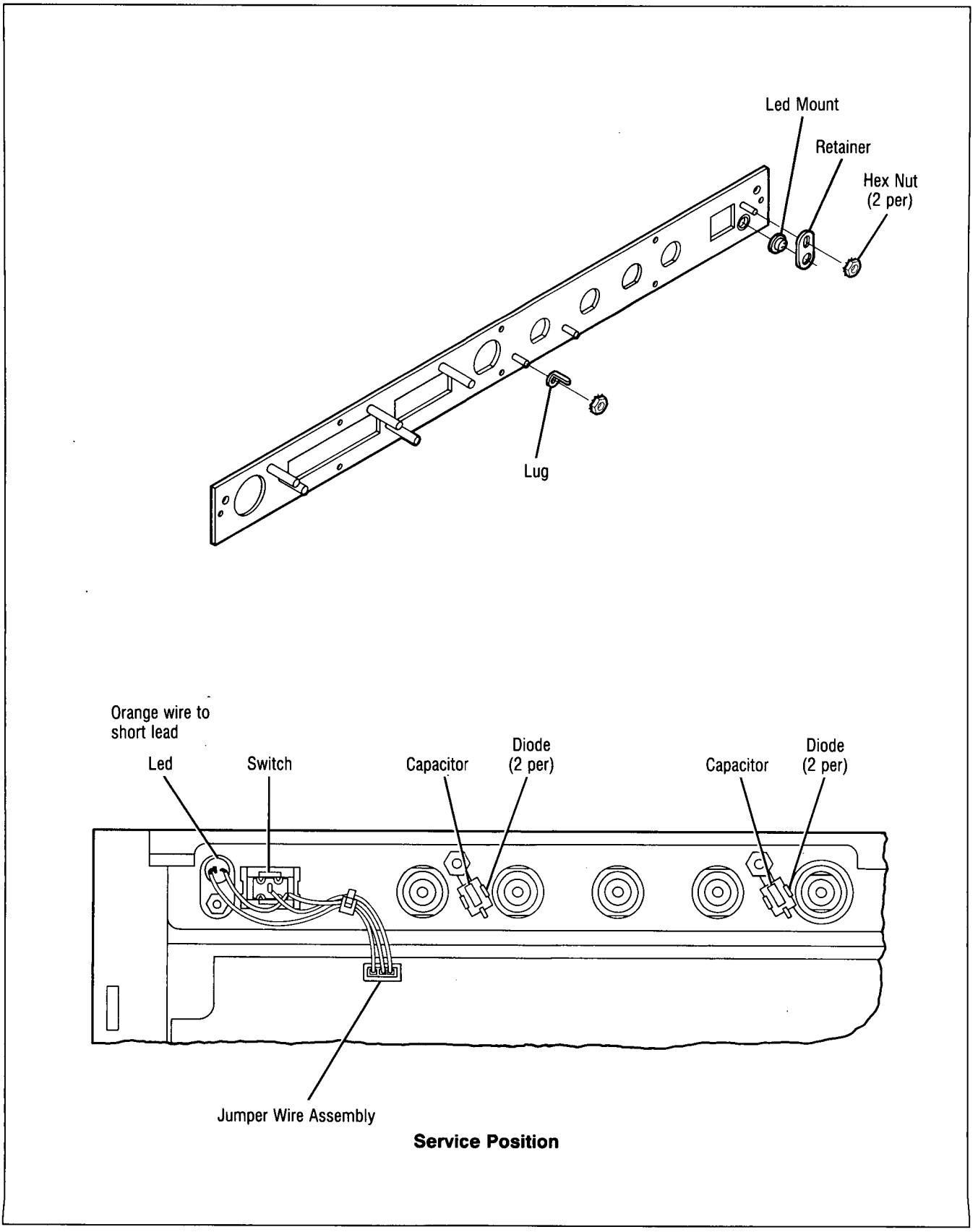


Figure G-9. Panels, Switch, and Connectors Disassembly (2 of 3)

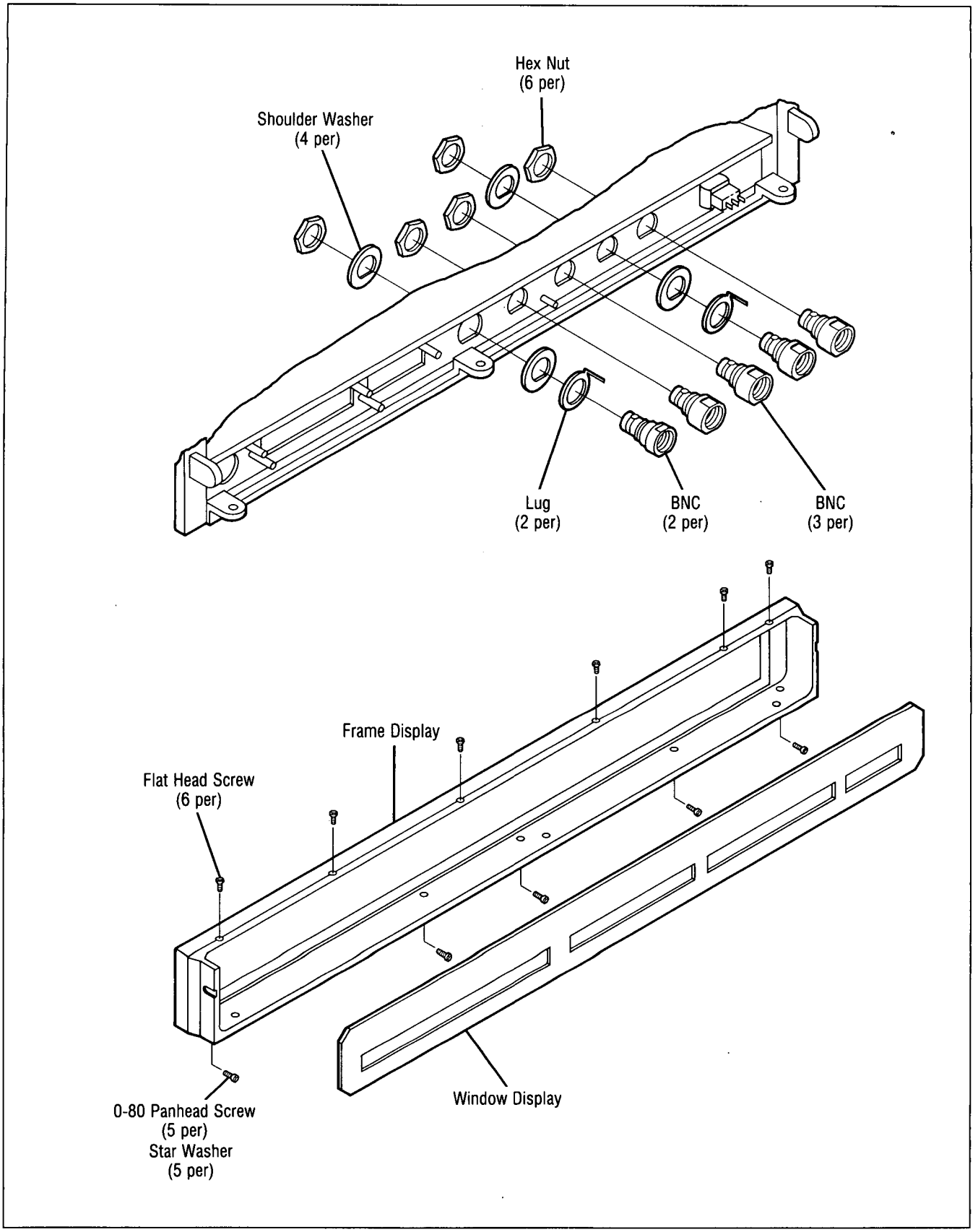


Figure G-9. Panels, Switch, and Connectors Disassembly (3 of 3)

Front Panel
Replaceable Parts

This section provides provide front panel assembly-level replaceable parts information.

Table G-1. Front Panel Attaching Hardware

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
1	0360-0005	9	1	TERMINAL-SLDR LUG PL-MTG FOR-#8-SCR	28480	0360-0005
2	0510-1148	2	2	RETAINER-PUSH ON KB-TO-SHFT EXT	28480	0510-1148
3	0624-0264	2	16	SCREW-TPG 4-40 .312-IN-LG 82 DEG	00000	ORDER BY DESCRIPTION
4	1400-0249	0	2	CABLE TIE .062-.625-DIA .091-WD NYL	06383	PLT1M-8
5	2190-0016	3	2	WASHER-LK INTL T 3/8 IN .377-IN-ID	28480	2190-0016
6	2200-0105	4	7	SCREW-MACH 4-40 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
7	2200-0113	4	5	SCREW-MACH 4-40 .625-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
8	2200-0115	6	6	SCREW-MACH 4-40 .75-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
9	2260-0009	3	2	NUT-HEX-W/LKWR 4-40-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
10	2950-0043	8	2	NUT-HEX-DBL-CHAM 3/8-32-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
11	08340-00086	5	1	DRESS PANEL KEYBOARD (8340B)	28480	08340-00086
	08341-00004	8	1	DRESS PANEL KEYBOARD (8341B)	28480	08341-00004
12	08340-00025	2	1	DRESS PANEL LOWER KEYBOARD	28480	08340-00025
13	08340-00026	3	1	SUB-PANEL LOWER KEYBOARD	28480	08340-00026
14	08340-20078	7	1	BEZEL-KEYBOARD FINISHED	28480	08340-20078
15	1450-0615	9	1	RETAINER	28480	1450-0615
16	08340-40002	9	1	LED MOUNT	28480	08340-40002
17	0370-2992	8	1	KNOB-BASE 1-1/8 JGK .252-IN-ID	28480	0370-2992
18	0590-1251	6	4	NUT-SPCLY 15/32-32-THD .1-IN-THK .562-W	28480	0590-1251
19	00310-48801	0	2	WASHER SHOULDER	28480	00310-48801
20	0360-1158	5	1	LUG	28480	0360-1158

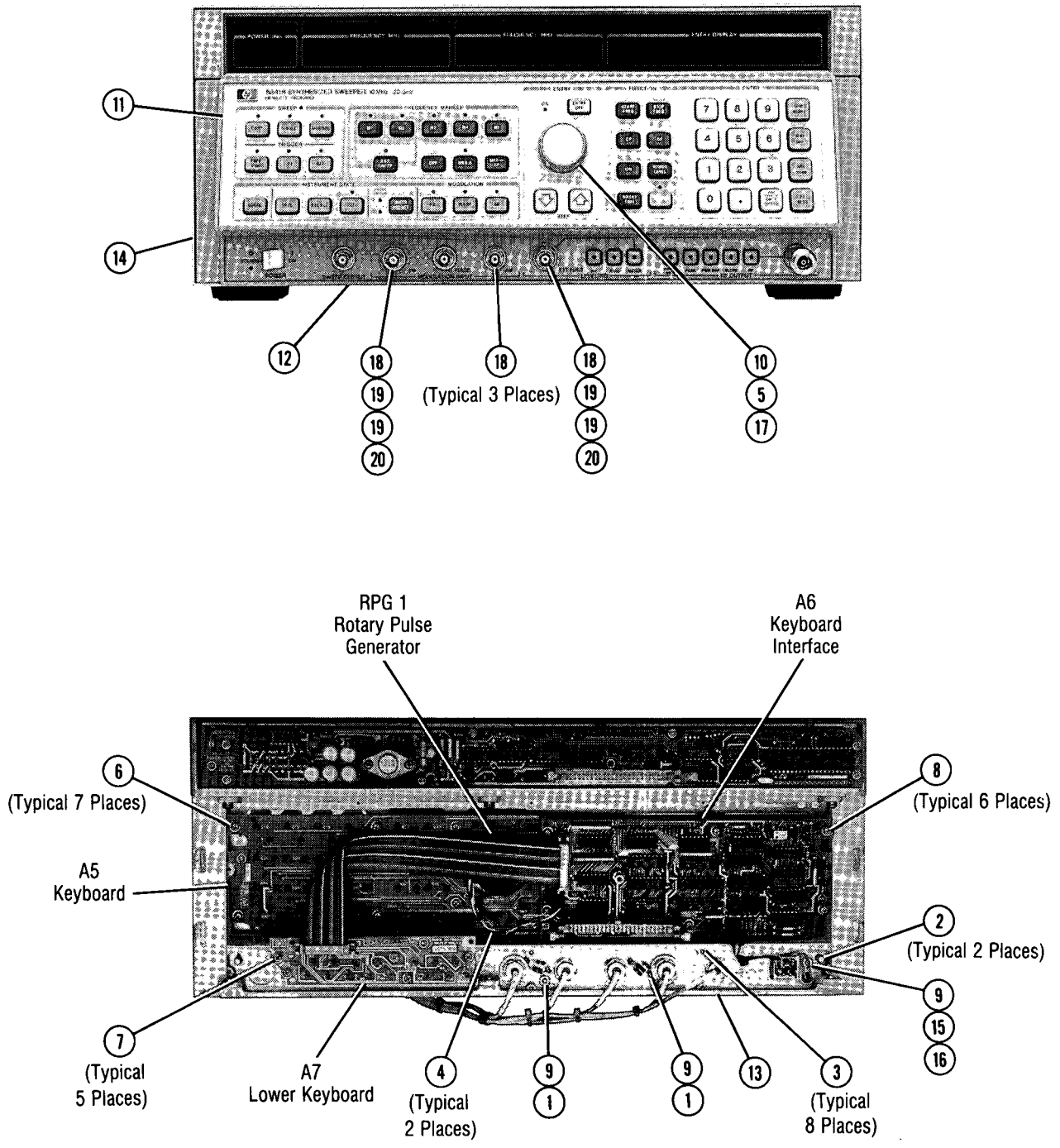


Figure G-10. Front Panel Attaching Hardware

Table G-2. A5, A6, A7 Attaching Hardware

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
1	2360-0115	4	3	SCREW-MACH 6-32 .312-IN-LG PAN-HD-POZI	28480	ORDER BY DESCRIPTION
2, A5	08340-60010	1	1	A5 KEYBOARD ASSEMBLY	28480	08340-60010
3, A6	08340-60011	2	1	A6 KEYBOARD INTERCONNECT ASSEMBLY	28480	08340-60011
4	2200-0115	6	6	SCREW-MACH 4-40 .75-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
5	2200-0105	4	7	SCREW-MACH 4-40 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
6	2200-0113	4	5	SCREW-MACH 4-40 .625-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
7, A7	08340-60012	3	1	A7 LOWER KEYBOARD ASSEMBLY	28480	08340-60012

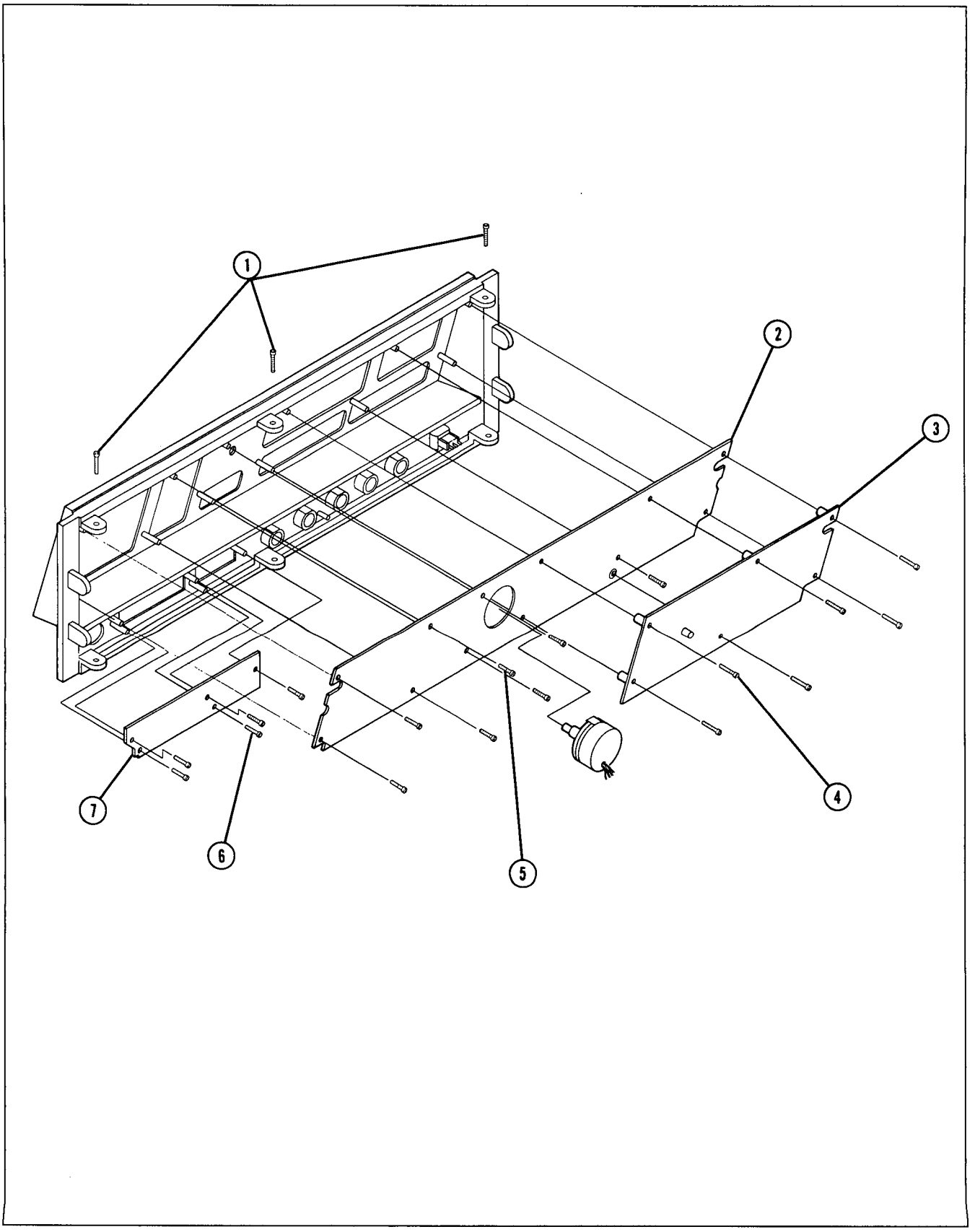


Figure G-11. A5, A6, A7 Attaching Hardware

Table G-3. A2, A3 Attaching Hardware

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A2	**08340-60007**	**6**	**1**	**A2 DISPLAY ASSEMBLY**	**28480**	**08340-60007**
A3	**08340-60182**	**8**	**1**	**A3 DISPLAY DRIVER ASSEMBLY**	**28480**	**08340-60182**
1	0050-2141	1	1	CASTING-AL CTR DISPLAY	28480	0050-2141
	08340-60195	3	1	CASTING REPLACEMENT KIT	28480	08340-60195
2	0520-0127	6	5	SCREW-MACH 2-56 .188-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
3	0520-0136	7	2	SCREW-MACH 2-56 .625-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
4	0520-0139	0	8	SCREW-MACH 2-56 .875-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
5	0520-0174	3	8	SCREW-MACH 2-56 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
6	0570-0189	5	6	SCREW-MACH 0-80 .125-IN-LG 82 DEG	00000	ORDER BY DESCRIPTION
7	2190-0014	1	7	WASHER-LK INTL T NO 2 .089-IN-ID	28480	2190-0014
8	2190-0045	8	8	WASHER-LK HLCL NO 2 .088-IN-ID	28480	2190-0045
9	3050-0098	6	8	WASHER-FL MTLC NO 2 .094-IN-ID	28480	3050-0098
10	4040-1912	5	1	WINDOW-DISPLAY	28480	4040-1912
11	08340-00036	5	1	INSULATOR-HEAT CONDUCTIVE	28480	08340-00036
12	08340-20057	2	1	FRAME-DISPLAY/MACH	28480	08340-20057
13	2360-0115	4	3	SCREW	28480	2360-0115

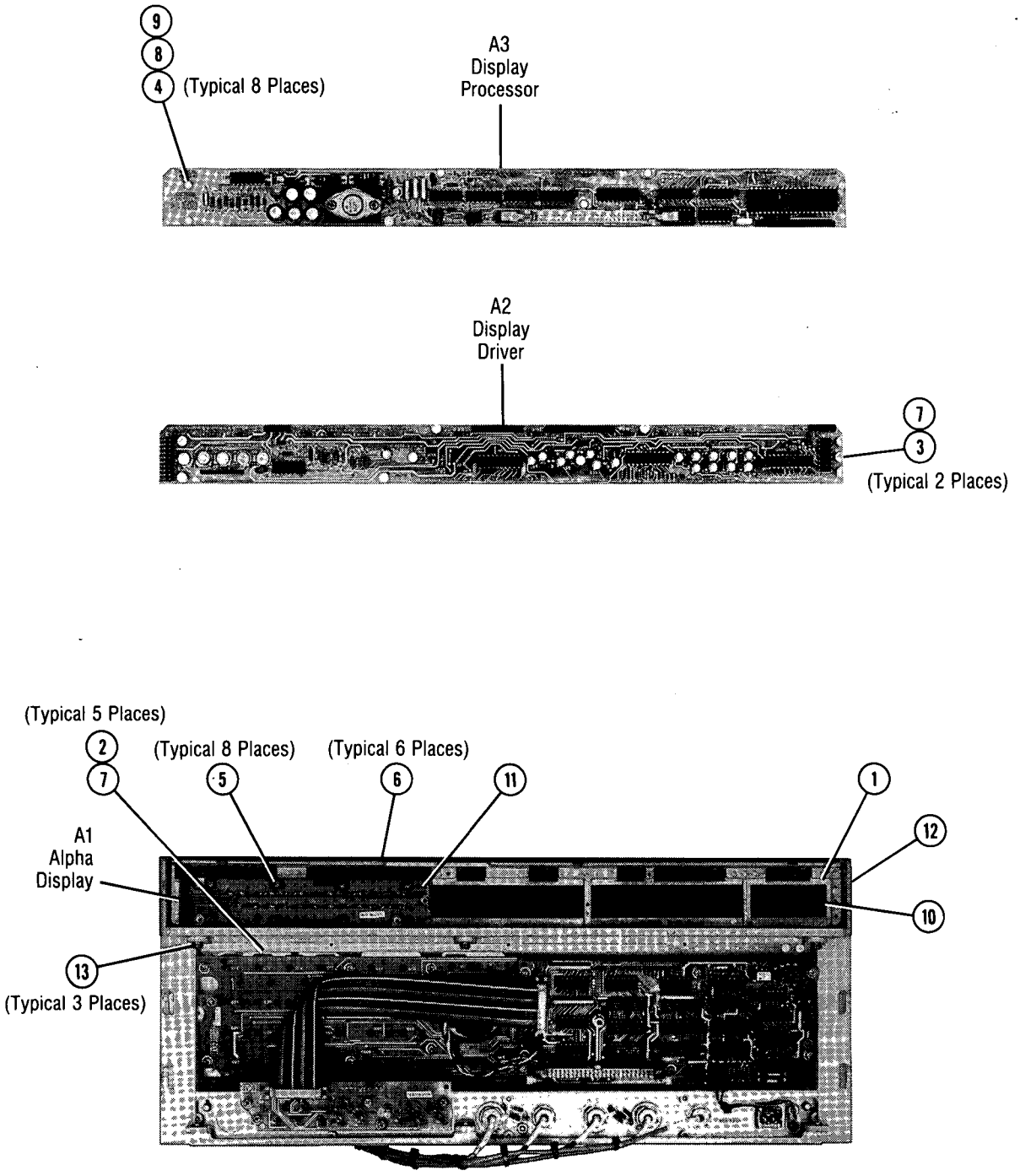


Figure G-12. A2, A3 Attaching Hardware

Table G-4. A1 Attaching Hardware

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
1	08340-20058	3	1	CENTER-SECTION DISPLAY	28480	08340-20058
2	08340-00036	5	1	INSULATOR	28480	08340-00036
3	6040-0239	9		THERMAL COMPOUND	28480	6040-0239
4	0520-0174	3	8	SCREW-MACH 2-56 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
5, A1	08340-60007	2	1	A1 ALPHA DISPLAY ASSEMBLY	28480	08340-60007

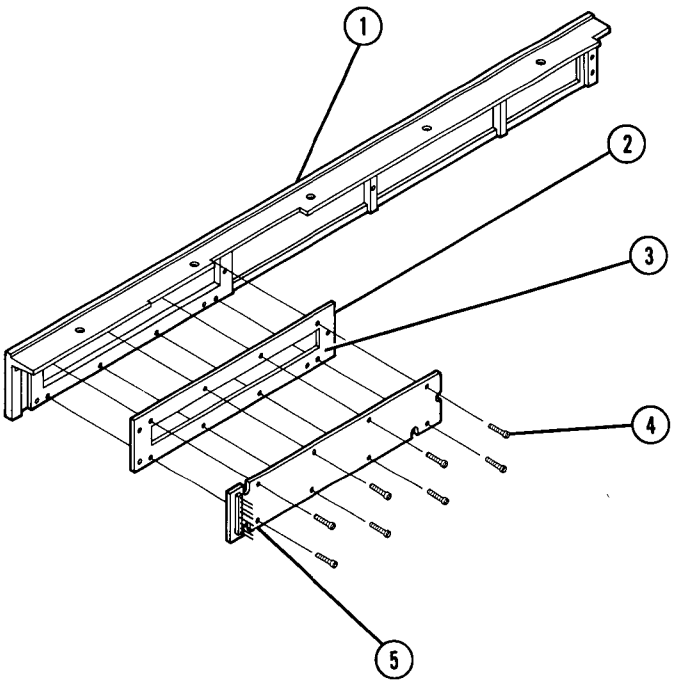


Figure G-13. A1 Attaching Hardware

Table G-5. RPG Attaching Hardware

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
1	2950-0043	8	2	NUT-HEX-DBL-CHAM 3/8-32-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
2	2190-0016	3	2	WASHER-LK INTL T 3/8 IN .377-IN-ID	00000	ORDER BY DESCRIPTION
3	5060-0329	9	1	ROTARY PULSE GENERATOR	28480	5060-0329
4	1251-4223	1	1	PIN LOCKING TANG	28480	1251-4223
	08340-60197	5	1	ROTARY PULSE GENERATOR REPLACEMENT KIT (Includes items 1 through 4)	28480	08340-60197

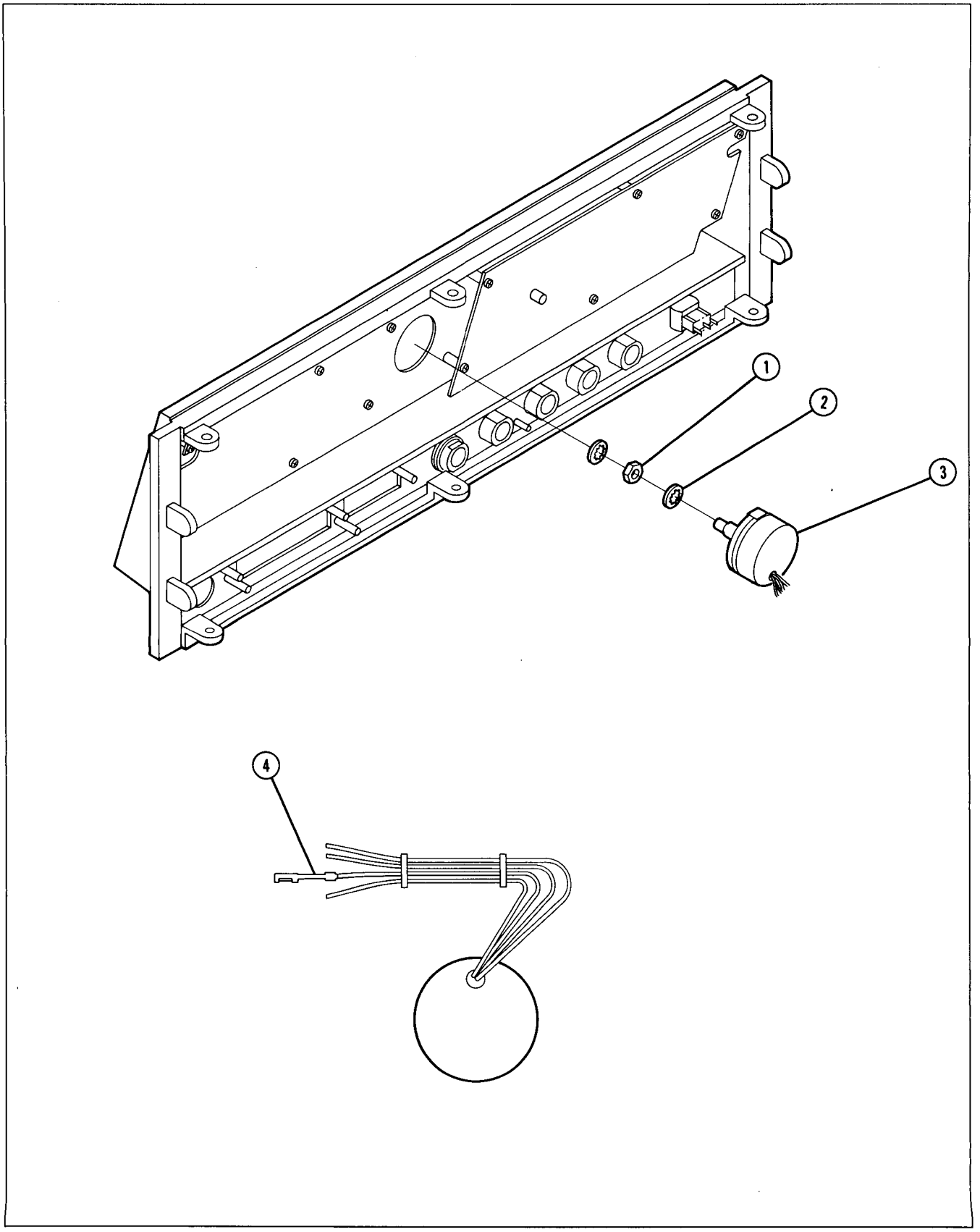


Figure G-14. RPG Attaching Hardware

Table G-6. Panels, Switch, and Connector Attaching Hardware

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
1	08340-20078	7	1	BEZEL-KEYBOARD FINISHED	28480	08340-20078
2	08340-00024	1	1	SUB-PANEL	28480	08340-00024
3	0624-0264	2	16	SCREW-TPG 4-40 .312-IN-LG 82 DEG	00000	ORDER BY DESCRIPTION
4	08340-00025	2	1	DRESS PANEL LOWER KEYBOARD	28480	08340-00025
5	3101-2193	5	1	SWITCH-TGL SUBMIN SPDT 2A 250VAC	28480	3101-2193
6	1990-0858	6	1	LED-LAMP LUM-INT=150UCD IF=25MA	28480	1990-0858
7	08340-00026	3	1	SUB-PANEL LOWER KEYBOARD	28480	08340-00026
8	0510-1148	2	2	RETAINER-PUSH ON KB-TO-SHFT EXT	28480	0510-1148
9	08340-40002	9	1	LED MOUNT	28480	08340-40002
10	1450-0615	9	1	RETAINER	28480	1450-0615
11	2260-0009	3	2	NUT-HEX-W/LKWR 4-40-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
12	0360-0042	4	1	LUG	28480	0360-0042
13	1990-0858	6	1	LED-LAMP LUM-INT=150UCD IF=25MA	28480	1990-0858
14	3101-2193	5	1	SWITCH-TGL SUBMIN SPDT 2A 250VAC	28480	3101-2193
15	0160-4832	4	1	CAPACITOR-FXD .01UF ±10% 100VDC CER	28480	0160-4832
16	1901-0179	7	2	DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
17	08340-60065	6	1	JUMPER WIRE ASSEMBLY	28480	08340-60065
18	00310-48801	0	2	WASHER SHOULDER	28480	00310-48801
19	0590-1251	6	4	NUT-SPCLY 15/32-32-THD .1-IN-THK .562-W	28480	0590-1251
20	0360-1158	5	1	TERMINAL-SLDR LUG PL-MTG .062-HOLE-ID	28480	0360-1158
21	1250-1091	3	1	BNC	28480	1250-1091
22	1250-1870	6	3	BNC	28480	1250-1870
23	0570-0189	5	6	FLAT HEAD SCREW	00000	ORDER BY DESCRIPTION
24	08340-20057	2	1	FRAME DISPLAY	28480	08340-20057
25	0520-0127	6	5	0-80 PAN HEAD SCREW	00000	ORDER BY DESCRIPTION
26	2190-0014	1	2	WASHER-LK	28480	2190-0014
27	4040-1912	5	1	WINDOW DISPLAY	28480	4040-1912

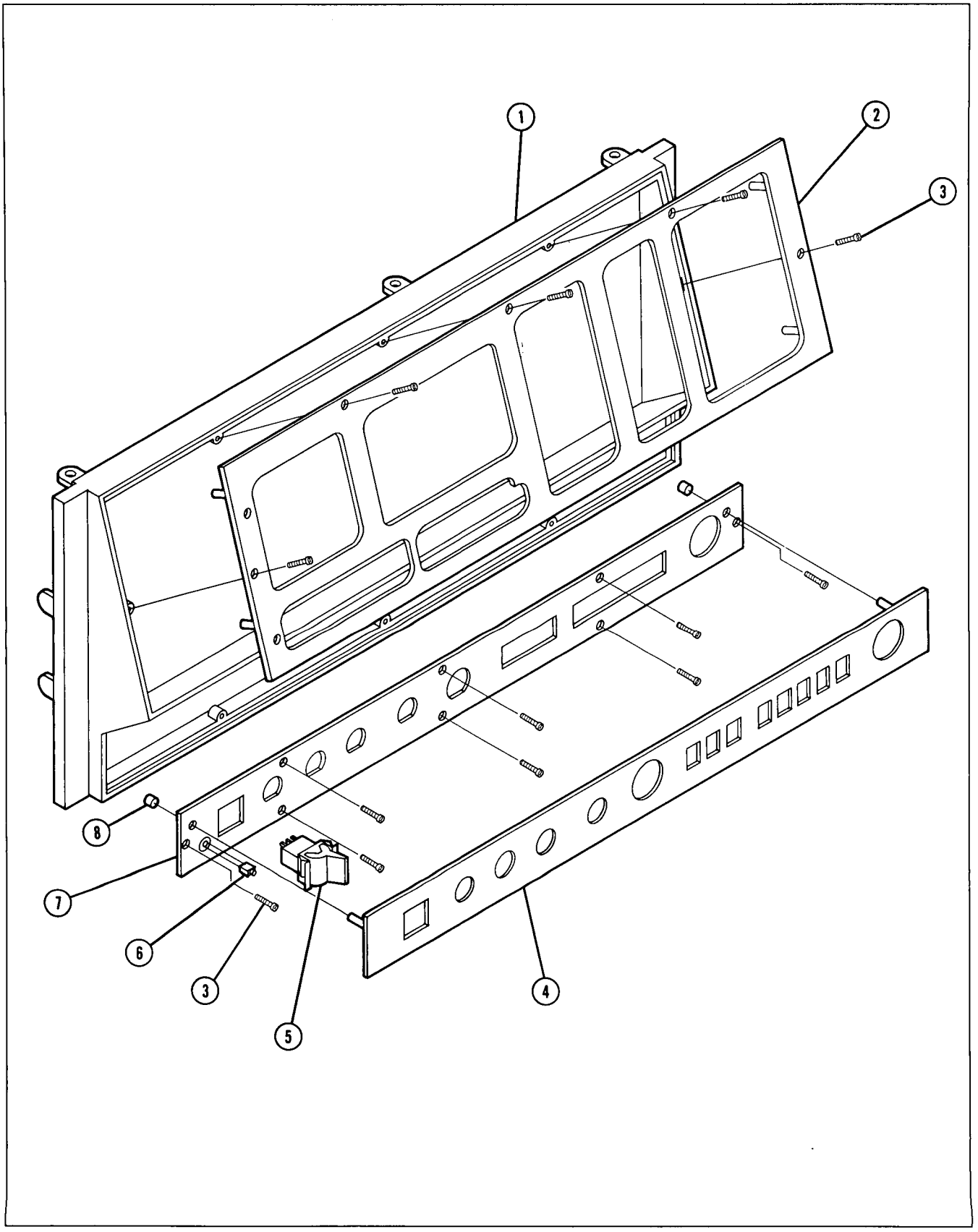


Figure G-15. Panels, Switch, and Connectors Attaching Hardware (1 of 3)

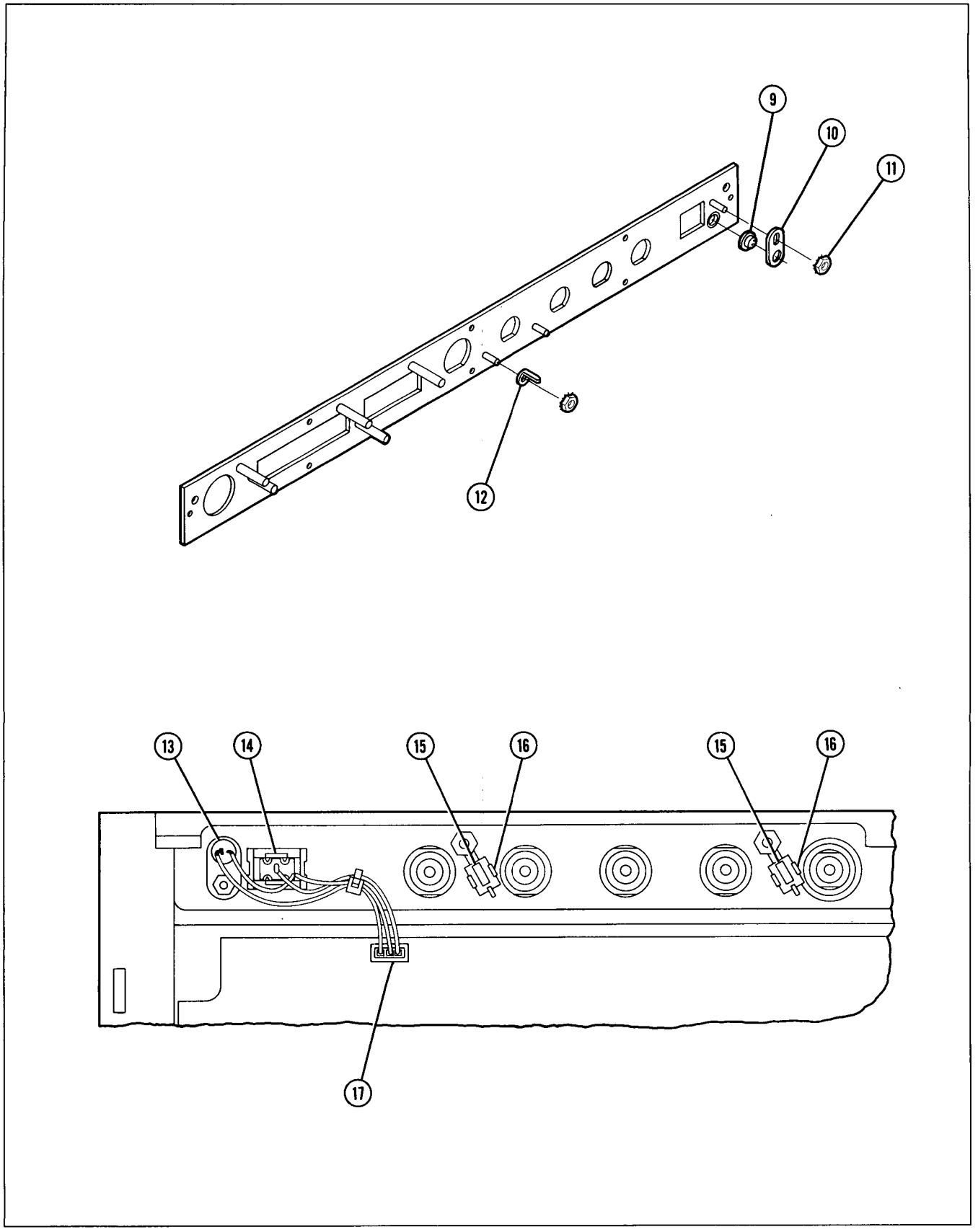


Figure G-15. Panels, Switch, and Connectors Attaching Hardware (2 of 3)

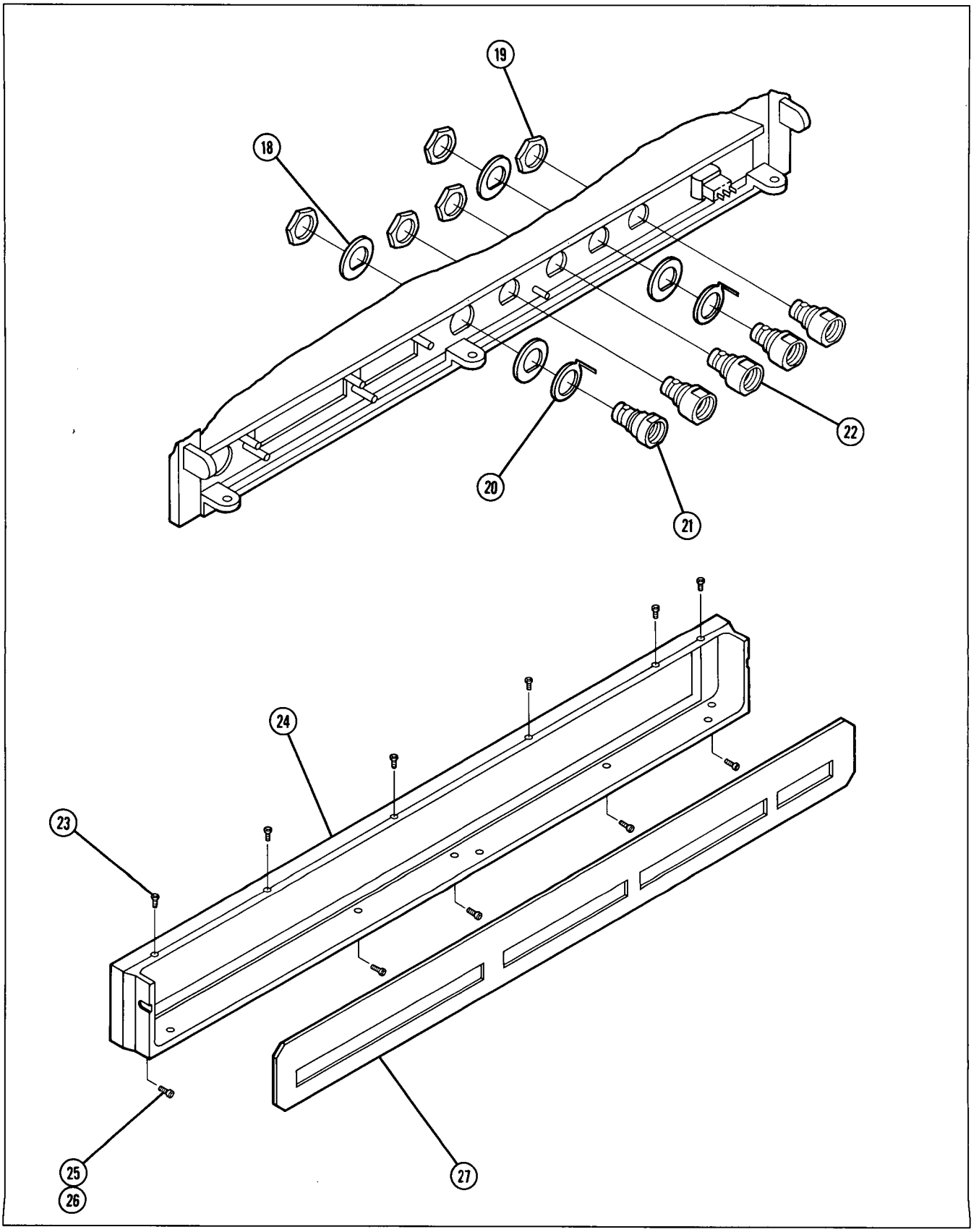


Figure G-15. Panels, Switch, and Connectors Attaching Hardware (3 of 3)

Rear Panel
Theory of Operation

REAR PANEL FUNCTIONAL GROUPS

The assemblies and components mounted on the instrument rear panel are divided into the following functional groups:

- **HP-IB**

  Provides a digital interface by which the synthesizer communicates with other HP-IB equipped instruments or controllers.

- **Sweep-Related Interface Lines**

  Signals that allow the synthesizer to interface with external devices (e.g. X-Y recorders, network analyzers). An external device can determine the instrument's sweep state, and can stop the sweep using STOP SWP IN/OUT. When the synthesizer is in the external trigger mode, an external device can initiate a sweep using the EXT TRIGGER INPUT.

- **Frequency Standard**

  Includes the INT and EXT connectors and the frequency standard switch. Use this group to select either the internal or external frequency standard, the synthesizer's master timebase.

- **RF Outputs**

  Include the AUX OUTPUT connector, and, for option 004 instruments, the RF OUTPUT connector.

- **Dedicated Interface Connectors**

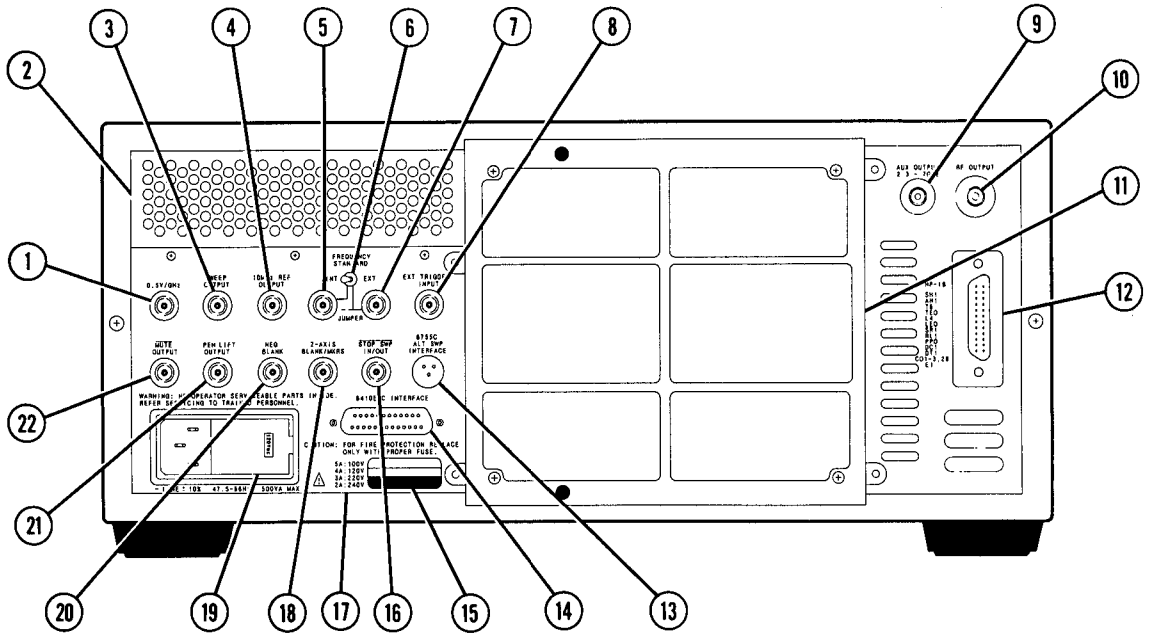
  Interface with the HP 8410B/C vector network analyzer.

- **Fan**

  Provides instrument cooling.

- **Line Module**

  Holds the main line fuse and the line voltage selector cam, and suppresses line transients.



1. 0.5V/GHz J6
2. HEAT SINK (P/O A62 Motherboard)
3. SWEEP OUTPUT J7
4. 10 MHz REF OUTPUT J8
5. FREQUENCY STANDARD INT J9
6. FREQUENCY STANDARD SWITCH
7. FREQUENCY STANDARD EXT J10
8. EXT TRIGGER INPUT J7 – J11
9. AUX OUTPUT 2.3 – 7 GHz J19
10. RF OUTPUT J20 (Option 004)
11. FAN (B1)
12. HP-IB J21
13. HP 8755C ALT SWP INTERFACE J17
14. HP 8410 INTERFACE J18
15. SERIAL TAG
16. $\overline{\text{STOP SWP}}$ IN/OUT J16
17. FUSE RATING GUIDE
18. Z-AXIS BLANK/MKRS J15
19. LINE MODULE
20. NEG BLANKING J14
21. PEN LIFT OUTPUT J13
22. $\overline{\text{MUTE}}$ OUTPUT J12

Figure G-16. Rear Panel Features

RF CONNECTORS

The nominal impedance of the following RF connectors is 50 ohms.

J19 — Auxiliary Output 2.3 to 7 GHz

This female, type-N connector nominally provides a −3 dBm RF output from the YIG oscillator.

J20 — RF Output

In option 004 and 005 instruments, this male, precision 3.5 mm connector replaces the standard front panel RF output connector.

Protection from DC Voltages. A capacitor in series with the RF output protects the instrument from DC potentials of up to 50V.

Where to Find Precision 3.5 mm Connector Care Information. Be careful when using precision 3.5 mm connectors. For detailed information on the care of these connectors, refer to *Microwave Connector Care*, HP part number 08510-90064.

BNC CONNECTORS

J6 — 0.5V/GHz

Maximum Specified Voltage. The output of this BNC connector is proportional to the RF output frequency (0.5V per GHz), across the entire frequency span.

Load Impedance and Current Limiting. The 0.5V/GHz accuracy is ±1% ±2 mV with a load impedance of 4 kΩ or greater. This output is current limited; a load of less than 4 kΩ causes the circuit to current limit at high frequencies.

1V/GHz. You can have an output voltage ratio of 1 volt per GHz by adding two jumpers on the A28 SYTM assembly. This provides a maximum specified voltage of 19V. Above 19 GHz, the output levels off at approximately 20V.

J7 — Sweep Output

Swept Mode Voltage Range. When the instrument sweeps, the voltage range for this connector is 0 to 10V, regardless of sweep width.

CW Mode Voltage. When the instrument is in CW, the voltage at J7 is 0 to 10V across the frequency range.

Manual Mode Voltage Range. In the manual mode, the sweep output ranges from 0V at 10 MHz to 10V at the instrument's maximum frequency, with proportional voltages at the frequencies between these two points.

J8 — 10 MHz Reference Output

This output, from the instrument's internal frequency standard, is 10 MHz at approximately 0 dBm. This signal can be the master time base reference output for a network of instruments.

J9 – Internal/J10 – External

Use these connectors, and the INT/EXT switch, to select either the internal 10 MHz crystal oscillator frequency standard, or an external frequency standard as the instrument's master time base.

How to Select the Internal Standard:

1. Place the switch in the INT position.
2. Connect a jumper cable between the INT and EXT BNC connectors.

How to Select an External Standard:

1. Check that the source to be used is 10 MHz ±100Hz.
2. Check that the source to be used provides 1 to +10 dBm.
3. Place the switch in the EXT position.
4. Connect the external source to the EXT BNC connector.

When the switch is in the EXT position, the internal standard is turned off, and the amber EXT REF annunciator comes on above the front panel ENTRY DISPLAY.

J11 – External Trigger Input

Use this input (2 kΩ nominal impedance) to trigger the start of sweep. A trigger signal must be at least 2V (10V maximum), and wider than 0.5 microseconds.

J12 – Mute Output

This output is an active low TTL signal used to pause external X-Y recorders or instruments when the synthesizer crosses a frequency-band switchpoint. For more information on using an X-Y recorder, refer to the *Operating Manual*.

J13 – Penlift Output

Penlift disables an X-Y recorder during sweep retrace. If you press **[SHIFT] [LINE]**, penlift also disables the recorder during band switchpoints.

Penlift provides a current path to ground for the recorder's pen solenoid. A zener diode protects the penlift circuit from excessive recorder solenoid voltage, and a diode protects it from negative voltages on the input.

J14 – Negative Blanking

This output provides a negative rectangular pulse (approximately −5V into 2kΩ) during sweep retrace and band switchpoints.

J15 – Z-Axis Blanking / Markers

This output supplies a positive rectangular pulse (approximately +5V into 2kΩ) during sweep retrace and band switchpoints.

When the RF output is at a marker frequency, this output supplies a −5V pulse.

J16 – Stop Sweep In / Out

Grounding this Input Stops the Sweep. Forward sweep stops when this line is grounded, and resumes when the input is released from ground. If the input is grounded during retrace, retrace continues, but the next sweep does not begin until the input is released from ground.

Stop Sweep Indicates when Sweep Stops. As an output, a TTL low indicates that the sweep has been stopped by the synthesizer.

NOTE: For more information on the preceding BNC signal operating parameters, refer to the *Operating Manual*.

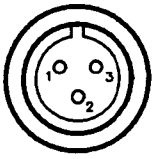
INTERFACE CONNECTORS

J17 – 8755C Alternate Sweep Interface

The synthesizer can sequence alternate sweeps in the HP 8755C scalar network analyzer using an interface cable (HP part number 8120-3174). Figure G-17 shows the pin configuration and a complete description of the sweep interface signals.

ALTERNATE SWEEP INTERFACE CONNECTOR J17

8755C
ALT SWP
INTERFACE



(viewed from rear of instrument)

Pin	Mnemonic	Description	Level	Wire Color Code	A62J31 Pin	Source
1	LALTEN	LOW to Externally Enable ALT SWP Mode in HP 8755C	TTL OUTPUT	9 - 1 - 5	23	A57P1-60
2	LALTSEL	Channel Select (HIGH =Channel 1, LOW =Channel 2)	TTL OUTPUT	9 - 1 - 6	24	A57P1-59
3	LRETRACE	LOW During Retrace	TTL OUTPUT	9 - 1 - 7	25	A57P1-58

Figure G-17. 8755C Alternate Sweep Interface (J17)

J18 – 8410B/C Interface Connector

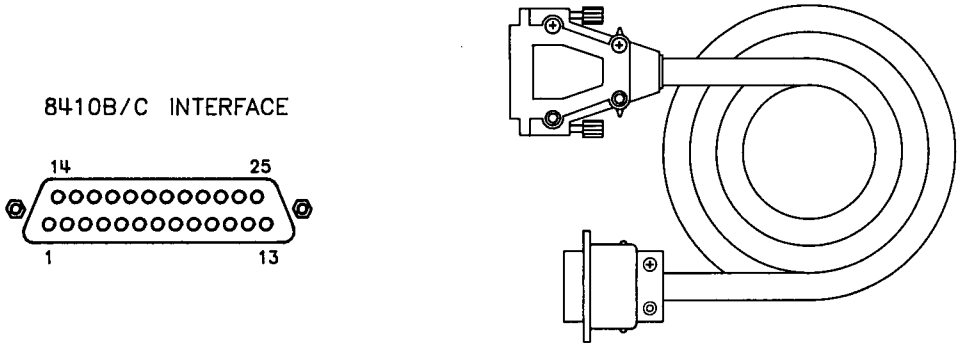


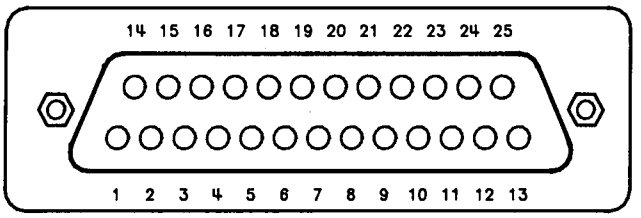
Figure G-18. 8410B/C Interface and Cable

The purpose of J18. Using a source control cable (HP part number 08410-60146), this interface permits multi-octive operation of the HP 8410B/C with the synthesizer.

The Interface Signals. Pins of this connector duplicate several rear panel functions (see Figure G-19). There is also a pin input (LSTEPUP) for a switch closure to execute the UP key function, which increments the active front panel control function.

8410B/C INTERFACE CONNECTOR J18

(As seen from rear panel)



J18 Pin	Mnemonic	Levels	Input/Output	Signal Source/ Destination	A62J31 Pin	J18W46 Wire Color Code
1						
2	Z-AXIS BLANK	+5V, −5V*	OUTPUT	A57P1-99	2, 16	2
3						
4	LALTSEL	TTL (LOW TRUE)	OUTPUT	A57P1-59	10, 24	0
5	LSSP (LSTOP SWEEP)	TTL (LOW TRUE)	I/O	A57P1-107	5, 19	5
6	+5.2V			A52P1-17, 18, 41, 42	3	3
7						
8						
9	EXT TRIG	EXT SOURCE INPUT LEVEL	INPUT	A57P1-106	4, 18	6
10	PEN LIFT	SEE TEXT	OUTPUT	A57P1-108	6, 20	8
11	$\overline{\text{MUTE}}$	TTL (LOW TRUE)	INPUT	A57P1-61	8, 22	4
12						
13						
14	NEG BLANK	0V, −5V*	OUTPUT	A57P1-41	1, 15	1
15						
16	LRETRACE	TTL (LOW TRUE)	OUTPUT	A57P1-58	11, 25	9 - 0
17	LALTEN	TTL (LOW TRUE	OUTPUT	A57P1-60	9, 23	9
18						
19	GND			STOP SWEEP BNC GND LUG		9 - 0 - 7
20						
21						
22	LSTEPUP	TTL (LOW TRUE)	INPUT	A62J1-28	14	9 - 0 - 8
23						
24	8410 TRIG	TTL (LOW TRUE)	OUTPUT	A57P1-62	7	7
25						

*See text

Figure G-19. 8410B/C Interface Connector (J18)

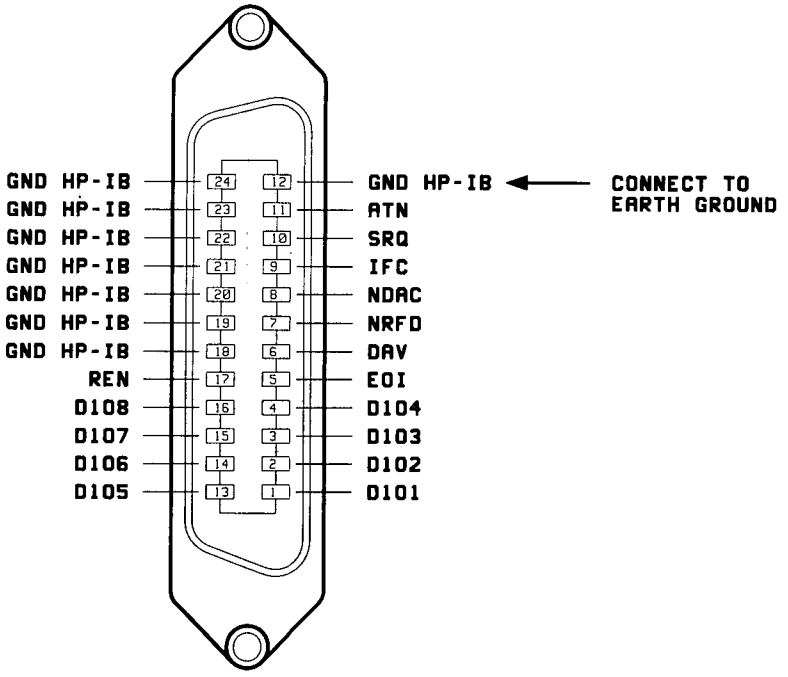
J21 – HP-IB Interface Connector

The Purpose of J21. The HP-IB interface lets the synthesizer communicate with another instrument or device on the HP-IB bus.

Figure G-20 shows the HP-IB connector and its signal.

Where to Look for HP-IB Operating Information. For more information on HP-IB operation, refer to the remote programming information in the *Operating Manual*.

Where to Look for Troubleshooting Information. Refer to the Controller functional group for HP-IB troubleshooting information.



NOTE
The HP-IB logic levels are TTL compatible, i.e., true state 0 V dc to 0.4 V dc, False State +2.5 V dc to +5 V dc.

Mnemonics Table

Mnemonic	Description
ATN	LOW = Attention control line
DAV	LOW = Data Valid control line
DIO1 through 8	LOW = Data Input/Output lines
EOI	LOW = End Or Identify control line
IFC	LOW = Interface Clear control line
NDAC	LOW = Data Not Accepted control line
NRFD	LOW = Not Ready For Data control line
REN	LOW = Remote Enable control line
SRQ	LOW = Service Request control line

Figure G-20. HP-IB Connector (J21)

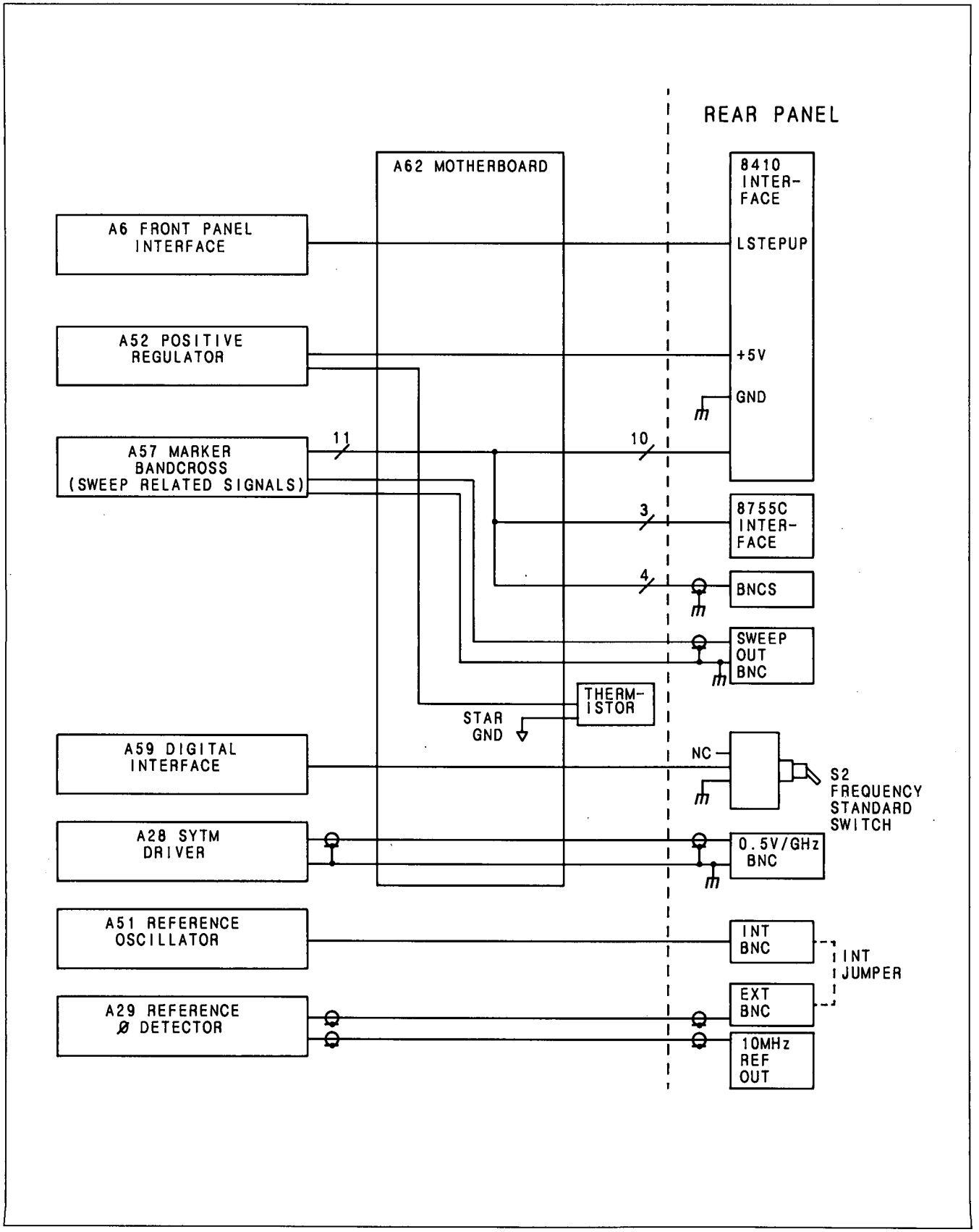


Figure G-21. Rear Panel Simplified Block Diagram (1 of 2)

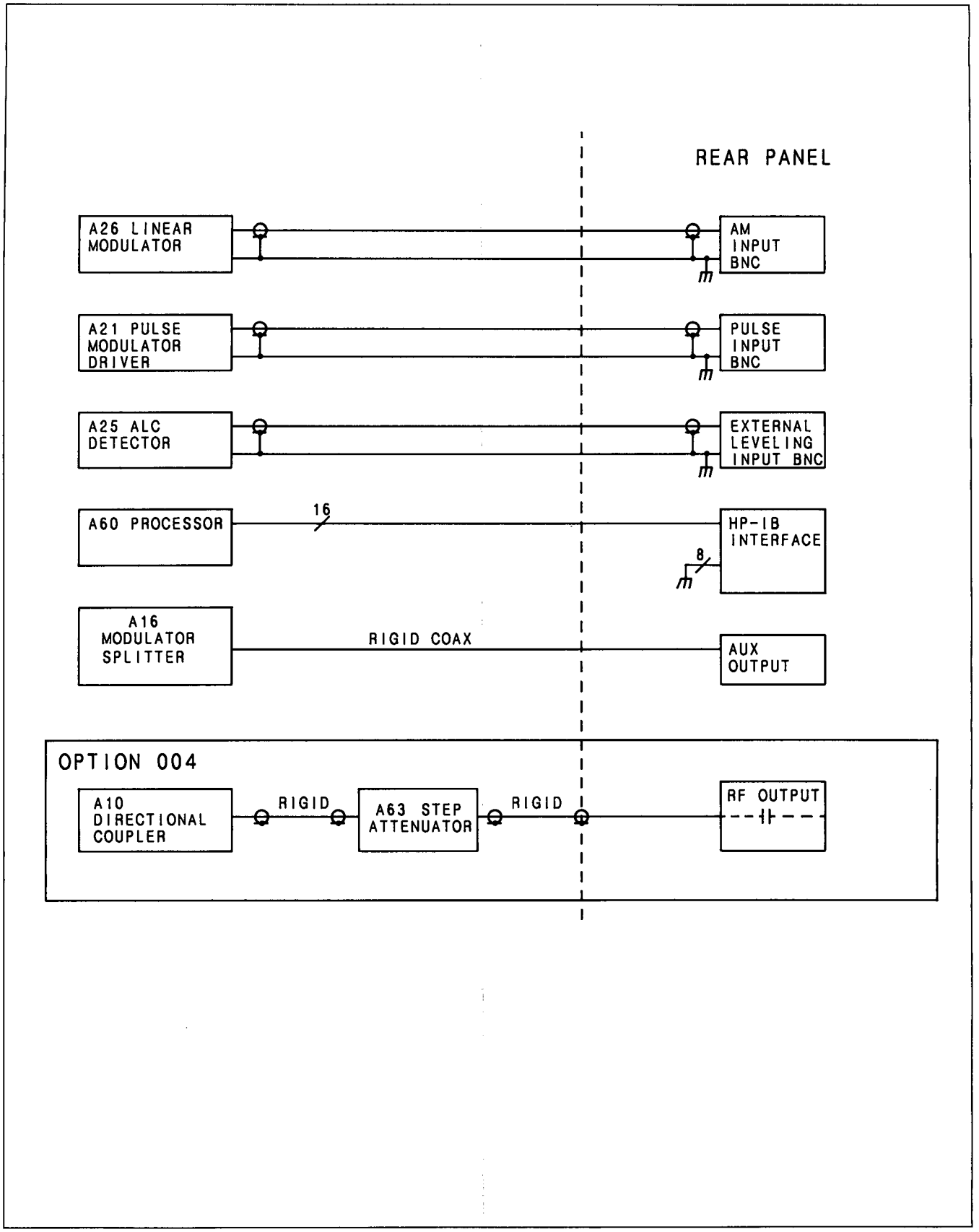


Figure G-21. Rear Panel Simplified Block Diagram (2 of 2)

Rear Panel
Assembly-Level Troubleshooting

REAR PANEL CONNECTORS

Refer to Figure G-21 and determine the source/destination assembly that generates/receives the signal you wish to troubleshoot, and the assembly(ies) and/or cable(s) through which the signal goes.

FAN

Refer to Power Supply — Fan functional group for fan troubleshooting information.

LINE MODULE

Refer to Power Supply — Fan functional group for line module troubleshooting information.

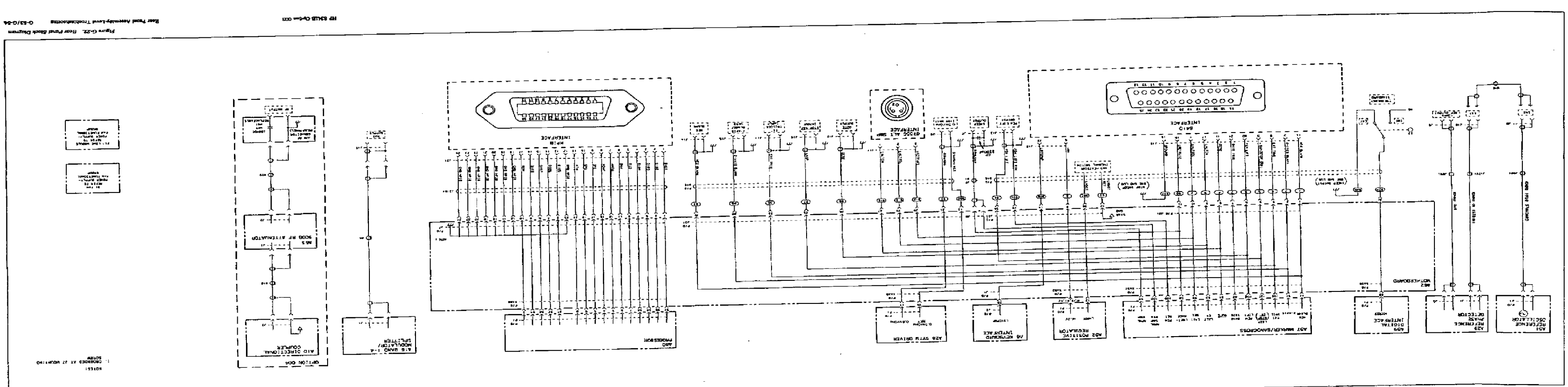


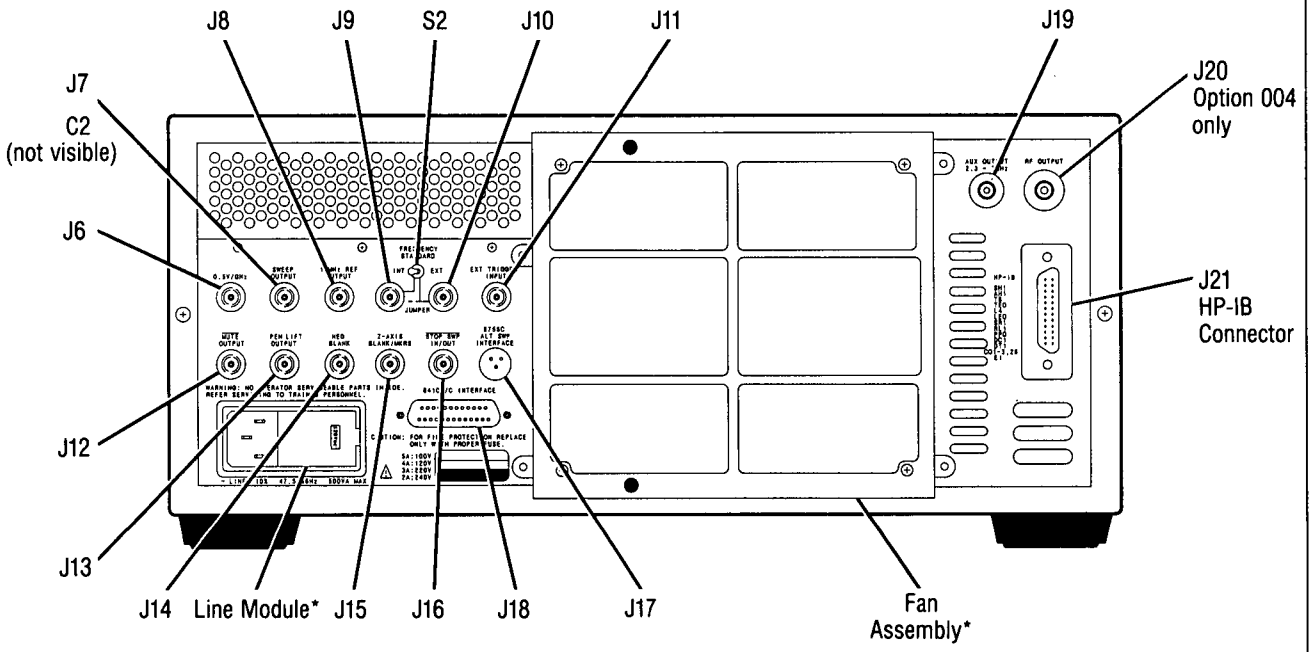
Figure 0-22. Rear Panel Block Diagram

Rear Panel Replaceable Parts

This section provides rear panel assembly-level replaceable parts.

Table G-7. Rear Panel Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
				REAR PANEL		
C2	0160-4819	7	1	CAPACITOR-FXD 2200PF ±5% 100VDC (On J7, sweep output)	28480	0160-4819
J6	1250-0083	1	8	CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0083
	0360-1632	0	4	TERMINAL-SLDR LUG LK-MTG FOR-#3/8-SCR	28480	0360-1632
	2950-0001	8	2	NUT-HEX-DBL-CHAM 3/8-32-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
J7	1250-0083	1		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0083
	0360-1632	0		TERMINAL-SLDR LUG LK-MTG FOR-#3/8-SCR	28480	0360-1632
	2950-0001	8		NUT-HEX-DBL-CHAM 3/8-32-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
J7W1	08340-60070	3	1	CABLE ASSY-COAX (A62J8 TO R.P. J7)	28480	08340-60070
J8	1250-0102	5	3	CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0102
	2190-0068	5	3	WASHER-LK INTL T 1/2 IN .505-IN-ID	28480	2190-0068
	2950-0054	1	3	NUT-HEX-DBL-CHAM 1/2-28-THD .125-IN-THK	00000	ORDER BY DESCRIPTION
J8W1	08340-60086	1	1	CABLE ASSY-COAX (A29J5 TO R.P. J8)	28480	08340-60086
J9	1250-0102	5		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0102
	2190-0068	5		WASHER-LK INTL T 1/2 IN .505-IN-ID	28480	2190-0068
	2950-0054	1		NUT-HEX-DBL-CHAM 1/2-28-THD .125-IN-THK	00000	ORDER BY DESCRIPTION
J9W1	08340-60089	4	1	CABLE ASSY-COAX (A51J1 TO R.P. J9)	28480	08340-60089
J10	1250-0102	5		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0102
	2190-0068	5		WASHER-LK INTL T 1/2 IN .505-IN-ID	28480	2190-0068
	2950-0054	1		NUT-HEX-DBL-CHAM 1/2-28-THD .125-IN-THK	00000	ORDER BY DESCRIPTION
J10W1	08340-60085	0	1	CABLE ASSY-COAX (A29J1 TO R.P. J10)	28480	08340-60085
J11	1250-0083	1		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0083
	2190-0016	3	4	WASHER-LK INTL T 3/8 IN .377-IN-ID	28480	2190-0016
J12	1250-0083	1		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0083
	2190-0016	3		WASHER-LK INTL T 3/8 IN .377-IN-ID	28480	2190-0016
J13	1250-0083	1		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0083
	0360-1632	0		TERMINAL-SLDR LUG LK-MTG FOR-#3/8-SCR	28480	0360-1632
J14	1250-0083	1		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0083
	2190-0016	3		WASHER-LK INTL T 3/8 IN .377-IN-ID	28480	2190-0016
J15	1250-0083	1		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0083
	2190-0016	3		WASHER-LK INTL T 3/8 IN .377-IN-ID	28480	2190-0016
J16	1250-0083	1		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0083
	0360-1632	0		TERMINAL-SLDR LUG LK-MTG FOR-#3/8-SCR	28480	0360-1632
J17	1251-6781	0	1	CONNECTOR 3-PIN M CIRC AUDIO (Includes mounting hardware)	28480	1251-6781
J18	1251-0064	0	1	CONNECTOR 25-PIN F D SERIES	28480	1251-0064
	1251-2942	7	2	MOUNTING HARDWARE KIT	28480	1251-2942
J19	08340-60127	1	1	CONNECTOR-TYPE N (R.P. AUX OUT)	28480	08340-60127
	2190-0104	0	1	WASHER-LK INTL T 7/16 IN .439-IN-ID	28480	2190-0104
	2950-0132	6	1	NUT-HEX-DBL-CHAM 7/16-28-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
J20				REFER TO OPTION 004 AND 005 LISTINGS		
J21				P/O J21W1		
J21W1	8120-3653	9	1	CABLE ASSY-RIBBON (HP-IB) (Includes J21 and mounting hardware)	28480	8120-3653



*See Power Supplies/Fan Replaceable Parts

Figure G-23. Rear Panel Replaceable Parts

RF Section
Assembly-Level Service

CONTENTS

CONTENTS (Cont'd)

RF Section Introduction

ASSEMBLIES

The RF section functional group consists of the following assemblies:

Microcircuit Assemblies

- A8 3.7 GHz oscillator
- A9 low band pulse modulator
- A10 directional coupler
- A11 high band detector
- A12 low band splitter/detector
- A13 SYTM (switched YIG-tuned multiplier)
- A14 high band power amplifier/detector
- A15 low band low pass filter
- A16 modulator/splitter
- A17 low band mixer
- A18 low band power amplifier
- A20 RF section filter
- A63 RF attenuator/J5 RF output connector
- A64 low band low pass filter
- AT1 peripheral mode isolator
- AT3 isolator

ALC Loop Assemblies

- A25 ALC detector
- A26 linear modulator
- A27 level control

SYTM-Related Assemblies

- A22 RF clamp/SRD bias
- A24 attenuator driver/SRD bias
- A28 SYTM driver/A47 sense resistor assembly

Pulse Modulation Related Assembly

- A21 pulse modulator driver

RF Section
Theory of Operation

The RF section contains the microcircuits and board assemblies that produce, amplify, and control the RF output. Refer to Figure H-2 for a simplified RF functional group block diagram.

RF power generated by the YIG oscillator is delivered to the mod/splitter, which couples off a portion of the signal for the rear panel auxiliary output. The mod/splitter also splits the power to provide RF to the high band power amplifier, and the low band mixer.

LOW BAND

Low band is produced by mixing a high-power swept LO signal with a fixed RF signal. The fixed signal is generated by the 3.7 GHz oscillator, and passes through a linear modulator, pulse modulator, low pass filter, and isolator, before it reaches the mixer.

The mixer output frequency (IF) is the difference between the LO and the RF frequencies. Because the LO sweeps from 3.71 to 6.0 GHz, and the RF is fixed at 3.7 GHz, the IF sweeps from 0.01 to 2.3 GHz. The low band power amplifier amplifies the IF, routes through a low pass filter, and sends it to the low band splitter/detector, where a small portion of the signal is split off and detected for leveling.

The leveled IF (RF) enters the SYTM (switched YIG-tuned multiplier), which provides a straight through path for RF from the low band splitter/detector when low band is activated. After passing through the SYTM, the signal passes through the directional coupler, which performs no function in low band, and the step attenuator, before reaching the instrument output connector.

HIGH BAND

The high bands are produced by feeding the mod/splitter RF output through the high band power amplifier. The SYTM generates harmonics from the high level output of the power amplifier, to produce bands 2 and 3. The SYTM contains a bandpass filter tuned to the desired RF output frequency, which allows it to pass the desired RF output frequency, and reject the unwanted harmonics.

The directional coupler couples off part of the SYTM RF output to the high band detector for high band leveling. The step attenuator provides low power output levels in all bands.

LEVELING

The ALC (automatic level control circuit) uses feedback to hold the RF output constant throughout the full frequency range.

When internally leveled in high band, voltage from the high band detector is fed through a log amplifier and summed with a correction level that closely approximates the variations of the RF attenuator and the RF cables. The corrected detector level is then fed through the sample/hold, and routed to the linear modulator driver assembly where the corrected detector voltage is summed with the reference voltage at the integrator input.

If the corrected detector voltage is not equal to the reference voltage, the integrator output voltage changes, and drives an exponential driver that feeds current to the linear modulator in the mod/splitter. This changes the RF output level, changing the detected voltage from the high band detector. The modulator driver is also switched to the A9 high band modulator in the 3.7 GHz oscillator.

PULSE MODULATION

Pulse modulation requires special drive circuitry and modulators to achieve narrow pulse widths. The high band pulse modulator is in the mod/splitter, and the low band pulse modulator is located just after the 3.7 GHz oscillator. The pulse modulator drive circuitry coordinates ALC operation with the pulse signal. When the pulse input is driven low to turn off the RF, the ALC is triggered to sample and hold the current RF level. During the time the pulse is held low, the output is attenuated by more than 80 dB. When the pulse input is returned to its normal high level, the ALC releases the hold circuits, and the instrument returns to the RF level it had before the RF was turned off.

STEP RECOVERY DIODE (SRD)

The SYTM contains a step recovery diode that generates the harmonics for the high bands. Power level, frequency, and DC bias effect the SRD's ability to generate harmonics. For maximum conversion efficiency, SRD bias is varied with power level and frequency.

In band 1 (2.3 to 7 GHz), the SRD is biased on to allow the fundamental to pass through. The SYTM also contains a YIG-tuned bandpass filter that can be tuned over the high bands by changing the magnetic field. The filter passband must closely track the YO frequency, or some harmonic of it, to cover the high bands.

SYTM DRIVER COMPENSATIONS

The SYTM driver compensates for nonlinearities in the tuning magnet, hysteresis, and magnetic delay. The SYTM pin diode switch allows the low band signal to be switched off when high band is selected. The bias for this switch is generated on the attenuator driver/SRD bias assembly.

A8 3.7 GHZ OSCILLATOR

The A8 3.7 GHz oscillator provides a fixed 3.70 GHz RF output. The A8A1 oscillator microcircuit and the A8A2 oscillator bias assembly are located inside the A8 3.7 GHz oscillator housing. This source is phase-locked to a 100 MHz internal standard. A linear modulator, at the output of the oscillator, provides amplitude control from nominally +1 to −70 dBm.

The A8A2 bias assembly provides the necessary circuitry to amplify the 100 MHz input signal and phase-lock the 3.70 GHz signal to it. A lock signal is generated when the two signals are phase-locked. A8A2 also provides the +20V and −10V microcircuit bias voltages.

A9 LOW BAND PULSE MODULATOR

The A9 pulse modulator is a shunt PIN diode modulator that provides an on/off ratio greater than 80 dB in low band. Modulator control is the LOPMOD DR (low band pulse mod drive) signal from the A21 pulse modulator driver assembly.

A10 DIRECTIONAL COUPLER

The A10 directional coupler has a −16 dB coupling coefficient. The reverse-coupled port is terminated. The coupled output is sent to the A11 high band detector for leveling in the higher bands. Although the low band output passes through the A10 directional coupler, it does not affect low band leveling. The insertion loss is less than 1.3 dB at 26.5 GHz.

A11 HIGH BAND DETECTOR

The A11 high band detector detects the RF amplitude for leveling in high band, producing a positive output voltage proportional to the RF power. The detector output is sent to the A25 ALC detector assembly for processing.

A12 LOW BAND SPLITTER/DETECTOR

The A12 low band splitter/detector samples and detects the RF amplitude for low band leveling. It consists of a resistive power splitter, and a schottky diode detector that produces a positive output voltage proportional to the RF power.

The LDET BW (low detector bandwidth control) input (from the A26 linear modulator assembly) switches in additional filtering for leveling below 400 MHz. A thermistor (mounted inside the splitter/detector package) compensates for detector temperature variations.

A13 SWITCHED YIG-TUNED MULTIPLIER (SYTM)

The A13 SYTM uses a PIN diode switch to turn the band 0 signal off when you select band 1-3. In band 0, the SYTM provides a straight path for the 0.01 to 2.3 GHz RF signal from the A12 low band splitter/detector. Low band insertion loss is typically less than 0.5 dB.

For high band, the RF input from the AT1 isolator is fed to the SYTM. This signal is applied through an impedance matching circuit to an SRD (step recovery diode) to produce an output rich in harmonics. The SRD BIAS applied to the diode is different for each band to optimize the harmonic required for that band:

Band 1 = fundamental
Band 2 = second harmonic
Band 3 = third harmonic

The YIG tuned filter is a tunable bandpass filter. It is tuned to the RF output frequency by the SYTM coil drive-current (supplied by the A28 SYTM driver). The filter bandpass frequency is determined by a small YIG sphere whose resonant frequency depends on the strength of the surrounding magnetic field. The magnetic field is established by an opposing pair of electromagnet coils. Changing the current through the coils changes the magnetic field strength, and, consequently, the bandpass frequency. Typically, the bandpass is ±12 MHz.

A14 HIGH BAND POWER AMPLIFIER/DETECTOR

The A14 high band power amplifier/detector is a GaAs FET (gallium arsenide field effect transistor) that covers the 2.3 to 7.0 GHz frequency range. The amplifier provides approximately 26 dBm output power. The small-signal gain is typically 25 dB, but at maximum leveled output, the amplifier can be 10 dB into compression.

A 7.0 GHz notch filter reduces harmonics out of the amplifier. This filter is switched in when the amplifier operates below 4.5 GHz.

The detector portion of the A14 microcircuit provides the control signal for the SRD bias.

A15 LOW BAND LOW PASS FILTER

The A15 low pass filter attenuates harmonics from the 3.7 GHz oscillator to minimize unwanted mixing products produced in the A17 low band mixer.

A16 HIGH BAND MODULATOR/SPLITTER

The A16 modulator/splitter divides the YIG oscillator output into three paths:

- The low band output provides LO drive for the low band mixer.
- The high band output feeds the high band amplifier.
- The third output feeds the AUX OUTPUT via an internal coupler.

A17 LOW BAND MIXER

The A17 mixer mixes a fixed 3.7 GHz signal with the swept 3.71 to 6.0 GHz YO output, producing the 0.01 to 2.3 GHz RF output of low band.

A 3.7 GHz directional filter (before the single balanced mixer) and a 2.75 GHz low pass filter (at the output) minimize unwanted mixing products. The swept YO output, after passing through the A16 modulator/splitter, acts as the local oscillator signal for the mixer. Conversion loss is approximately 9 dB at 1 GHz

A18 LOW BAND POWER AMPLIFIER

The A18 low band power amplifier is a bipolar amplifier that provides approximately 40 dB of gain and 20 dBm of output power from 0.01 to 2.3 GHz. At 20 dBm, harmonic output is less than −25 dBc.

The A18A1 low band power amplifier bias assembly provides the bias currents, the +20V, and the −10V required by the A18 amplifier. The amplifier and bias board are matched and attached at the factory; there are no adjustments or replaceable parts, and the two must be replaced together.

When you turn the RF off, or operate the synthesizer in high band, the −10V bias is removed, shutting off the amplifier.

A63 RF ATTENUATOR

The RF attenuator provides 90 dB of attenuation, in 10 dB steps. Combined with the range of the ALC loop, this gives the instrument a maximum setable power range of +20 to −110 dBm. The step attenuator functions like four fixed attenuators (one 10, one 20 and two 30 dB). Latching relays close contacts that either insert these attenuators in the RF path or bypass them.

The attenuator control and drive circuitry is located on the A24 attenuator driver assembly. Insertion loss, with 0 dB of attenuation selected, is less than 2.8 dB at 26.5 GHz.

A64 LOW BAND LOW PASS FILTER

The A64 low pass filter attenuates harmonics from A17 low band mixer that are amplified by A18, so only frequencies at or below 2.4 GHz are sampled and detected for RF leveling.

J5/J20 RF OUTPUT CONNECTOR

The J5 (front panel)/J20 (rear panel) RF output is a female type-N connector. This type has an internal 1000 pF (non-replaceable) DC-blocking capacitor. The blocking capacitor can handle up to 50 Vdc.

AT1 PERIPHERAL MODE ISOLATOR

The AT1 isolator provides 20 dB of isolation, and has less than 1 dB of insertion loss. AT1 improves the match between the high band power amplifier and the switched YTM.

AT3 ISOLATOR

The AT3 isolator improves the match between the A15 low band low pass filter and the A17 low band mixer with 20 dB of isolation. Coupled RF from the high band modulator splitter is isolated from the low pass filter, reducing any mismatch signal propagated as video feedthrough.

ALC LOOP

The ALC loop is a feedback control system that monitors RF power and maintains that power at a set level. The power can be monitored at a point inside the instrument (internal leveling), or at some point in the test setup (external leveling). Three assemblies provide control circuitry for the ALC loop:

- The A25 ALC detector assembly
- The A26 linear modulator driver assembly
- The A27 level control assembly

Several RF microcircuits are included in the ALC loop, providing the input voltages for the loop assemblies.

Leveling Loop Description

A voltage derived from the power sensor (internal crystal detector, external crystal detector, or external power meter) is compared to a reference voltage at the loop summing point (see Figure H-1). If the resulting currents at the summing node do not cancel, the loop integrator output voltage changes, causing the modulator to vary the RF output power. The power changes until the voltage representing RF power cancels the reference, at which point the integrator output stops changing and the power remains constant. The feedback loop reduces the current to the integrator to zero. Because there is one detector output voltage that causes zero integrator current for any given reference voltage, the loop controls the detector output voltage.

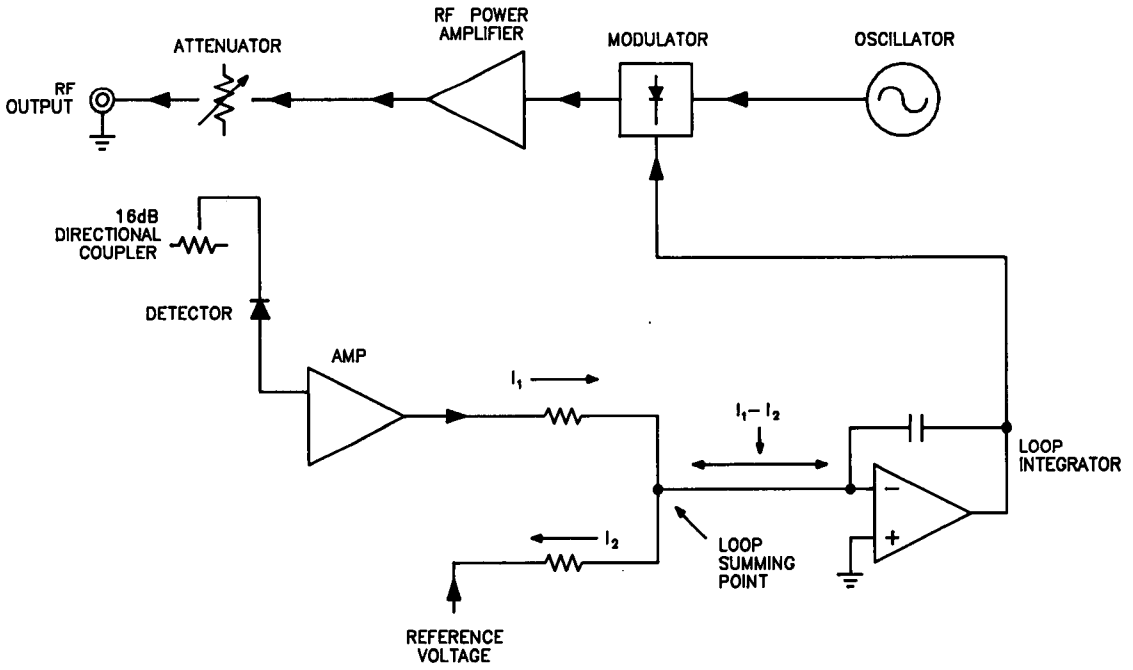


Figure H-1. Leveling Loop Simplified Block Diagram

A 16 dB directional coupler samples the RF output power. Its coupled arm produces a signal 16 dB smaller than the level of the RF output power. Any RF power coming into the instrument from the outside is ideally not coupled to the coupled arm at all, but because the 16 dB coupling factor is not perfectly flat (constant as a function of RF frequency), the detector connected to the coupled arm does couple minimal reverse power into the detector.

Because the response of the 90 dB step attenuator (10 dB steps) between the coupler and the RF output connector is not flat, as the leveling loop holds the detector output voltage constant, the RF output power varies with frequency due to the flatness of the detector, coupler, attenuator, and RF hardware. This variation can be plotted on a graph, and approximated with several straight line segments to within ±1 dB.

While the detector output voltage is a function of RF power to the detector, because the output voltage also varies with both temperature and RF frequency, forcing the detector output voltage to a particular level does not guarantee the RF power will remain constant as the temperature or frequency changes.

By making the reference voltage change as a function of frequency, this circuit can compensate for straight line variations. This is essentially what is done with the level correction voltage from the A27 level control assembly. The detector temperature characteristics are corrected by temperature compensation circuits on the A25 ALC detector assembly.

The normal range of power at the coupler output is from 0 to −10 dBm; the attenuator provides lower powers. For example, −56 dBm is produced with 50 dB of attenuation and the ALC loop set to −6 dBm.

Because of noise and drift, the ALC loop is not normally set to less than −10 dBm (the detector output is approximately 1 mV for −10 dBm RF output). The maximum attenuation is 90 dB. To go from −100 to −110 dBm, the ALC runs from −10 to −20 dBm. For power levels greater than 0 dBm, the ALC loop runs at the desired power without attenuation.

At some frequencies, the synthesizer can produce +20 dBm, the maximum ALC power. To get +20 dBm, the power amplifier is driven into saturation by approximately 10 dB. To reduce its output 30 dB (to −10 dBm), the amplifier input is reduced 40 dB by the modulators.

Modulator Attenuation

The modulator attenuation is a non-linear function of drive current. Plotted on log-log paper, the plot is straight over the high current end, and if fed from a current source that is offset approximately 1 mA, the plot of attenuation in dB versus log is straight over the entire range.

Because the ALC loop bandwidth and stability are a function of the gain and frequency response of each element in the loop, ideally, these parameters do not change with operating conditions (RF frequency and power level). Although not linear, the modulator characteristic described above lends itself to a constant gain ALC loop.

SYTM RELATED ASSEMBLIES

The three assemblies that directly provide control circuitry for the SYTM are the A22 RF clamp/SRD bias, A24 attenuator driver, and A28 SYTM driver assembly.

A22 RF Clamp/SRD Bias Assembly

The A22 assembly controls some SYTM functions:

Step recovery diode bias
RF clamp

Step Recovery Diode Bias. In band 0, the SRD (step recovery diode) is reversed biased, at +5V. In band 1, the SRD is forward biased with a negative voltage. In the higher bands, the SYTM conversion efficiency is related to the SRD DC bias voltage. Proper SRD biasing is also necessary to avoid squegging[1].

To maintain optimum SRD bias for the higher bands, the bias voltage is generated as a function of both frequency and power level. The SRD bias voltage variation is derived from 1.4V/GHz (from the A28 assembly), which is proportional to the YO frequency. The SRD bias is adjusted for power level correction with the VIDEO DETector output from the A14 power amplifier/detector microcircuit (a voltage corresponding to the power amplifier output).

RF clamp. This circuit, when engaged, helps prevent squegging. Three separate adjustments (band 1, 2, and 3) limit (clamp) the RF voltage to the SRD to prevent the YIG sphere from being overdriven.

A24 Attenuator Driver Assembly

In low band, the RF input passes unattenuated through the SYTM, and the YIG sphere is tuned by the A28 assembly to a fixed non-interfering frequency. In the high bands, the SYTM driver provides a tuning current, as described previously, while the SYTM low band RF input port is grounded to keep it from interfering with the desired high band RF output. The process of selectively grounding the low band RF signal is facilitated by the PIN diode switch in the SYTM. The PIN diode switch driver is located on the A24 attenuator driver assembly.

Temperature compensation. Because the SYTM passband drifts if the temperature varies, the YIG sphere temperature is held constant with positive temperature coefficent resistors, (located on the SYTM substrate), and supporting circuitry (on the A24 assembly).

A28 SYTM Driver Assembly

The SYTM passband must track the appropriate harmonic of the YO frequency to an accuracy of approximately 0.1%, without feedback. The primary function of the A28 assembly is to tune the center of the SYTM passband to the correct frequency for the high bands by varying the magnetic field about its YIG sphere.

The YIG sphere magnetic field is proportional to the current through the SYTM coil (with a sensitivity of approximately 15 mA/GHz), which is generated from the pretune signal from the A54 YO pretune assembly, and the latched band information from the A27 level control assembly. To track the correct YO frequency harmonic, the SYTM driver has circuitry that adds corrections to the SYTM tuning current that accounts for the effects of the nonlinear tuning curve, hysteresis, and magnetic delay.

Nonlinear Tuning Curve Compensation. The A28 SYTM driver has three breakpoint adjustments to correct the nonlinearities in the SYTM tuning curve (one fixed ; two adjustable).

Magnetic Delay Compensation. The SYTM magnet does not respond fast enough to track the correct frequency when the current drive is changed rapidly. This causes an increasingly severe delay problem as the instrument sweep rate is increased. To compensate for the slow SYTM response, the delay compensation current, which is a function of sweep rate and change in frequency from the start of sweep, adds to the SYTM tuning current.

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1. Squegging is an undesired oscillation in the A13 SYTM assembly. Symptoms of squegging are power reversal (RF power decreases as selected power is increased), power loss at specific frequencies, and spurious signals on the RF output.

SYTM Peaking

SYTM peaking tunes the SYTM such that the RF signal (YO frequency or multiple of the YO frequency) is in the center of the SYTM 1 dB passband [2], ensuring that maximum RF power is available.

To manually peak access the peaking routine (stored in ROM), press **[PEAK]**. To remotely access the peaking routine, use "RP1" (to turn peaking on) and "RP0" (to turn peaking off). When you access the peaking routine this way, it executes only if the instrument is in CW or manual mode, and the RF is on. If you access the peaking routine by pressing **[SHIFT] [AMPT MKR]**, or by remotely programming "SHAK", it executes immediately, regardless of the instrument state, but only a fine search around the most recent slope DAC setting is done. Because the SYTM passband is not tuned to track the output frequency in low band, the peaking routine does not execute if the instrument is in low band.

MODLVL is fed to the A27 level control assembly, where it becomes one input to the ADC input multiplexer. The peak routine programs the ADC multiplexer to route the MODLVL voltage to test the ADC. By monitoring the test ADC output while tuning the SYTM, the program finds the peak RF signal level.

When you select the peak function from the front panel, the instrument does a full peak (coarse and fine search) if in CW or manual. If you leave the peaking function on, the instrument repeaks every seven minutes, doing a fine search around the most recent slope DAC setting; if you change the frequency using the step or numerical entry keys the instrument performs a full peak.

Because the SYTM passband can vary with power level, peaking is done at the current ALC power level. In the fundamental band, the SYTM YIG sphere may squeg if too much power is applied. To prevent this from interfering with peaking, the maximum ALC power setting (in the fundamental only) is 0 dBm during the coarse search, and +10 dBm for the fine search. Once peaking is completed, the original power is restored.

When the instrument goes unleveled, the current driving the ALC modulator is turned off to give maximum available power. The MODLVL line still gives an indication of the detected power out of the SYTM, with a sensitivity of 30 mV/dB. The absolute voltage level shifts by about 1V when the instrument goes unleveled, but the incremental level remains valid. Because the peaking routine uses incremental changes, the absolute level shift poses no problem to the peaking routine.

SYTM Tracking. Initiate SYTM tracking by either pressing **[SHIFT] [PEAK]** on the front panel, or remotely programming "SH RP" over the HP-IB.

Each band is tracked independently. To track a band, a single band sweep is set and the sweep is stopped at several points across the band. The number stored in the calibration constant represents the least squares analysis of the straight line fit for the slope DAC numbers returned from the peaking routine. If the least squares number is out of the slope DAC range, the fault light turns on with the TRK indicator flashing.

In band 1, the SYTM is peaked at 2.3 GHz, and in 1 GHz steps from 3 to 7 GHz.
In band 2, the SYTM is peaked at 6.9 GHz, and in 1 GHz steps from 7.5 to 13.5 GHz.
In band 3, the SYTM is peaked at 13.4 GHz, and in 1 GHz steps from 14 to 20 GHz.

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2. The minimum 1 dB passband is 24 MHz. In band 3, the passband is 3 dB.

PULSE MODULATION ASSEMBLY

A21 Pulse Modulator Driver

Pulse modulation is produced by the A21 pulse modulator driver assembly driving one of the two pulse modulators. The front panel pulse modulation input is a TTL compatible input. A low signal on this input turns the RF off, and a high turns the RF on. With no connection, the pulse modulation input is internally pulled to a TTL high level.

When a low signal is present on the pulse modulation input, the A21 pulse modulator driver delivers 20 mA to one of the two pulse modulators. An output multiplexer on the A21 assembly directs the 20 mA modulator current to the A9 low band pulse modulator when the instrument is in low band, or to the pulse modulator in the A16 mod/splitter when the synthesizer is in high band.

The leveled instrument pulse modulation capability requires timing signals be sent to the ALC assemblies. The timing signals coordinate the leveling operation with the pulse operation. When a pulse is initiated, three timing signals are generated on the A21 pulse modulator driver assembly:

Sample/Hold Timing

This signal controls the sample/hold gate on the A25 detector assembly. It is adjusted to close the gate (sample) when the RF pulse is on and open the gate (hold) when the RF is off. The sample/hold output voltage represents the peak RF amplitude.

Bias Sample/Hold Timing

This signal controls the sample/hold gate on the A22 assembly. It is adjusted to close the gate (sample) when the RF pulse is on and open the gate (hold) when the RF is off. The signal keeps the SRD bias constant when the RF output is off.

Analog to Digital Converter (ADC) Timing

This signal enables the analog to digital converter on the A27 level control assembly to monitor the output of the sample/hold. The ADC is enabled when the RF is on, and for 1 ms after the RF is turned off. After 1 ms, voltage droop renders the sample/hold value inaccurate.

Integrator Timing

This signal controls the integrate and hold gate on the A26 linear modulator assembly. This gate is closed when the RF is on and stable. To speed response time for narrow pulses, the gate is held closed for a minimum of 10 µs. The sample/hold maintains a valid integrator input after the pulse is turned off

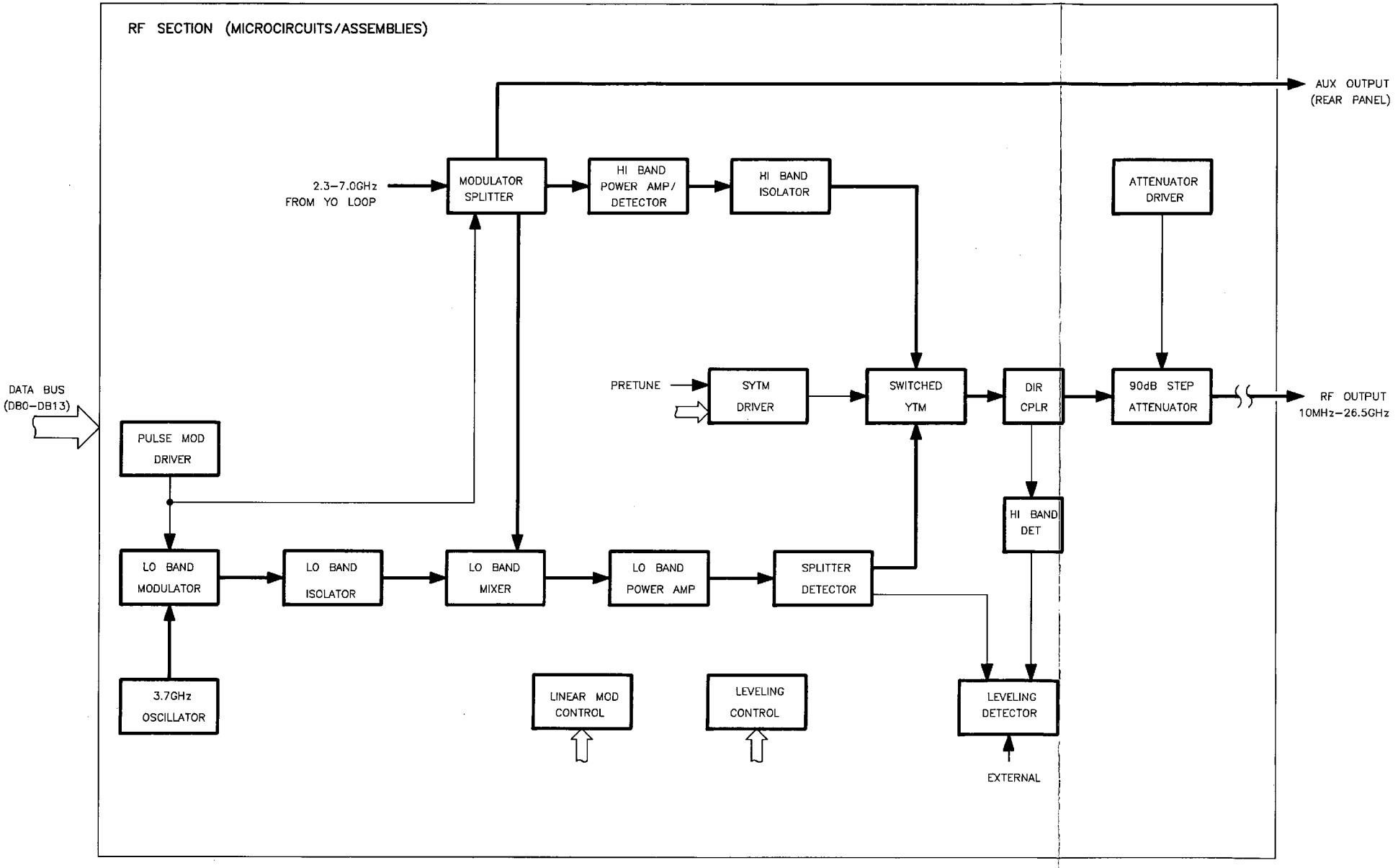


Figure H-2. RF Section Simplified Block Diagram

RF Section
Overall Assembly-Level Troubleshooting

Begin initial instrument troubleshooting in the service introduction section. Once you isolate the problem to the RF section, the troubleshooting in this section can be broken into three areas:

- SYTM peaking

  Peaking is a function designed to tune the SYTM so that the RF output is in the center of the SYTM passband, ensuring that maximum RF power is available. Use the SHIFT MANUAL sweep diagnostic to troubleshoot the peaking function.

- ALC loop

  The ALC loop is a feedback control system that monitors RF power and maintains that power at a set level. A voltage representing the RF power level is detected (internally or externally) and compared to a reference level. If the levels are unbalanced, the ALC circuitry drives the modulators and varies the RF output until the voltage levels balance. Use the SHIFT METER diagnostic to open the ALC loop for troubleshooting.

- RF path

  The RF path consists of 14 RF microcircuits and their associated bias assemblies. To troubleshoot the RF path, initialize the instrument to a known state and measure the RF power levels at various junctions in the path. Minimum power levels are provided for each microcircuit on the RF path troubleshooting block diagram.

TROUBLESHOOTING SEQUENCE

Troubleshoot the RF section in an ordered sequence to systematically isolate assemblies:

1. SYTM peaking problems
2. ALC loop problems
3. RF path problems

Each troubleshooting sequence leads to the next. What may appear to be an ALC loop fault, for example, may actually be an RF path (microcircuit) failure. By completing the ALC loop diagnostics, the RF path failure is indicated, leading you to the RF path troubleshooting procedures.

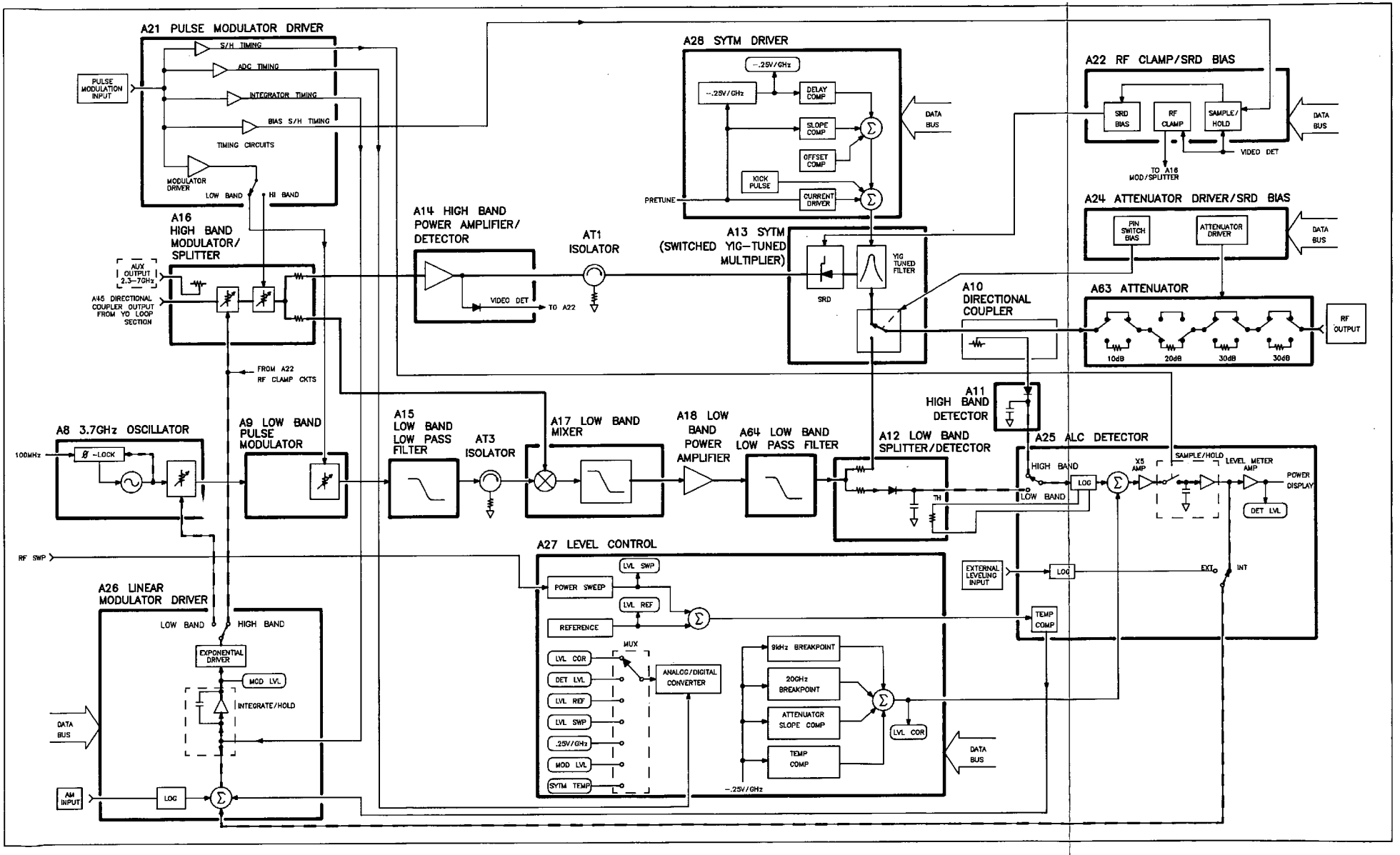


Figure H-3. RF Section Overall Block Diagram

SYTM Peaking Assembly-Level Troubleshooting

THE FAULT ANNUNCIATOR COMES ON

If the FAULT annunciator comes on, determine the function that caused the fault as follows:

1. Press **[INSTR PRESET] [SWEEPTIME] [1] [SEC] [SHIFT] [MANUAL]**.

   If the peak or tracking indicator is flashing, the peaking routine failed to find a peak within the range of the SYTM slope DAC. This can be caused by:

   a. The A28 SYTM driver assembly may not be shifting the passband.
   b. There may not be enough power from the SYTM for proper ALC operation.
   c. The A16 ALC modulator may be defective.

   If the instrument won't auto track properly (no fault indication), the problem may be:

   a. The ALC loop is not leveling.
   b. The ALC loop is oscillating during leveling.
   c. The YO endpoints are off (lock and roll errors).

2. Look at the CMP test point (A28TP3) for an indication of how the slope DAC is varying slope compensation (see Figure H-4 for a typical CMP waveform). If the waveform is incorrect, the A28 assembly is the most probable fault.

3. Check the MODLVL test point (A26TP3). Refer to Figure H-5 for a typical MODLVL waveform.

4. Check the MOD test point (A26TP5). See Figure H-6 for a typical MOD waveform. If either the MODLVL or MOD signal is significantly different from Figures H-5 and H-6, the most probable cause is the A26 assembly.

5. To clear the fault annunciator, press **[INSTR PRESET]**, or turn the line power off then on.

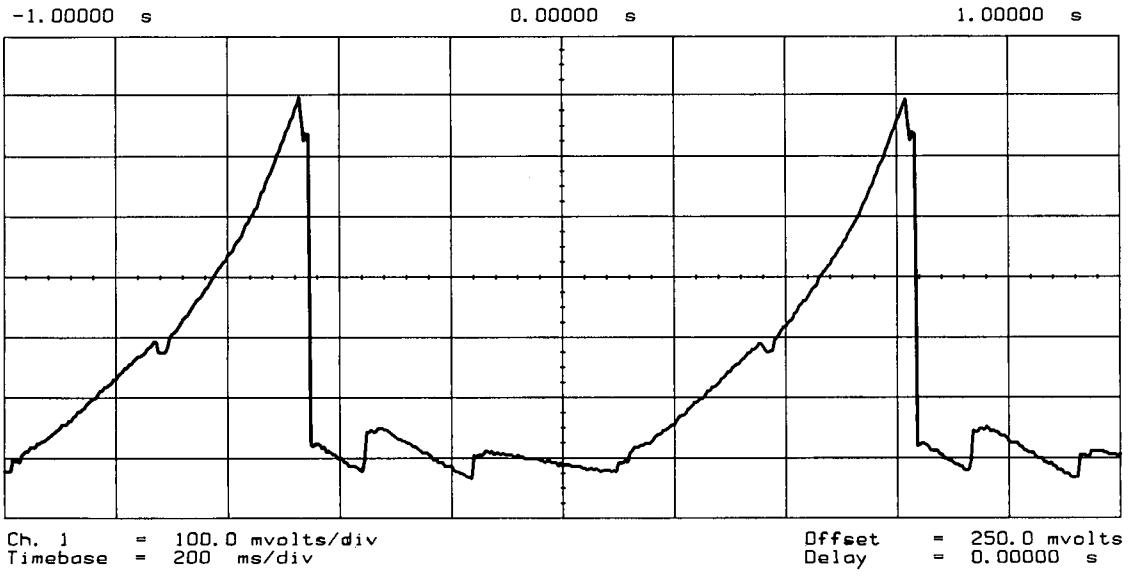


Figure H-4. Typical CMP Waveform

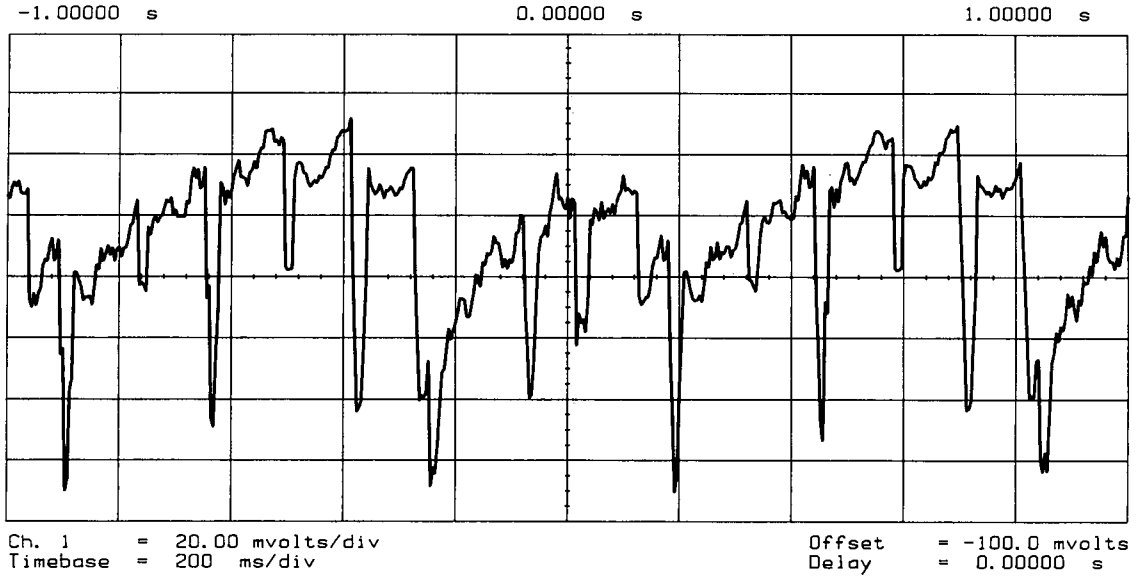


Figure H-5. Typical MODLVL Waveform

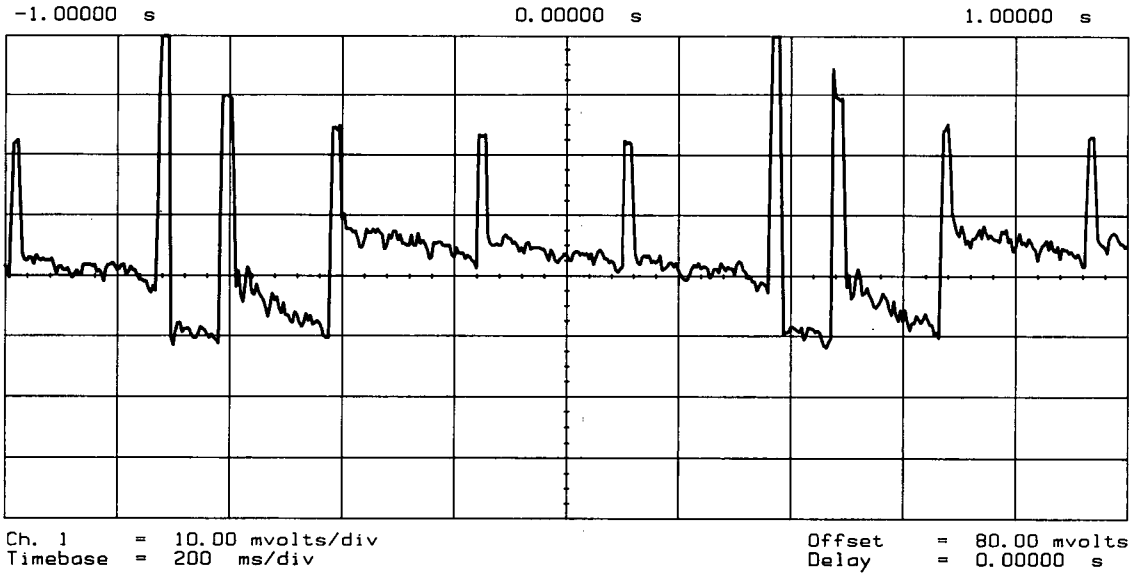


Figure H-6. Typical MOD Waveform

ALC Loop
Assembly-Level Troubleshooting

To troubleshoot the ALC loop, you can break the loop and inject a signal that you can trace around the loop.

In the ALC loop troubleshooting mode, FET switches break the connection from the A25 ALC detector assembly to the A26 linear modulator assembly). A resistor (A26R17) is switched across the integrator capacitor on the A26 linear modulator assembly, converting this stage to an inverting amplifier. In this way, the integrator output can be controlled via the reference DAC, and the signal traced from there to the modulator driver, RF output, detector output, logger output, X5 amplifier, through the sample and hold, level amplifier, and to the analog-to-digital converter driving the level meter.

1. To enter the test mode, press **[INSTR PRESET] [CW] [SHIFT] [METER]**.

   The UNLEVELED annunciator should be on. The POWER dBm display should indicate the approximate RF output power. The ENTRY display should indicate **ATN: −00, MOD: 0.0 dB**.

   The modulators are controlled by the control voltage MODLVL, on the A26 assembly. This voltage is programmed by the A27 level control assembly ALC reference generator DAC. The DAC can be controlled using the RPG.

2. Rotate the front panel knob CCW and note that the ENTRY display MOD level changes.

3. Continue turning the front panel knob CCW until the POWER dBm display begins to change.

   The absolute MOD level indication is not important, but a further decrease in MOD level should generate a corresponding decrease in the POWER dBm display, and the RF output power. For example, a 10 dB MOD level change should generate a 10 dB ±3 dB power change.

4. Isolate a defective assembly by tracing the voltage from the MODLVL output to the modulators, or by tracing the voltage from the high and low band detectors to the level meter amplifier output on the A25 ALC detector assembly. The AM signal path (on the A26 assembly) must be checked separately. Refer to Figure H-7.

5. Attach an oscilloscope or DVM to the MODLVL test point (A26TP3) and vary the front panel knob.

   The voltage level should vary between +0.5 (ENTRY display MOD level at 0.0 dB) and −2.50 Vdc (ENTRY display MOD level at −100 dB).

6. Attach an oscilloscope or DVM to the MOD test point (A26TP5) and vary the front panel knob.

   The voltage level should vary between −0.25 (ENTRY display MOD level at 0.0 dB) and +1.00 Vdc (ENTRY display MOD level at −100 dB). The signal should vary exponentially with the front panel knob.

7. If either MODLVL or MOD are incorrect, the A26 linear modulator assembly is the most probable cause. You can measure RF levels at various points in the RF path, and power levels should vary with the front panel knob.

   If the A26 assembly signals (MODLVL and MOD) are good, and the RF measurements are not correct (as indicated by the RF power display on the front panel), refer to the RF path troubleshooting procedures for microcircuit assembly isolation.

8. Check the voltage level at the A25 assembly input (A25TP1). The level should be approximately 9.4V, and not vary.

9. Attach an oscilloscope or DVM to the output of the X5 amplifier (A25TP2). The voltage level should vary between +0.50 and −1.00V as you vary the front panel knob.

   At 0.0 dBm (on the front panel power display), the voltage level should be 0.0V, and vary at a 30 mV/dB rate.

10. Measure the voltage at the level meter amplifier output (A25TP4). The voltage level should vary between −3.5 and +5.0V as you turn the front panel knob.

    At 0.0 dBm (on the front panel power display), the voltage level should be 0.0V, and vary at a 200 mV/dB rate.

11. If any of the A25 assembly voltage levels are incorrect, replace the A25 assembly.

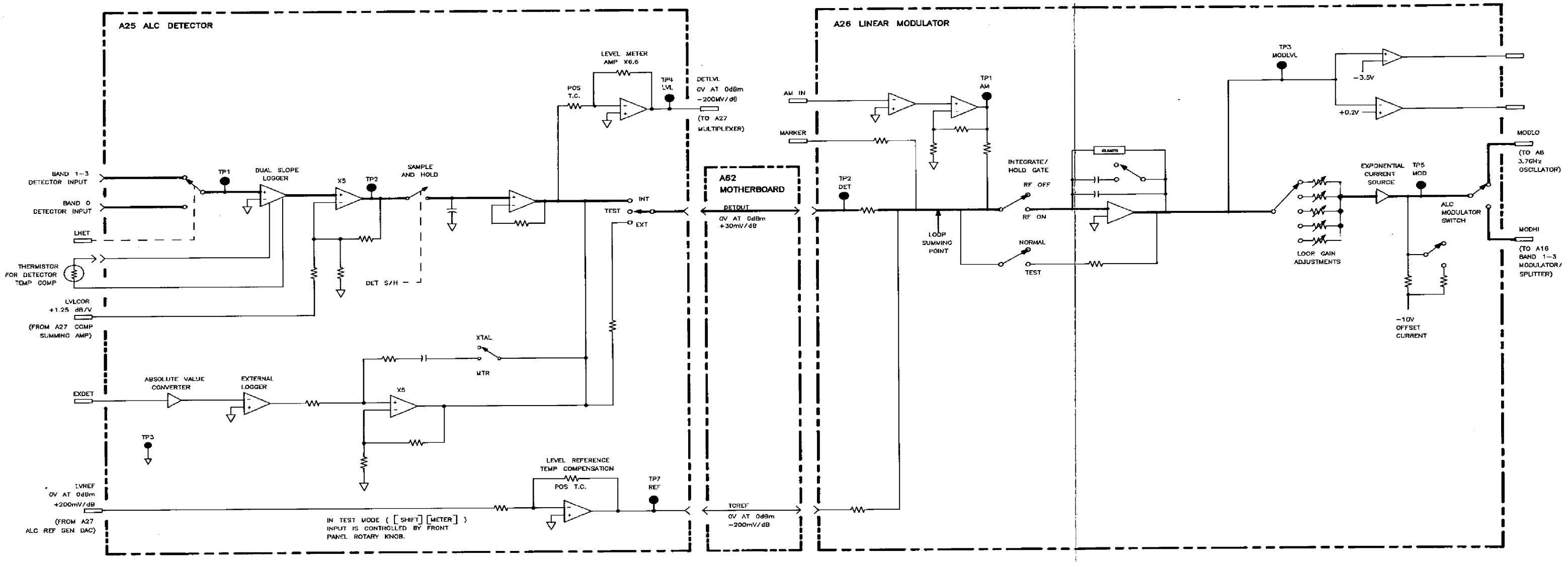


Figure H-7. ALC Loop Detailed Block Diagram

RF Path
Assembly-Level Troubleshooting

RF path troubleshooting consists of checking the power output of each microcircuit against the limits specified on the RF path block diagram. Because the ALC loop is open during power measurements, the instrument is in an unleveled condition.

NOTE: The acceptable power limits for each microcircuit in the RF path are dependent on a specified input level. The minimum input levels are indicated on the block diagram.

1. To initialize the instrument, press **[INSTR PRESET] [CW] [XX.XX] [GHz]**.
   The actual frequency depends on whether you wish to check the low or high band.
2. To put the instrument in an unleveled condition, press **[XTAL]** leveling.
3. Check the RF path frequency dependence across all bands by controlling the frequency with the front panel knob. Verify the full frequency bands.

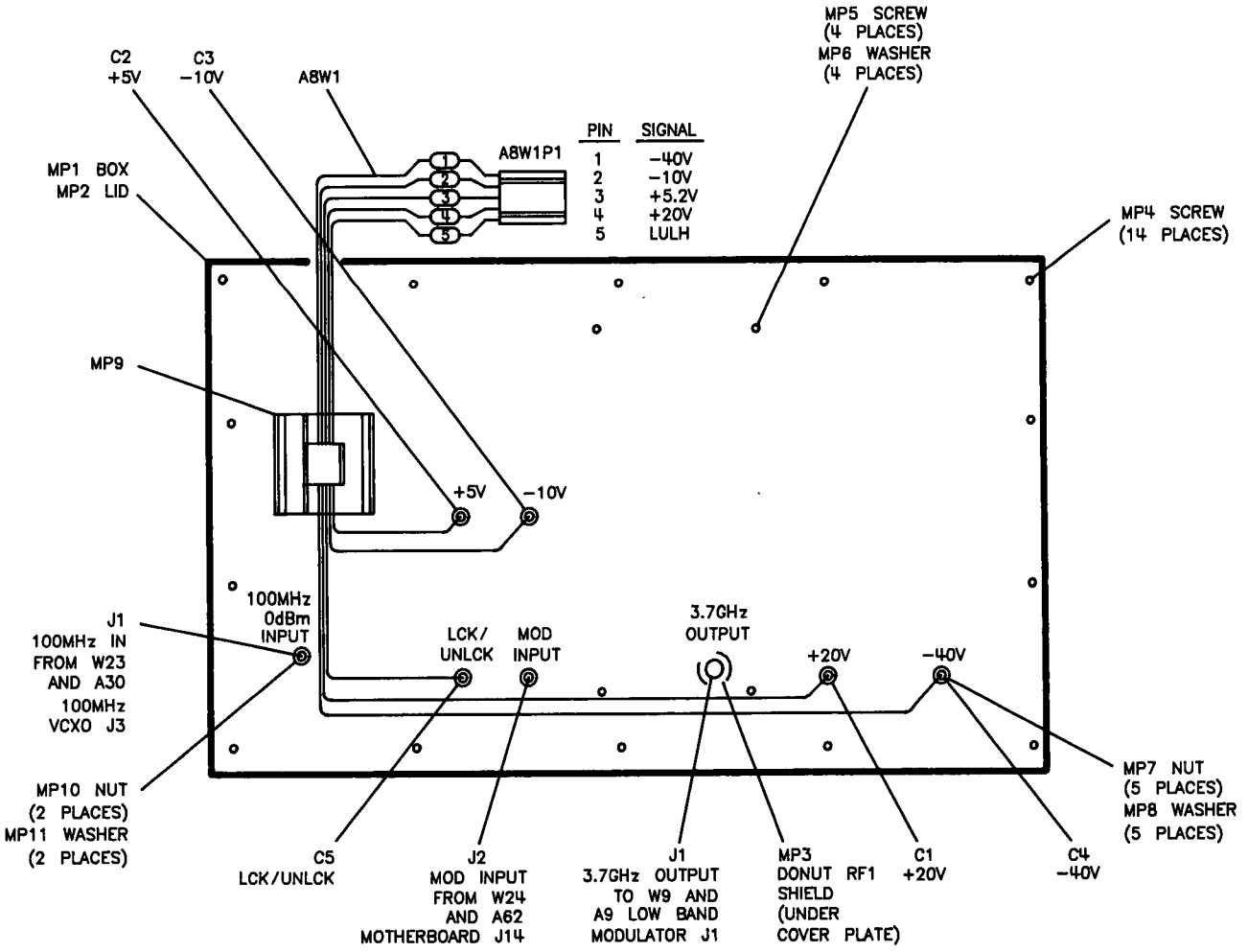


Figure H-8. A8 3.7 GHz Oscillator

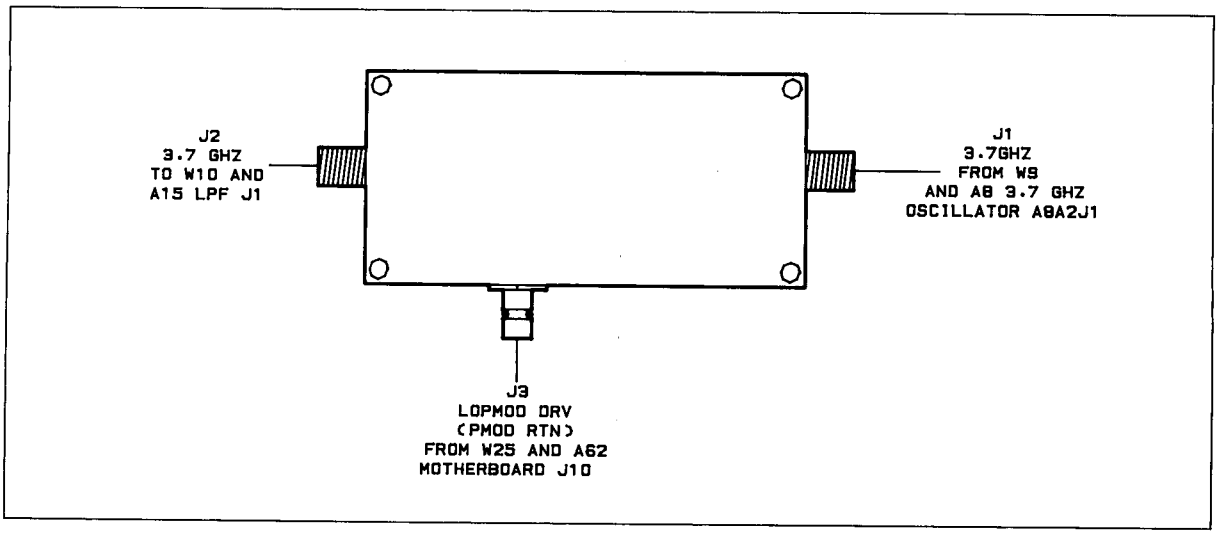


Figure H-9. A9 Low Band Pulse Modulator

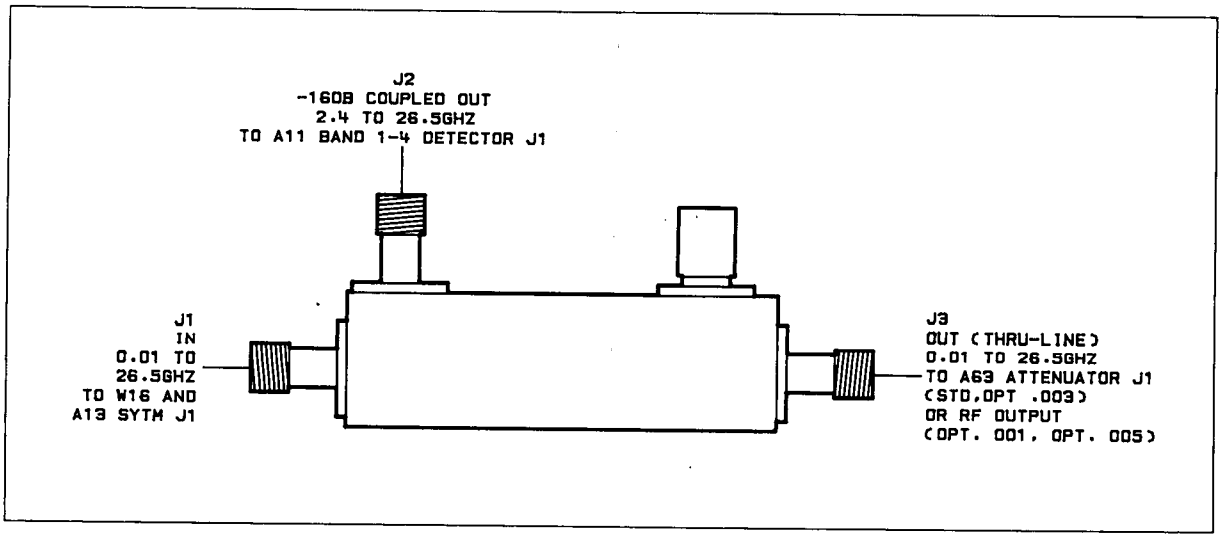


Figure H-10. A10 Directional Coupler

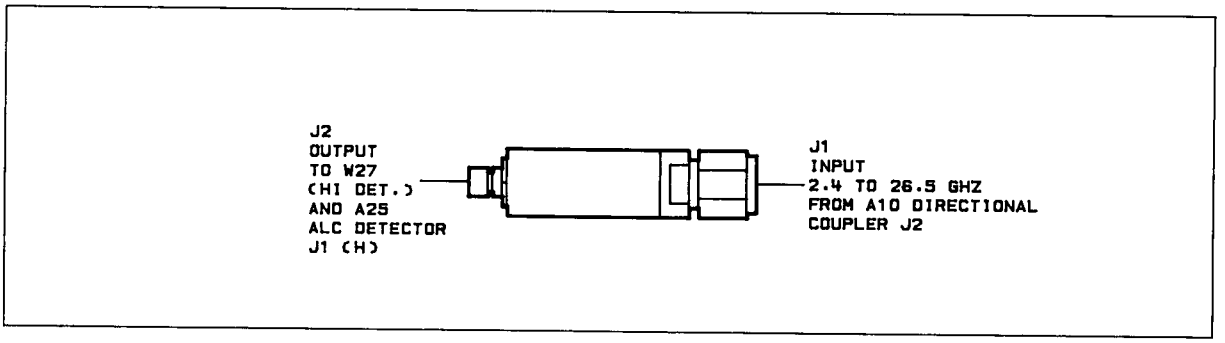


Figure H-11. A11 High Band Detector

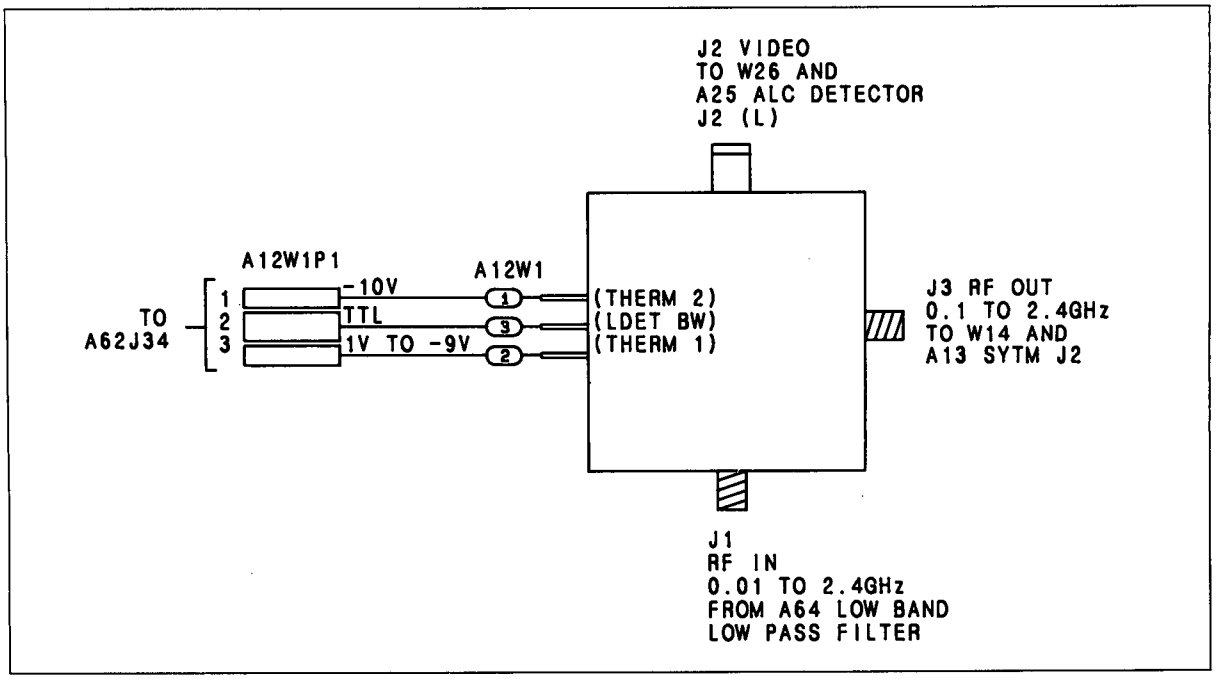


Figure H-12. A12 Low Band Splitter Detector

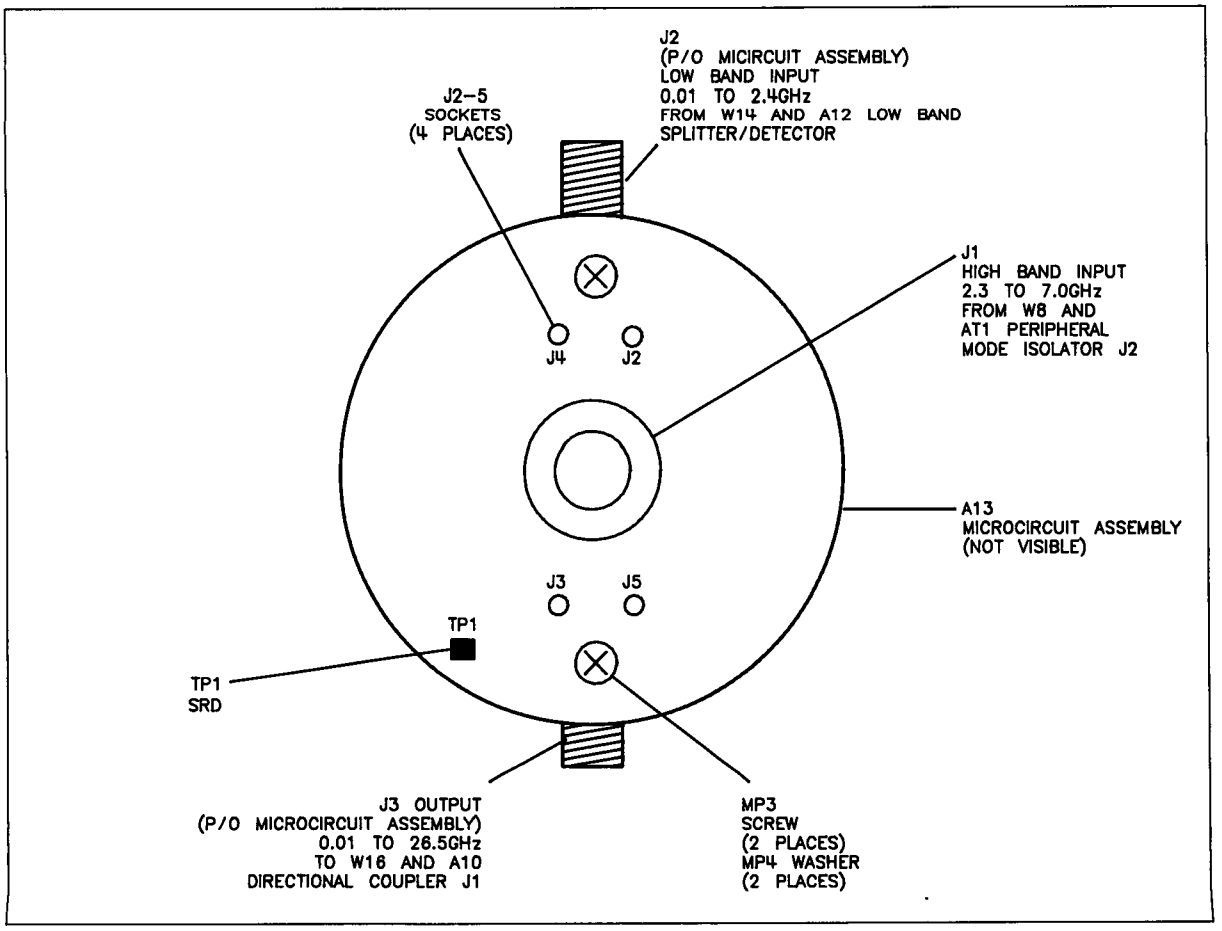


Figure H-13. A13 SYTM

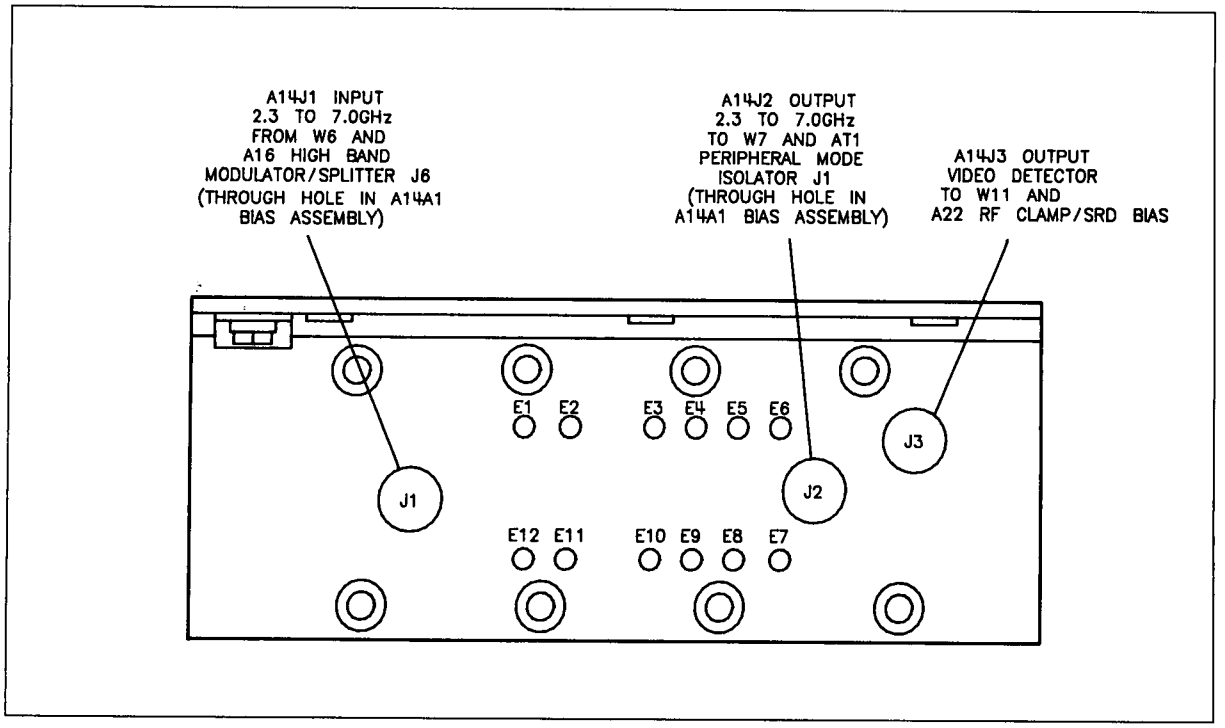


Figure H-14. A14 High Band Power Amplifier

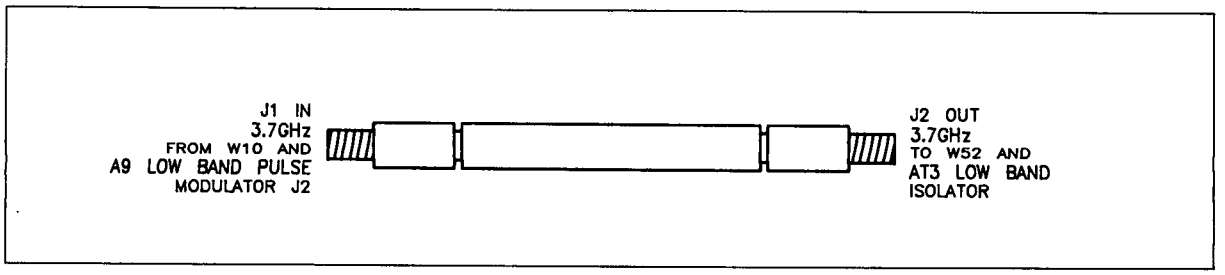


Figure H-15. A15 Low Band Low Pass Filter

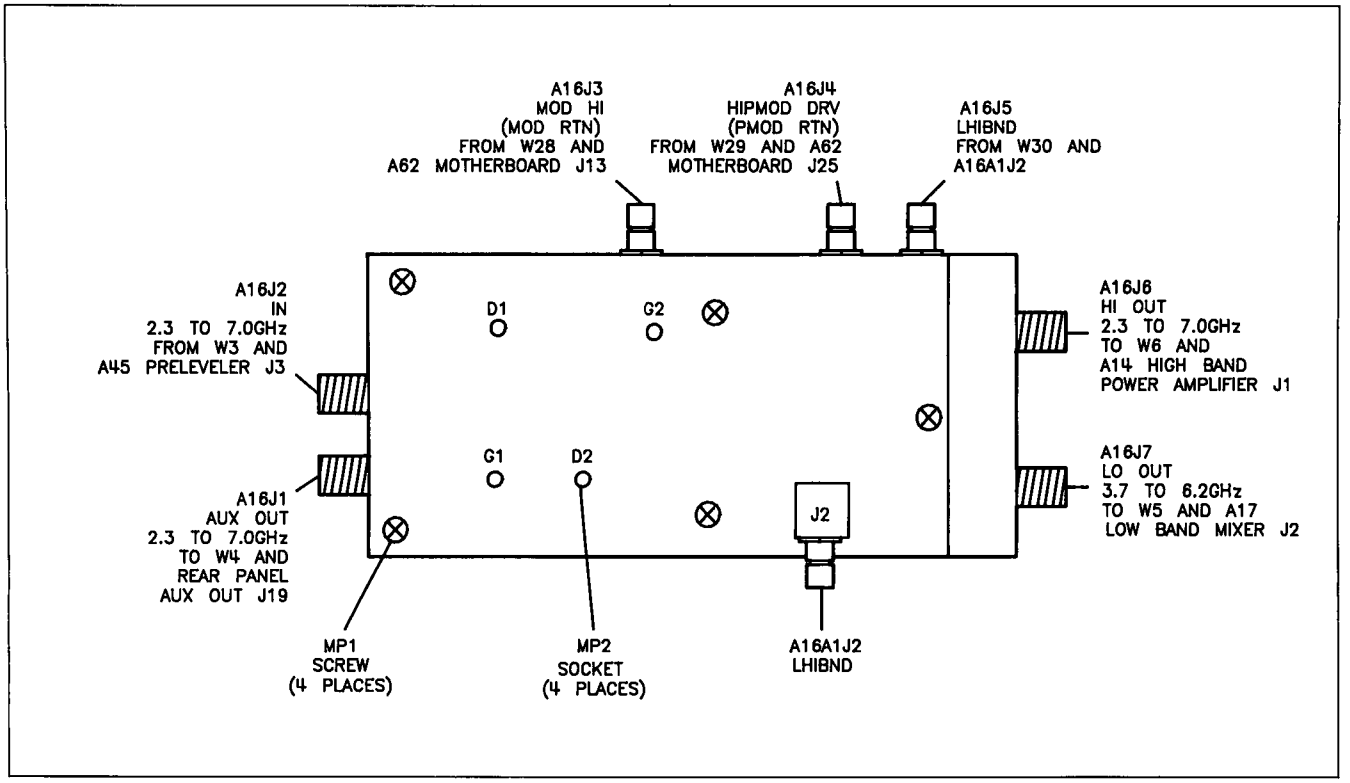


Figure H-16. A16 High Band Modulator/Splitter

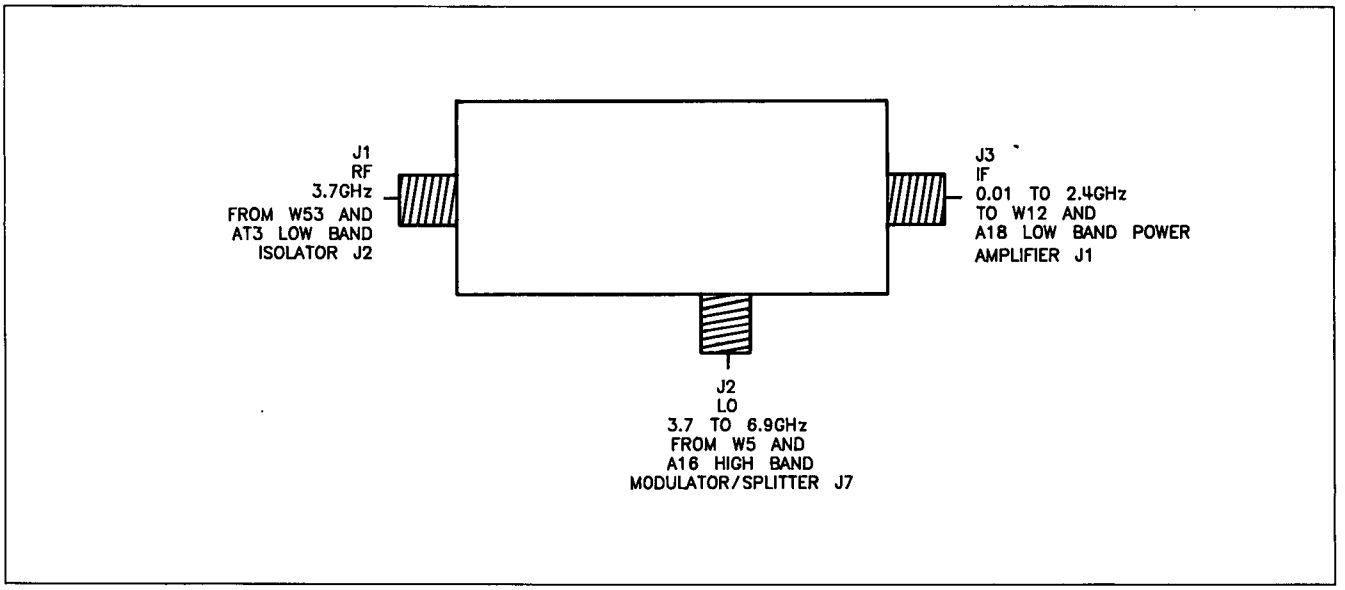


Figure H-17. A17 Low Band Mixer

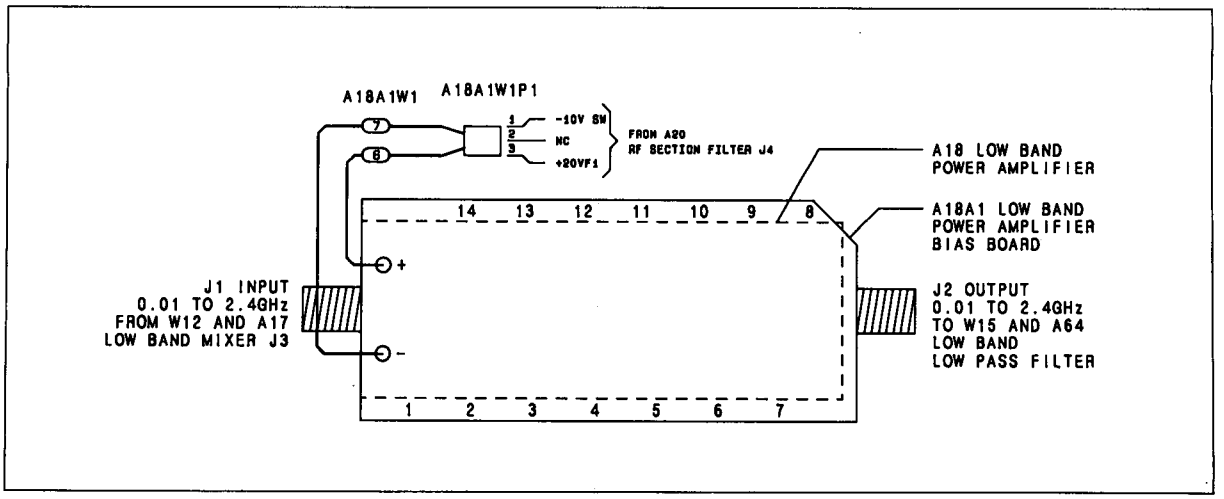


Figure H-18. A18 Low Band Power Amplifier

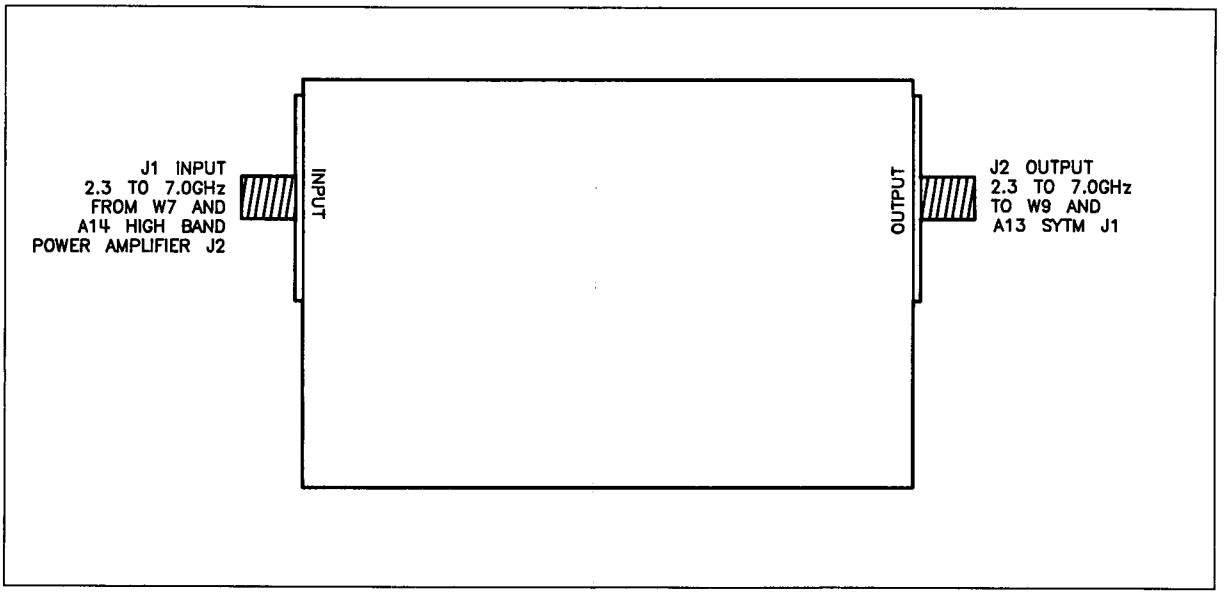


Figure H-19. AT1 Peripheral Mode Isolator

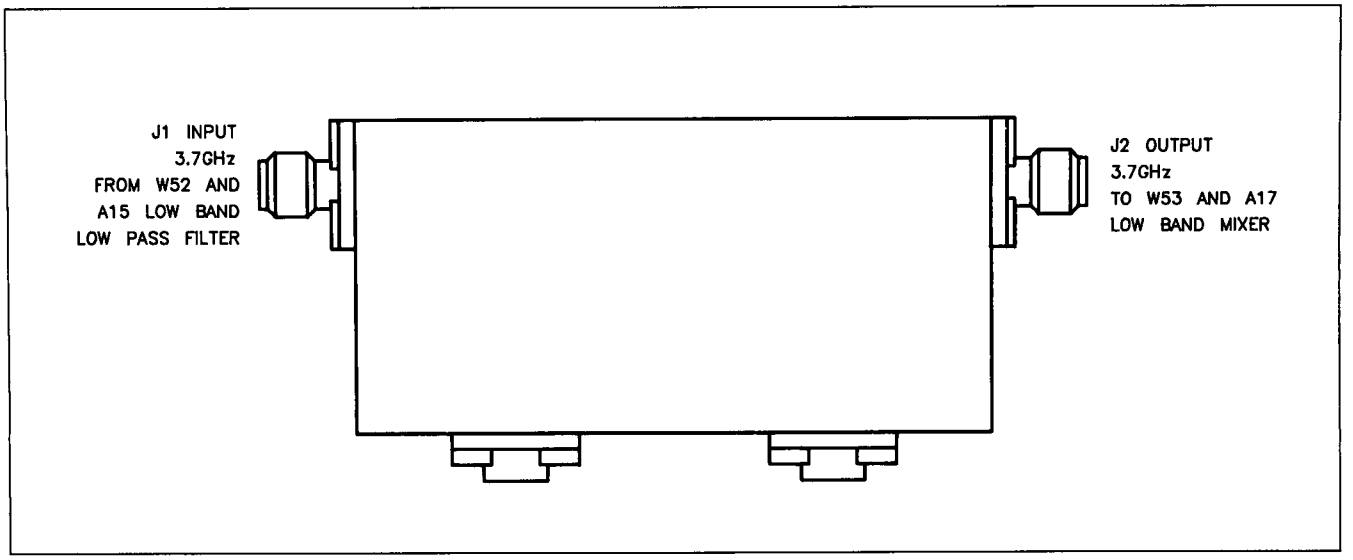


Figure H-20. AT3 Isolator

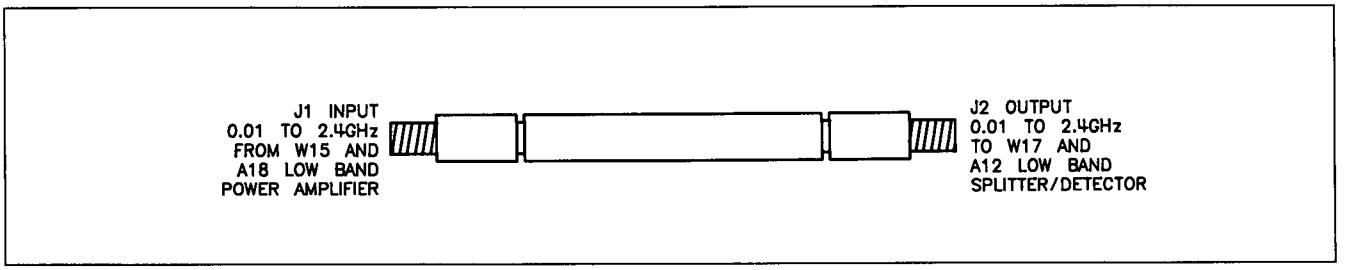


Figure H-21. A64 Low Band Low Pass Filter

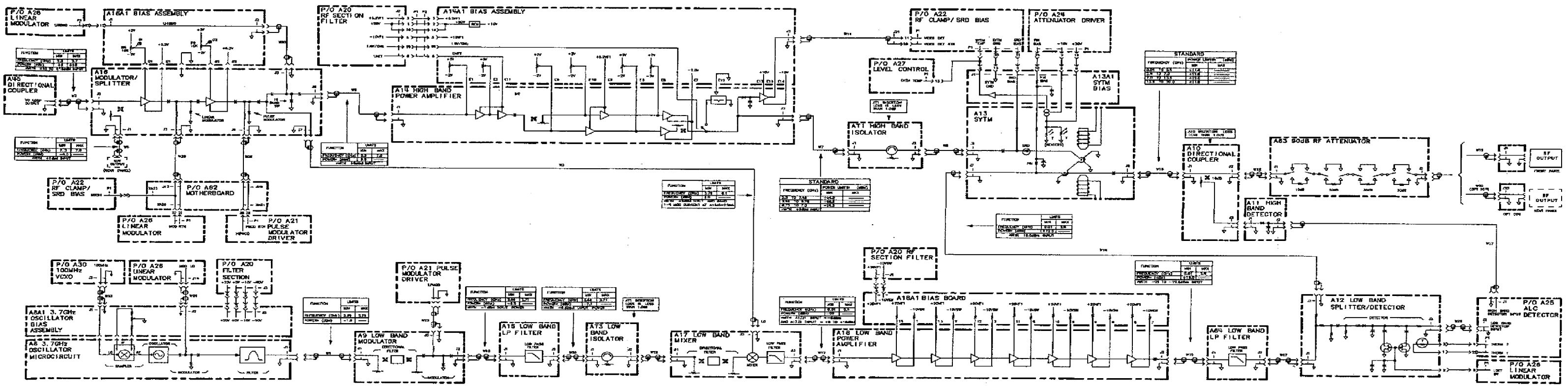


Figure H-22. RF Section Detailed Block Diagram

RF Section
Repair Procedures

This section contains information on:

- The module exchange program
- Removal/installation procedures for the RF assemblies

MODULE EXCHANGE PROGRAM

The A8 through A18, A63, AT1, and AT3 assemblies are not field repairable. Of these, the A8, A9, A13, A14, A16, A17, and A18 assemblies are available through the module exchange program.

The programs lets you exchange a defective module for a fully tested and guaranteed restored-exchange module at a reduced price (contingent on the return of the defective module).

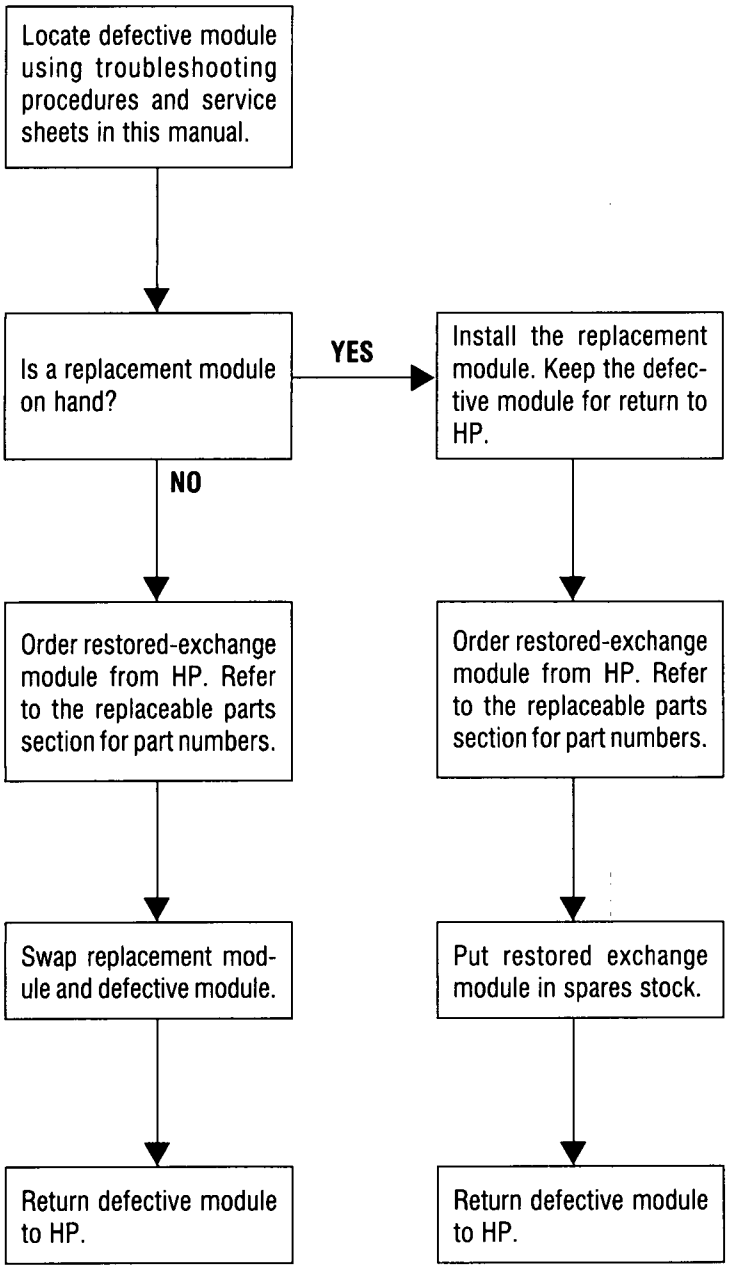
Figure H-23 illustrates the module exchange program. When you locate a defective module:

1. Order a replacement through the nearest Hewlett-Packard sales office (see Table H-2). A restored exchange module will be sent immediately, directly from a customer service replacement parts center.

2. When you receive the exchange module, return the defective module in the same special carton in which the exchange module arrived. DO NOT return the defective module until you receive the exchange module.

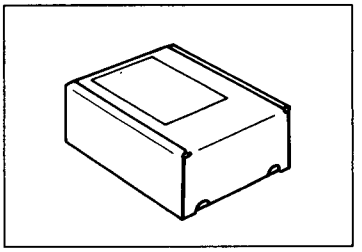
If you do not wish to return the defective module to Hewlett-Packard, or if you are ordering a module for spare parts stock, etc, order a new module.

The module exchange program described here is a fast, efficient, economical method of keeping your Hewlett-Packard instrument in service.



*HP pays postage on boxes mailed in U.S.A.

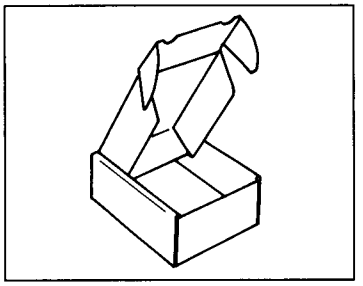
A.



Restored-exchange modules are shipped individually in boxes like this. In addition to the circuit module, the box contains:

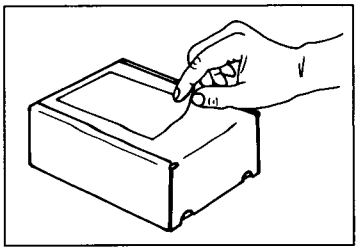
Exchange assembly failure report
Return address label

B.



Open box carefully - it will be used to return defective module to HP. Complete failure report. Place it and defective module in box. Be sure to remove enclosed return address label.

C.



Seal box with tape. Inside U.S.A.*, stick preprinted return address label over label already on box, and return box to HP. Outside U.S.A., do not use address label; instead address box to the nearest HP office.

Figure H-23. Module Exchange Procedure

DISASSEMBLY PROCEDURES

Equipment Required

	HP Part Number
Large Pozidriv (2 PT)	8710-0900
Small Pozidriv (1 PT)	8710-0899
5/16 Wrench	8720-0015
1/4 Nut Driver (A8 & A9 assemblies only)	8720-0002
5/16 Special Wrench (A8 & A15 assemblies only)	08555-20097
7/32 Wrench (A15 assembly only)	8710-0534

Introduction

Two types of procedures follow:

1. The assemblies that can be removed after disconnecting attached cables or wires and mounting hardware.
2. The assemblies that require that you open the hinged RF deck to access either whole assemblies or part of the mounting hardware.

   A13 high band SYTM
   AT1 high band peripheral mode isolator

In order to perform any of the following procedures:

1. Remove the instrument top, bottom, and perforated side covers.
2. Place the instrument on its left side (as viewed from the front).

CAUTION

A10J1, A10J2, and A10J3 are precision 3.5 mm connectors. The cables and the high band detector assembly that connect to them use SMA connectors. Take extreme care when connecting or disconnecting an SMA cable and a precision 3.5 mm connector.

A8 3.7 GHz Oscillator Replacement Procedure

Refer to Figure H-25, view C, for related assemblies, cables, and mounting hardware locations.

1. Disconnect W10 from the A15 assembly. You may have to place a special 5/16 inch slotted box end wrench (see equipment required, above) on A15J2 to keep the A15 assembly from turning when you remove W10 from A15J1.
2. Using a standard 5/16 inch wrench, disconnect W10 from A9. Remove W10 completely and set aside.
3. Disconnect A8W1 from the A20 assembly.
4. Disconnect W15 from the A18 assembly.
5. Disconnect W17 from the A64 assembly and slide the A64 assembly, with W15 rigid coax cable still attached, towards the front panel, so as to expose two screws mounted on the RF deck casting.

HINGED RF DECK ACCESS PROCEDURE

Instrument Bottom

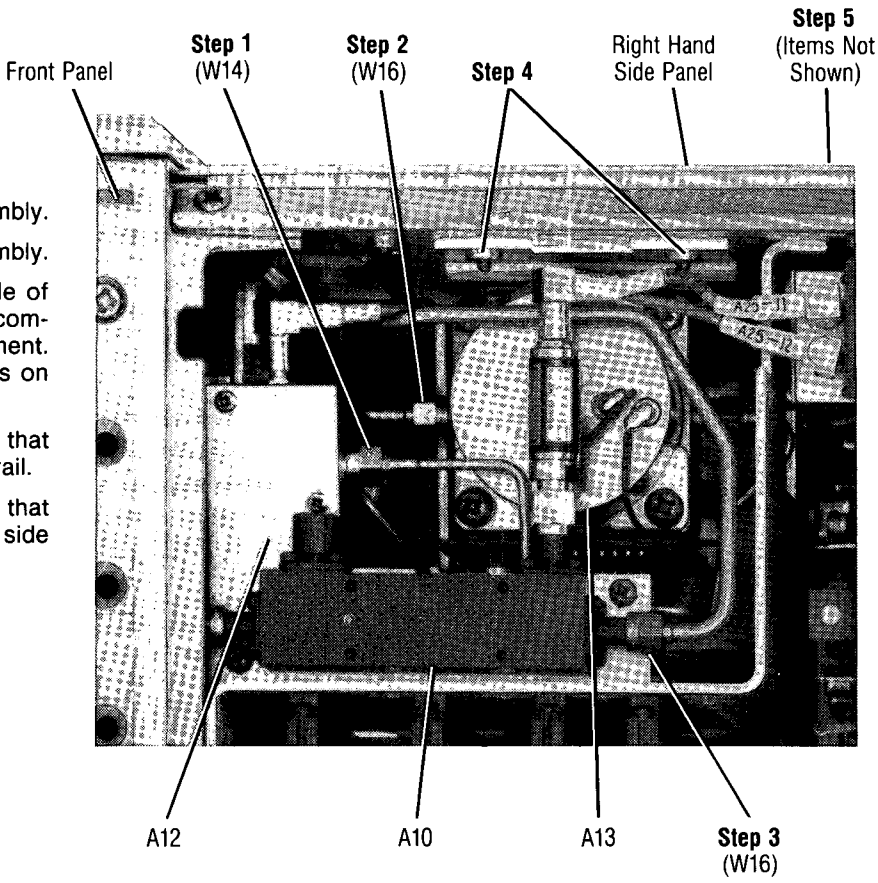
1. Disconnect W14 from the A12 assembly.
2. Disconnect W16 from the A13 assembly.
3. Carefully disconnect the other side of W16 from the A10 assembly and completely remove W16 from the instrument. Avoid twisting and turning motions on the W16 to A10J1 connection.
4. Remove the two side panel screws that hold the A13 assembly to the side rail.
5. Remove the two side panel screws that hold the A14 power amplifier to the side rail. (Refer to Figure H-25 View A.)

Instrument Top

6. Disconnect W3 and W4 from the A16 assembly.
7. Disconnect W17 from the A12 assembly.
8. Remove the two screws from the RF deck.
9. Remove the screw holding the casting to the motherboard.
10. Gently swing the RF deck open.

CAUTION

To avoid crushing A20 components mounted near the RF deck hinge, do not open the RF deck more than 45° from its original position.



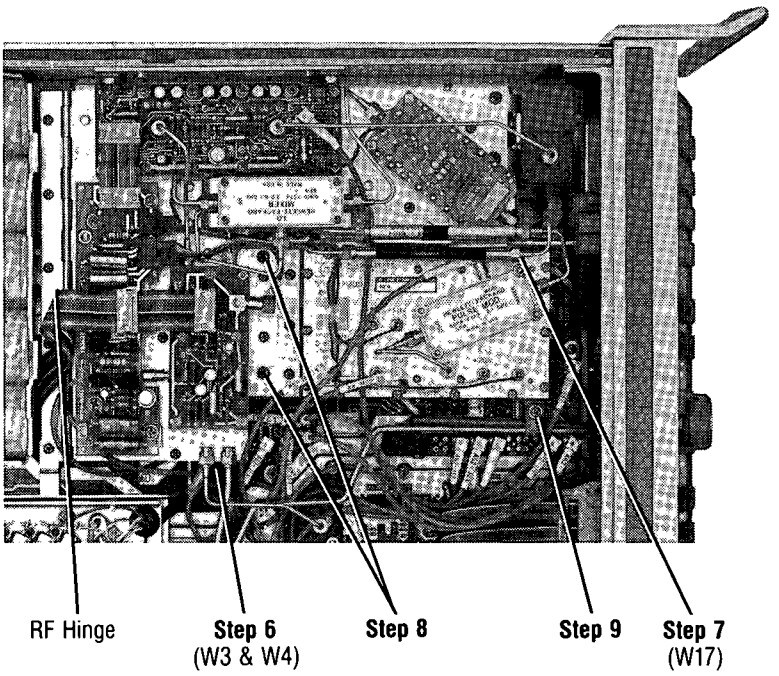


Figure H-24

6. Remove the five screws (item 2) that hold the combined A8 and A9 assemblies to the RF deck.
7. Remove the screw (item 3) that holds the A8 casting to the A62 motherboard. Note that this screw is longer than the five other screws (item 2).
8. Remove as necessary any cables connecting the A8 and A9 assemblies to the A62 motherboard.
9. Carefully remove the A8/A9 assembly from the instrument.
10. Remove W9 completely. When loosening W9 from A9J1, do not damage the −10V terminal on the A8 assembly with the wrench.
11. Separate the A8 and A9 assemblies, using a 1/4 inch nut driver to remove the four nuts at the corners of the A9 assembly.
12. To install a new A8 assembly, reverse the above procedure. When re-installing W10, completely tighten one end before you start the other.

A9 Low Band Pulse Mod Replacement Procedure

Refer to Figure H-25 for related assemblies, cables, and mounting hardware locations.

1. Disconnect W10 from the A9 assembly. You may have to place a special 5/16 inch slotted box end wrench (see equipment required, above) on A15J2 to keep the A15 assembly from turning when you remove W10 from A15J1.
2. Using a standard 5/16 inch wrench, remove W10 from A15J1.
3. Disconnect W9 from the A9 assembly by first loosening its connection to the A8J1 connector.
4. Remove the connection to A9J1 (LO PLS MOD) carefully, do not damage the −10V terminal on the A8 assembly.
5. Separate the A8 and A9 assemblies, using a 1/4 inch nut driver to remove the four nuts at the corners of the A9 assembly.
6. To install a new A9 assembly, reverse the above procedure.

A10 Directional Coupler

Refer to Figure H-25 for related assemblies, cables, and mounting hardware locations.

CAUTION

A10J1, A10J2, and A10J3 are precision 3.5 mm connectors. The cables and the high band detector assembly that connect to them use SMA connectors. Take extreme care when disconnecting or connecting an SMA cable and a precision 3.5 mm connector. The SMA cable center conductor must align with the 3.5 mm connector center conductor. Any axial force on the cable when you disconnect the SMA fitting can damage the 3.5 mm connector center conductor, and the A10 directional coupler will have to be replaced. Remove the axial force on the cable by first disconnecting the end of the cable that does not mate with the 3.5 mm connector, or by removing the A10 assembly mounting screws. Do both where possible. The A11J1 connector has a captured nut that does not allow axial force on the precision 3.5 mm center conductor until well after the SMA center conductor is disengaged.

1. Disconnect W17 from the A64 assembly (Figure H-25, view C).
2. Disconnect W14 and W26 from the A12 assembly (Figure H-25, view B).
3. Using a small pozidriv, remove the two screws that hold the A12 assembly (item 13).
4. With W17 attached, remove the A12 assembly.
5. Referring to the front panel – rear panel functional group, remove the front panel. You don't need to remove the ribbon cables.
6. Remove the two screws (item 6) that hold the A10/A12 assembly mounting bracket.
7. Remove the high band detector assembly (A11) from A10J2.
8. Remove the W16 cable from the A13 SYTM assembly.
9. Carefully remove the other end of W16 from the precision 3.5 mm A10J1 connector.
10. Carefully remove the cable from the A10J3 connector (near the front panel). Avoid axial force on the cable.
11. Pull the A10/A13 mounting bracket out far enough to access the screws that hold the A10 assembly in place, and remove the screws.
12. To install a new A10 assembly, reverse the above procedure. With the front panel removed, the cable going to A10J3 is accessible through the front of the instrument.

A12 Low Band Detector

Refer to Figure H-12 for related assemblies, cables, and mounting hardware locations.

1. Disconnect W17 from the A64 assembly (Figure H-25, view C).
2. Disconnect W14 and W26 from the A12 assembly (Figure H-25, view B).
3. Using a small pozidriv, remove the two screws that hold the A12 assembly (item 13).
4. With W17 attached, remove the A12 assembly.
5. Disconnect W17 and unsolder the three wires attached to the A12 assembly.
6. To install a new A12 assembly, reverse the above procedure.

A13 High Band SYTM Replacement Procedure

Refer to Figure H-24, Figure H-25, and Figure H-26 for related assemblies, cables, and mounting hardware locations.

1. Using the Hinged RF Deck Access Procedure, Figure H-24, open the hinged RF deck assembly.

NOTE: When you remove the ribbon cable from A13A1 (below), note its proper orientation. If you put this cable on backwards, all the power supplies shut down.

2. Remove W8 from AT1J2.
3. Using a small, flat tool, gently pry up the ribbon connector (W33) from A13A1J1. Note the original orientation. Do not pull the ribbon cable off by hand; this can badly bend the pins.
4. Disconnect W8 from A13J1, and remove it from the instrument. Do not bend the small terminals on the A13A1 assembly with the wrench.
5. Completely remove W14, which connects A13J2 to A12J2.
6. Holding the A13 assembly, remove the two screws (item 8) shown in Figure H-25.
7. When replacing the A13 assembly, apply a thin, continuous layer of thermal compound (HP Part Number 6040-0454, CD0) to each side of the A13MP1 aluminum spacer between the SYTM and the RF deck.

CAUTION

Do not use silicone based thermal compound. Silicone based oil migrates past element sockets, switch contacts, or printed circuit board edge connectors, raising contact resistance, or electrically isolating the contacts. Silicone based thermal compounds disperse into the air, depositing themselves anywhere in the instrument. Heat increases the rate of dispersion.

AT1 Replacement Procedure

Refer to Figure H-25, view D for related assemblies, cables, and mounting hardware locations.

1. Using the Hinged RF Deck Access Procedure, Figure H-24, open the hinged RF deck assembly.
2. Remove W7 and W8 from the AT1 assembly.
3. Remove three of the the four screws shown in Figure H-25, view D.
4. When removing the fourth screw, hold the AT1 assembly.
5. Ensure that W7 and W8 are clear of AT1J1 and AT1J2 when you remove the AT1 assembly.
6. To install a new assembly, reverse the above procedure.

AT3 Replacement Procedure

Refer to Figure H-25, view C for related assemblies, cables, and mounting hardware locations.

1. Remove the four screws on the A17 assembly (one on each corner).
2. Disconnect W52 from the A15 assembly.
3. Disconnect W6 from the A14A1 and A16A1 assemblies, and remove it from the instrument.
4. Disconnect W5 and W12 from the A17 low band power amplifier, and remove the A17/AT3 assemblies.
5. Disconnect W53 from the amplifier, separating the A17 and AT3 assemblies.

6. Remove W53 and W52 from the isolator.

7. Note the orientation of the isolator (the out port is to the left when viewed from the top). Remove the two screws holding the isolator mounting plate.

8. To Install a new assembly, reverse the above procedure.

A14/A14A1 High Band Power Amplifier Replacement Procedure

Refer to Figure H-25 for related assemblies, cables, and mounting hardware locations.

1. Remove the ribbon cable going to A14A1, and completely remove W7.

2. Disconnect W6 from A14.

3. To disconnect W6 from A16, first disconnect A8W1. Remove W6.

4. Remove the eight screws that hold the A14/A14A1 assembly together.

5. To install a new A14/A14A1 assembly, reverse the above procedure. When reconnecting the ribbon connector, be extremely careful not to bend the pins.

A15 Low Band Low Pass Filter Replacement Procedure

Refer to Figure H-25 for related assemblies, cables, and mounting hardware locations.

1. Remove W10 and W52 from the A15 assembly and remove the A15 assembly.

2. To install a new assembly, reverse step 1.

NOTE: When tightening W10 and W52 to the A15 assembly, do not tighten so hard that W10 or W52 is stressed.

A16 High Band Modulator/Splitter Replacement Procedure

Refer to Figure H-25, view B for related assemblies, cables, and mounting hardware locations.

1. Disconnect the ribbon connector from A16A1.

2. Remove the A8W1 and A18A1W1 connectors from the A20 assembly.

3. Disconnect W5, W6, and W29 from the A16 assembly.

4. Remove the five A16 mounting screws (item 11).

5. Pull the A16 assembly out far enough to access cables W28 and W29. Remove these cables by gently and carefully prying them up with a small, flat tool.

6. the entire A16/A16A1 assembly is now free. Transfer the cable (W30) that interconnects A16 and A16A1 to the new A16/A16A1 assembly.

7. Remove the 5 countersunk screws that hold the A16 mounting plate to the A16 assembly, and attach the mounting plate to the new A16/A16A1 assembly.

8. To install the new assembly, reverse the above procedure (steps 1 through 5).

A17 Low Band Mixer Replacement Procedure

Refer to Figure H-25 for related assemblies, cables, and mounting hardware locations.

1. Remove the four screws on the A17 assembly (one on each corner).
2. Disconnect the three cables that go to the A17 low band mixer, and remove the assembly.
3. Install a new assembly by reversing the above procedure.

A18/A18A1 Low Band Power Amplifier Replacement Procedure

Refer to Figures H-25 and H-26 for related assemblies, cables, and mounting hardware locations.

1. Remove the two screws (item 12) that hold this assembly in place.
2. Remove the cables that go to the A18 assembly.
3. Take the assembly out of the instrument and remove the two countersunk screws that hold the A18 mounting plate to the assembly.
4. Attach the mounting plate to the new A18 assembly and install the assembly by reversing the above procedure.

A20 RF Section Filter Replacement Procedure

Refer to Figure H-25 for related assemblies, cables, and mounting hardware locations.

1. Remove all connectors from the assembly.
2. Remove the ribbon cable that goes to the A16A1 and A20 assemblies.
3. Remove the four screws holding the assembly (one in each corner).
4. Remove A8W1 and A18A1W1 and remove the A20 assembly.
5. Install the new assembly by reversing the above procedure.

NOTE: When reconnecting the ribbon cable to the A20 and A16A1 assemblies, ensure that the pins do not bend.

A63 RF Attenuator Replacement Procedure

1. Referring to the front panel — rear panel functional group, remove the front panel. You don't need to remove the ribbon cables.
2. Remove the two cables going to the A63 assembly.
3. Remove the two screws holding the A63 mounting bracket.
4. Remove the two screws holding the A63 assembly to the mounting bracket.
5. Install a new assembly by reversing the above procedure.

A64 Low Band Low Pass Filter

Refer to Figure H-25, view C, for related assemblies and cables.

1. Disconnect W17 from the A64 assembly.
2. Disconnect W15 from the A64 assembly and remove the A64 assembly.
3. To install a new assembly, reverse the procedure.

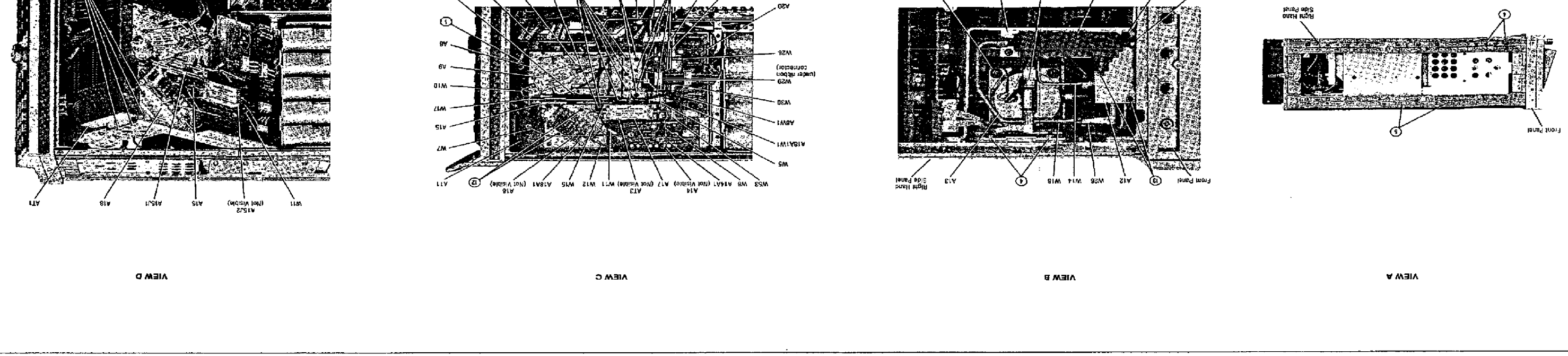


Figure H-25. RF Assemblies, Cables, Mounting Hardware Location

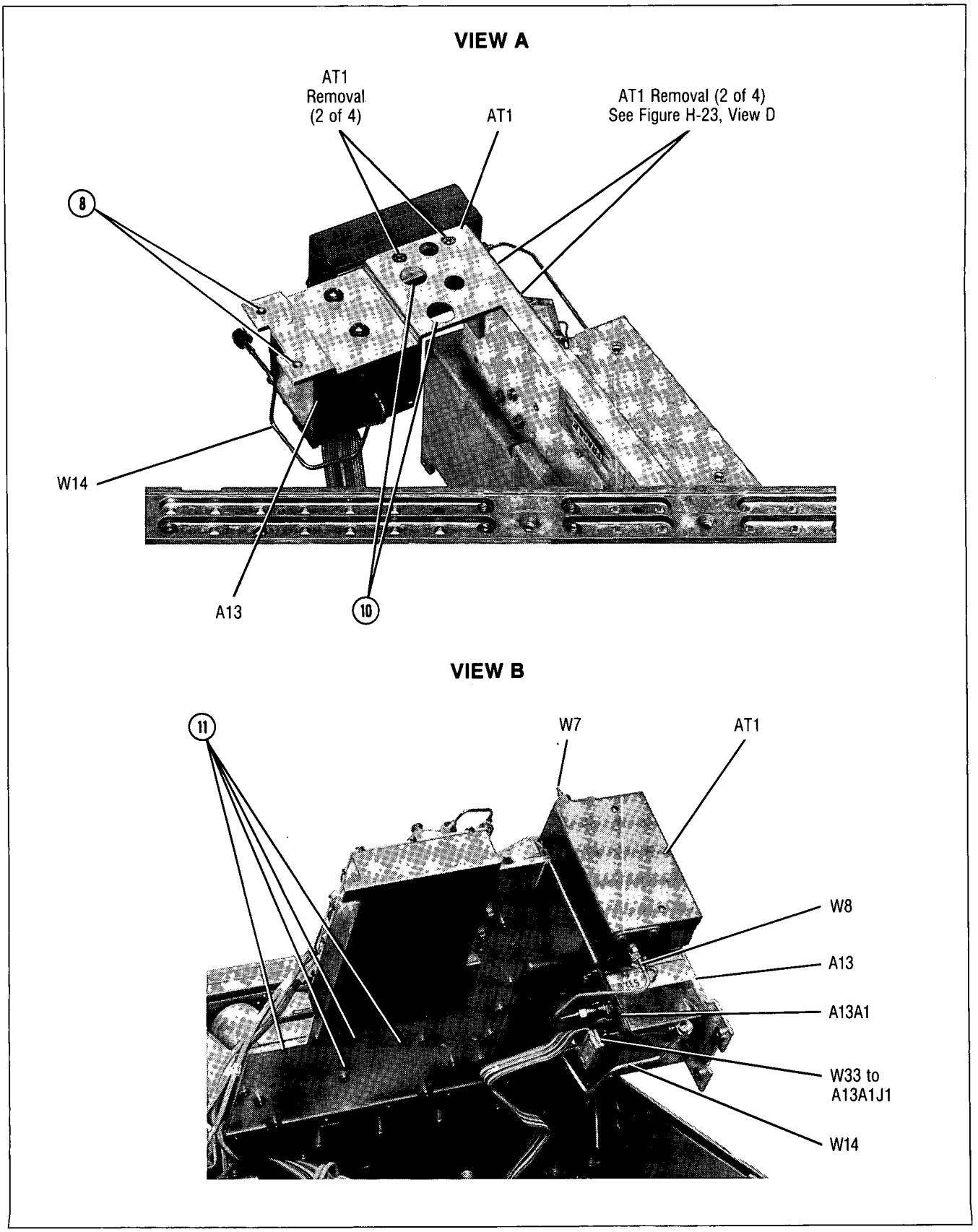


Figure H-26. A13, A13A1, A16, A18, and AT1 Assemblies, Cables, and Mounting Hardware Location

RF Section
Replaceable Parts

This section contains the RF section assembly-level replaceable parts. The microcircuits listed in Table H-1 are provided with a two-year warranty from the date of purchase and/or a restored exchange parts program.

The two-year warranty applies to both an original component and one that is purchased as a replacement, either new or restored, through the support life of the instrument. Using the restored exchange parts program, you can exchange a defective component for a factory-restored part, providing a substantial reduction in replacement cost over a new component.

If the original component is covered by a two-year warranty, the exchanged component also has a two-year warranty from the date of purchase.

Table H-1. Two-Year Warranty and Restored Exchange Parts

Reference Designation	Description	Two-Year Warranty	Restored Exchange Part
A8	3.7 GHz Oscillator	Yes	Yes
A9	Low Band Modulator	Yes	Yes
A12	Low Band Splitter/Detector	Yes	No
A13	Switched YTM	Yes	Yes
A14	High Band Power Amp	Yes	Yes
A16	High BandMod/Splitter	Yes	Yes
A17	Low Band Mixer	Yes	Yes
A18	Low Band Power Amp	Yes	Yes
A44	2.3 to 7.0 GHz YIG Oscillator (part number found in Sweep Generator – YO Loop Section)	Yes	Yes
A63	Attenuator	Yes	No

Table H-2. RF Section Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A8	5086-7309	3	1	3.7 GHZ OSCILLATOR	28480	5086-7309
	5086-6309	1	1	RESTORED EXCHANGE 3.7 GHZ OSCILLATOR	28480	5086-6309
A9	5086-7372	0	1	LOW BAND MODULATOR	28480	5086-7372
	5086-6372	8	1	RESTORED EXCHANGE LOW BAND MODULATOR	28480	5086-6372
A10	0955-0125	5	1	DIRECTIONAL COUPLER (8340)	28480	0955-0125
	0955-0148	2	1	DIRECTIONAL COUPLER (8341)	28480	0955-0148
A11	08340-60130	6	1	HIGH BAND DETECTOR	28480	08340-60130
A12	08340-60240	9	1	LOW BAND SPLITTER/DETECTOR	28480	08340-60240
A13	08340-60296	5	1	SWITCHED YIG-TUNED MULTIPLIER (8340)	28480	08340-60296
A14	~~08341-60027~~	1	1	HIGH BAND POWER AMPLIFIER (8340)	28480	~~08341-60027~~ 5086-7560
A15	9135-0191	6	1	LOW BAND LOW PASS FILTER	28480	9135-0191
A16	5086-7304	8	1	HIGH BAND MODULATOR/SPLITTER	28480	5086-7304
	5086-6304	6	1	RESTORED EXCHANGE HIGH BAND MOD/SPLITTER	28480	5086-6304
A17	5086-7374	2	1	LOW BAND MIXER	28480	5086-7374
	5086-6374	0	1	RESTORED EXCHANGE LOW BAND MIXER	28480	5086-6374
A18	5086-7217	0	1	LOW BAND POWER AMPLIFIER	28480	5086-7217
	5086-6217	8	1	RESTORED EXCHANGE LOW BAND POWER AMPLIFIER	28480	5086-6217
A20	08340-60203	4	1	RF SECTION FILTER	28480	08340-60203
A21	08340-60265	8	1	PULSE MODULATOR DRIVER	28480	08340-60265
A22	08340-60267	0	1	RF CLAMP/SRD BIAS ASSEMBLY	28480	08340-60267
A24	08340-60293	2	1	ATTENUATOR DRIVER	28480	08340-60293
A25	08340-60263	6	1	ALC DETECTOR	28480	08340-60263
A26	08340-60284	1	1	LINEAR MODULATOR	28480	08340-60284
A27	08340-60237	4	1	LEVEL CONTROL	28480	08340-60237
A28	08340-60256	6	1	SYTM DRIVER	28480	08340-60256
A47	08340-60094	1	1	SENSE RESISTER ASSEMBLY	28480	08340-60094
A63	08340-60175	9	1	90 DB PROGRAMMABLE RF ATTENUATOR	28480	08340-60175
A64	0955-0205	2	1	LOW BAND LOW PASS FILTER	28480	0955-0205
AT1	0960-0638	8	1	PERIPHERAL MODE ISOLATOR	28480	0960-0638
AT3	0960-0701	4	1	3.7 GHZ ISOLATOR	28480	0960-0701
W2	NONE	1		WIRE ASSY-RF MODULE(GND) TO FRONT PANEL		
W3	08340-20198	2	1	CABLE ASSY-RIGID COAX W51 TO A16J2	28480	08340-20198
W4	08340-20116	4	1	CABLE ASSY-RIGID COAX A16J1 TO J19	28480	08340-20116
W5	08340-20241	6	1	CABLE ASSY-RIGID COAX A17J2 TO A16J7	28480	08340-20241
W6	08340-20108	4	1	CABLE ASSY-RIGID COAX A16J6 TO A14J1	28480	08340-20108
W7	08340-20110	8	1	CABLE ASSY-RIGID COAX A14J1 TO AT1J1	28480	08340-20110
W8	08340-20111	9	1	CABLE ASSY-RIGID COAX AT1J2 TO A13J1	28480	08340-20111
W9	08340-20114	2	1	CABLE ASSY-RIGID COAX A8A2J1 TO A9J1	28480	08340-20114
W10	08340-20268	7	1	CABLE ASSY-RIGID COAX A9J2 TO A15J1	28480	08340-20268
W11	08340-60294	3	1	CABLE ASSY COAX A14J3 TO A62J21	28480	08340-60294
W12	08340-20107	3	1	CABLE ASSY-RIGID COAX A17J3 TO A18J1	28480	08340-20107
W13				NOT ASSIGNED		
W14	08340-20224	5	1	CABLE ASSY-RIGID COAX A12J2 TO A13J2	28480	08340-20224
W15	08340-20239	2	1	CABLE ASSY-RIGID COAX A18 TO A64	28480	08340-20239
W16	08340-20221	2	1	CABLE ASSY-RIGID COAX A13J3 TO A10J1	28480	08340-20221
W17	08340-20242	7	1	CABLE ASSY-RIGID COAX A64 TO A12	28480	08340-20242
W18	08340-20119	7	1	CABLE ASSY-RIGID COAX A10J3 TO A63J1(STD)	28480	08340-20119
W19	08340-20117	5	1	CABLE ASSY-RIGID COAX A63J2 TO J5 (STD)	28480	08340-20117
W20	08340-20122	2	1	CABLE ASSY-RIGID COAX A63J2 TO J20 (004)	28480	08340-20122

Table H-2. RF Section Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
W21	08340-20121	1	1	CABLE ASSY-RIGID COAX A10J3 TO J5 (001)	28480	08340-20121
W22	08340-20120	0	1	CABLE ASSY-RIGID COAX A10J3 TO J20 (005)	28480	08340-20120
W23	08340-60118	0	1	CABLE ASSY-COAX A30J3 TO A8A1J1	28480	08340-60118
W24	08340-60117	9	1	CABLE ASSY-COAX A62J14 TO A8A1J2	28480	08340-60117
W25	08340-60119	1	1	CABLE ASSY-COAX A62J10 TO A9J3	28480	08340-60119
W26	08340-60115	7	1	CABLE ASSY-COAX A12J3 TO A25J2	28480	08340-60115
W27	08340-60114	6	1	CABLE ASSY-COAX A11J2 TO A25J1	28480	08340-60114
W28	08340-60126	0	1	CABLE ASSY-COAX A62J13 TO A16J3	28480	08340-60126
W29	08340-60125	9	1	CABLE ASSY-COAX A62J25 TO A16J4	28480	08340-60125
W30	08340-60080	5	1	CABLE ASSY-COAX A16A1J2 TO A16J5	28480	08340-60080
W31	08340-60060	1	1	CABLE ASSY-RIBBON A62J19 TO A20J1/A16A1	28480	08340-60060
W32	08340-60058	7	1	CABLE ASSY-RIBBON A20J2 TO A14A1J1	28480	08340-60058
W33	08340-60061	2	1	CABLE ASSY-RIBBON A62J18 TO A13A1J1	28480	08340-60061
W52	08340-20233	6	1	CABLE ASSY-RIGID COAX A15J2 TO AT3J1	28480	08340-20233
W53	08340-20227	8	1	CABLE ASSY-RIGID COAX AT3J2 TO A17J1	28480	08340-20227

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
1	0520-0128	7	2	SCREW-MACH 2-56 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
2	0520-0136	7	4	SCREW-MACH 2-56 .625-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
3	2190-0003	8	20	WASHER-LK HLCL NO. 4 .115-IN-ID	28480	2190-0003
4	2190-0006	1	4	WASHER-LK HLCL NO. 6 .141-IN-ID	28480	2190-0006
5	2190-0045	8	6	WASHER-LK HLCL NO. 2 .088-IN-ID	28480	2190-0045
6	2200-0091	7	8	SCREW-MACH 4-40 .562-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
7	2200-0105	4	5	SCREW-MACH 4-40 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
8	2200-141	8	1	SCREW-MACH 4-40 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
9	2200-0143	0	7	SCREW-MACH 4-40 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
10	2200-0166	7	1	SCREW-MACH 4-40 .312-IN-LG 82 DEG	00000	ORDER BY DESCRIPTION
11	2260-0001	5	4	NUT-HEX-DBL-CHAM 4-40-THD .094IN-THK	28480	2260-0001
12	2360-0115	4	2	SCREW-MACH 6-32 .312-IN-LG-PAN-HD-POZI	00000	ORDER BY DESCRIPTION
13	2360-0207	5	8	SCREW-MACH 6-32 .875-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
14	2360-0334	9	6	SCREW-MACH 6-32 .312-IN-LG 100 DEG	28480	2360-0334
15	08340-00007	0	1	DECK-MICROCIRCUIT MOUNT	28480	08340-00007
16	08340-00045	6	1	BRACKET-PMI MOUNT	28480	08340-00045

Figure H-27. RF Section Attaching Hardware (1 of 2)

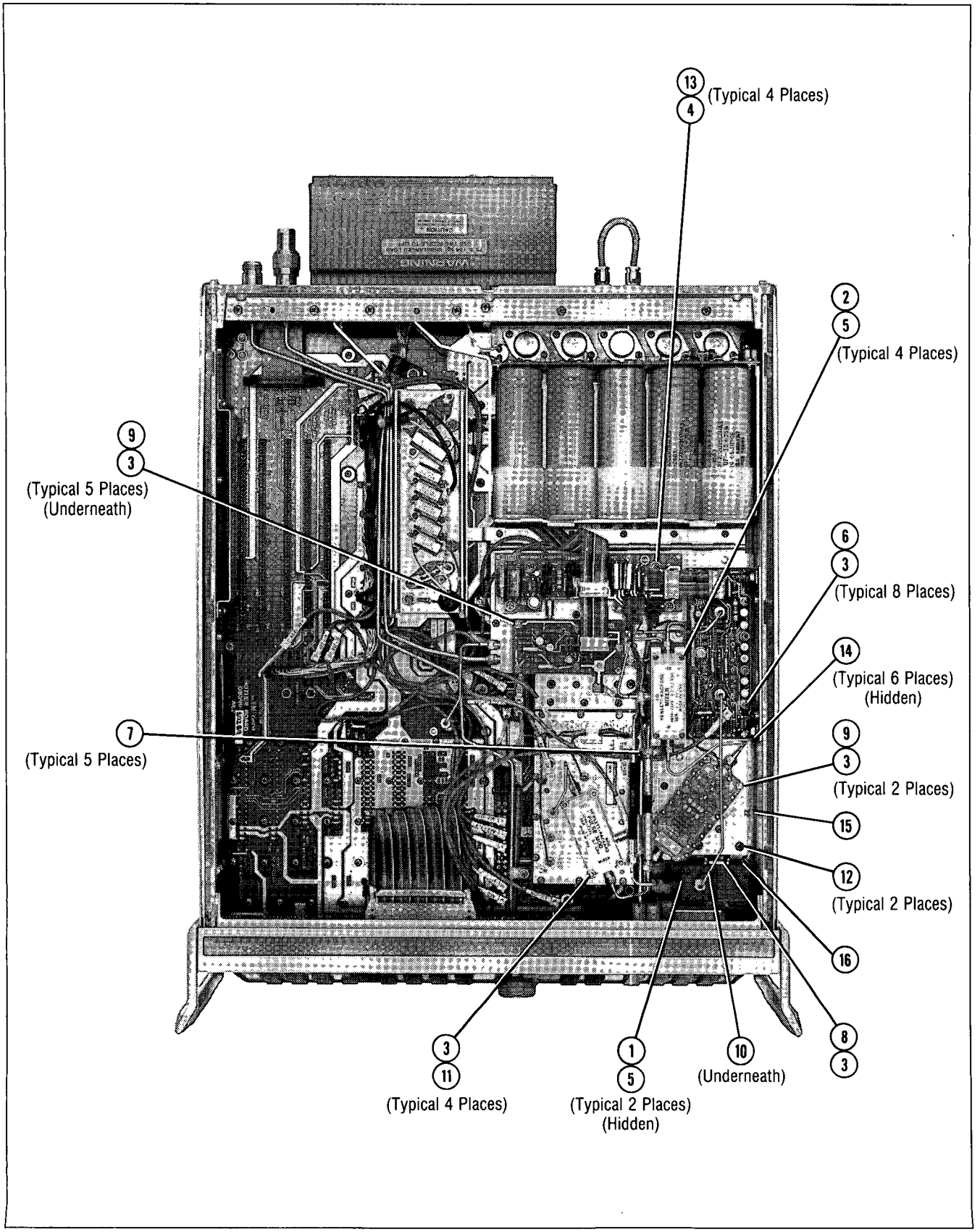


Figure H-27. RF Section Attaching Hardware (2 of 2)

Power Supplies – Fan

Power Supplies/Fan Assembly-Level Service

CONTENTS

Power Supplies/Fan Introduction

The power supplies produce the voltages required for the instrument and generate the power-up flag HPUP (high power up), which is used by the microprocessor and several other circuits to control instrument activity, and to ensure proper initialization.

ASSEMBLIES

The power supplies/fan functional group consists of five assemblies, and several components:

- A19 capacitor assembly
- A35 rectifier assembly
- A52 positive regulator assembly
- A53 negative regulator assembly
- A56 −15V regulator assembly
- A62 motherboard components
- FL1 power line module
- B1 fan assembly
- T1 transformer

Power Supplies/Fan Theory of Operation

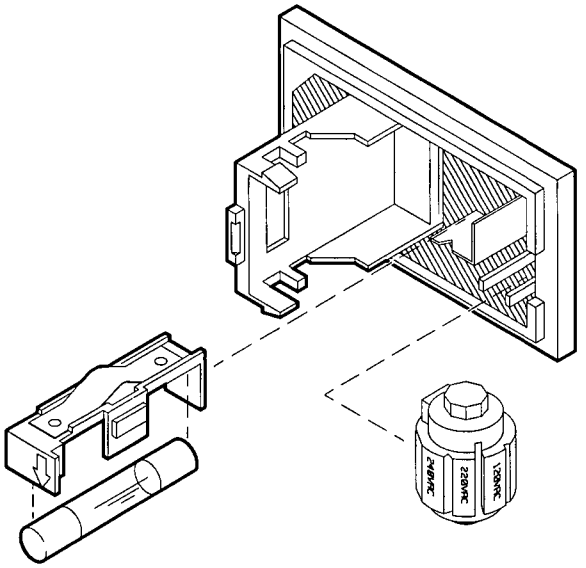
PRIMARY POWER

Primary power is supplied to the instrument transformer primary through the line filter module. The voltage selector cam position provides correct power connections to the transformer for line voltages of 100, 120, 220, or 240 Vac ±10%, at 47.5 to 66 Hz.

LINE MODULE

The line module performs several functions:

- The main line fuse protects the instrument from:
  Line voltage surges
  Incorrect line voltage
  Line module, transformer, motherboard, or rectifier assembly shorts.
- Line transient suppression.
- Line voltage configuration (see Figure I-1).



CAUTION:

Do not attempt to rotate the voltage selector cam while it is installed in the line module or non-repairable damage will result. The cam must be completely removed from the line module, rotated to the proper position, and reinstalled. Refer to the instructions below.

Replacement of fuse

1. Pry open line module cover door.
2. Pull out fuse carrier.
3. Insert fuse of proper rating.
4. Place carrier back into line module.

Selection of Operating Voltage

1. Pry open line module cover door.
2. **REMOVE CAM FROM THE LINE MODULE.**
3. Rotate the cam to the desired voltage. (When the line module cover is closed, the selected voltage will be visible through a small window.)
4. Insert the cam back into the line module.
5. Close the line module cover door.

Figure I-1. Power Line Module

A19 CAPACITOR ASSEMBLY

The A19 capacitor assembly contains the full-wave bridge rectifiers and line filters for the +20V and −10V power supplies. Also located on this assembly is a power-on safety indicator. When this indicator is illuminated, there are hazardous voltages present on the A62 motherboard.

A35 RECTIFIER ASSEMBLY

The A35 rectifier assembly consists of the following circuits:

- −40V Rectifier
- +22V Regulator
- +5V Rectifier
- Overvoltage Protection

A52 POSITIVE REGULATOR

The A52 positive regulator contains circuitry for the:

- +20V supply
- +12V supply
- +5.2V supply
- Voltage accuracy sensing circuitry
- ON/STANDBY and SHUTDOWN functions

The +20V supply is a self-starting regulator, with a precision reference to accurately set the output voltage. With the exception of the independent +22V standby supply (see the A35 assembly), all supplies are dependent on the +20V output.

NOTE: The +20 and +5.2V supplies are critical, low noise supplies with a specified periodic and random deviation (PARD) less than 100 μV peak. The +12V supply is non-critical, with a specified PARD less than 5 mV peak.

A53 NEGATIVE REGULATOR

The A53 assembly contains all circuitry for the −10V, −5.2V, and −40V power supplies, as well as voltage sensing circuitry to flag the A52 positive regulator assembly if one of these supplies goes out of tolerance.

NOTE: The −10 and −40V supplies are critical, low-noise supplies. They are limited to a periodic and random deviation (PARD) of less than 100 μV peak. The −5.2V supply is primarily a digital (ECL) supply, and has a PARD specification of 5mV.

A56 −15V REGULATOR

The A56 assembly contains the −15V regulator and voltage sense circuitry to flag the A52 positive regulator if an out-of-tolerance condition occurs in the supply.

POWER SUPPLIES

The 20V secondary is rectified and used by both the +20 and +22V regulators. The +22V supply is used for things that require power when the instrument is in standby (the 10 MHz standard oven, standby relay, and memory backup).

+20V is used to:

- Power the reference oscillator supply.
- Power the +12V supply.
- Provide a reference voltage for the +5.2, −10, and −40V supplies.

The −10V supply powers the −5.2V supply.

The −40V supply powers the −15V supply.

If the +20V supply fails, only the +22V supply will operate. The +20V supply is energized with a start-up current source until it reaches the voltage required to power the precision +10V reference. The +10V reference serves as a voltage reference for the +20V supply. If the instrument is turned off, or if the thermal switch temperature threshold is exceeded, the +20V supply shuts down.

The reference oscillator supply allows the 10 MHz reference oscillator to be turned off when an external 10 MHz reference is used

The 5V secondary output is rectified and regulated to generate the +5.2V regulated supply.

SUPPLY FAILURE MONITORING CIRCUITRY

HPUP (high power up) indicates whether all the instrument power supply voltages are operating. If a supply fails or is low, HPUP is low, and LIPS (low instrument preset) is low.

Pulling LIPS low causes the instrument microprocessor to reset, protects the instrument memory, resets the A3 display processor, and turns on all front panel LEDs. LIPS is also pulled low when you press **[INSTR PRESET]**.

STANDBY MODE

When line power is connected, and the front panel line switch is in the STANDBY position, the following happens:

- Power is supplied to the rectifiers on the A19 and A35 assemblies.
- The +22V regulator (on the A35 assembly) is powered by the +20V rectifier output (+20V UNREG).
- The cathode of DS1 (front panel standby LED) is grounded, lighting the LED.
- A62K1 switches (closes) into standby (fan remains off).
- LSBY (low standby) disables the +20V regulator.

WARNING

Although the +22V regulator is the only operational supply, line power is present, the rectifiers are fully operational, and the filter capacitors are fully charged.When the line switch is moved to on, the relay is disconnected from ground, providing power to the fan. Simultaneously, LSBY goes from 0 to 22V, allowing the +20V, and other supplies, to operate.

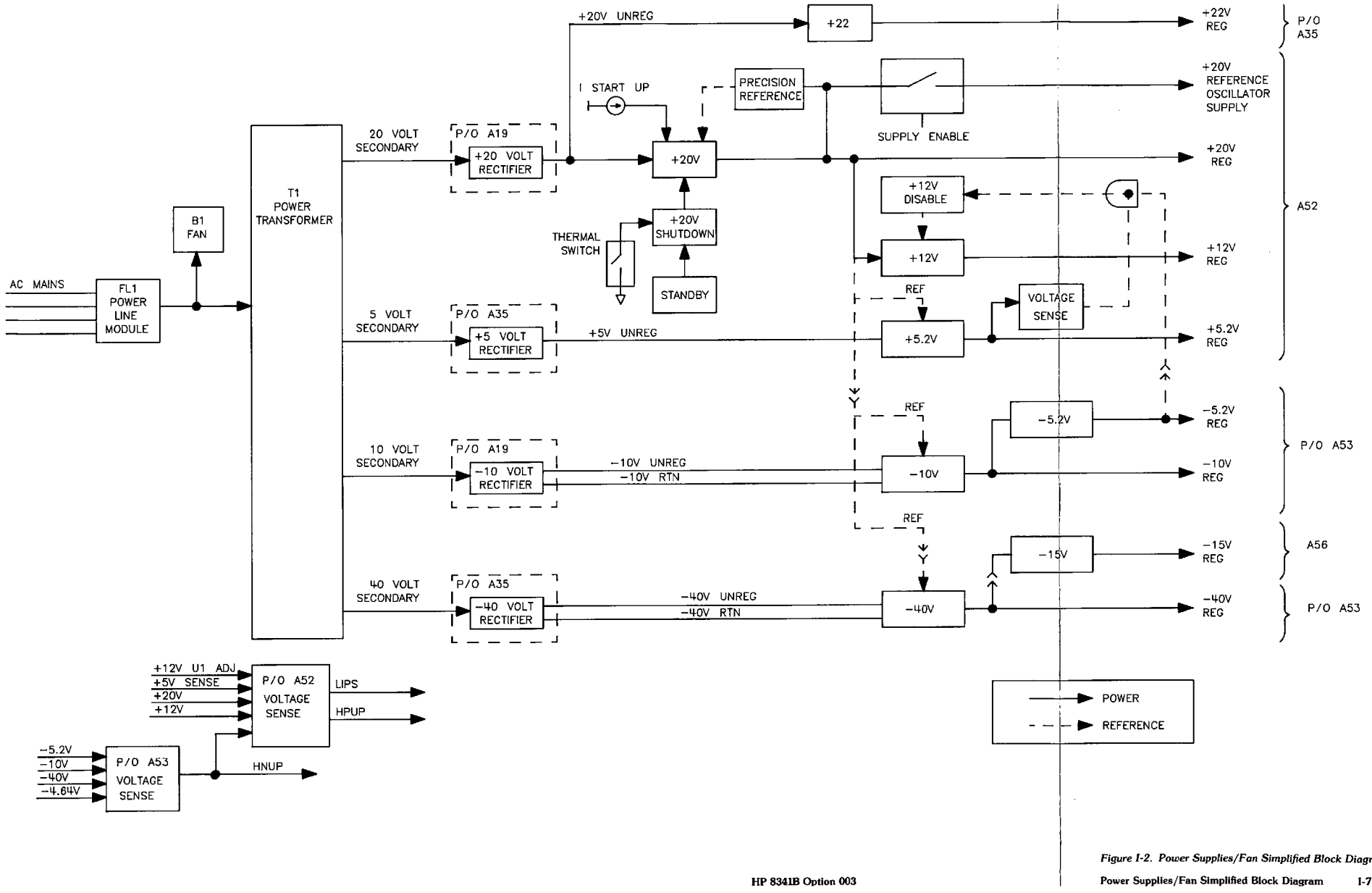


Figure I-2. Power Supplies/Fan Simplified Block Diagram

Power Supplies/Fan Assembly-Level Troubleshooting

WARNING

When the instrument is connected to ac line power and/or the A19 power-on safety indicator LED is on, there are voltages present inside the instrument that can cause personal injury or death. Only qualified personnel, who are aware of the hazards involved, should perform service on this instrument with its protective covers removed.

CAUTION

To avoid non-repairable damage to assemblies, do not reinstall the A19, A35, A52, or A53 assemblies unless ac mains is disconnected from the instrument.

To protect static sensitive components, troubleshoot these assemblies only at a work station equipped with an anti-static surface, and wear a grounding strap. When handling a printed circuit board, hold it by the edges; never touch the finger contacts.

INSTRUMENT BLOWS LINE FUSE

Initial Checks

1. Ensure that the line voltage selector cam is installed in the line filter module with the proper voltage selected.
2. Check that the proper value fuse is installed for the selected line voltage.

Regulator Checks

1. Remove line power and wait for the A19 power-on safety indicator to go out.
2. Remove the A52 regulator assembly.
3. Reconnect line power and turn on the instrument.
4. If the fuse blows, repeat the above procedure, removing, one at a time, the A53, A35, and A19 assemblies.
5. If the fuse blows with all these assemblies removed, suspect the A62 motherboard, or the transformer itself.
6. If the line fuse does not blow after you remove one of the assemblies, replace or troubleshoot that assembly.

LINE MODULE TROUBLESHOOTING

Refer to Figure I-6 in **REPAIR PROCEDURES**.

1. Ensure that the main line fuse and the selected line voltage are correct.
2. Disconnect line power, and remove the instrument top and bottom covers.
3. Wait for the A19 power-on safety indicator to go out.
4. Remove the portion of the rear panel that holds the line module:
   a. Remove two screws (item 12).
   b. Invert the instrument and remove three rear panel screws (item 7).
   c. Remove the A35 assembly protective cover.
   d. Remove three rear panel screws (item 13).
   e. Remove the fan.
   f. Remove three rear panel screws (item 8).
   g. From inside the instrument, push the rear panel out.
5. Reconnect line power.
6. If the line voltage selector cam is set to 120 or 240 Vac, measure the voltage across output pins C and E, and across pins D and F.

   If the line voltage selector cam is set to 100 or 220 Vac, measure the voltage across output pins A and F (see **LINE MODULE REPLACEMENT**).
7. The voltage across these pins should equal the selected line voltage. If no voltage is present, replace the line module.

RECTIFIERS AND REGULATORS

+22V is the only completely independent power supply, and no other power supply directly depends on it. When +22V comes on, LSBY (low standby) goes low, triggering the +20V supply.

The +20V supply does not directly require another supply to operate, but all other supplies (except +22V) are directly or indirectly dependent on it.

There are other power supply interrelationships as well:

- The +12V supply requires both the +5.2 and −5.2V supplies.
- The −5.2V supply is powered by the −10V supply.
- The −15V supply is powered by the −40V supply.

To determine the faulty rectifier or regulator when multiple supplies are down, or to determine if a single supply failure is caused by the rectifier or regulator, refer to Figure I-3.

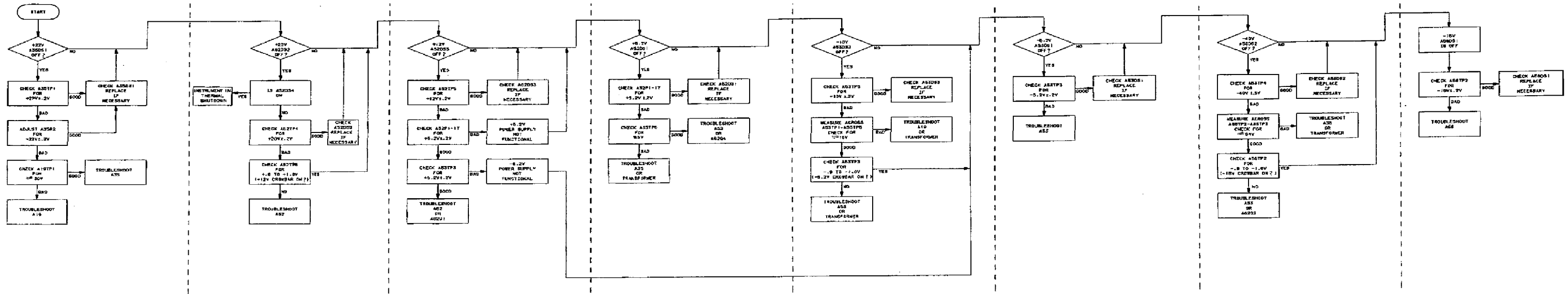


Figure 1-3. Power Supply — Troubleshooting to Assembly-Level Flow Chart

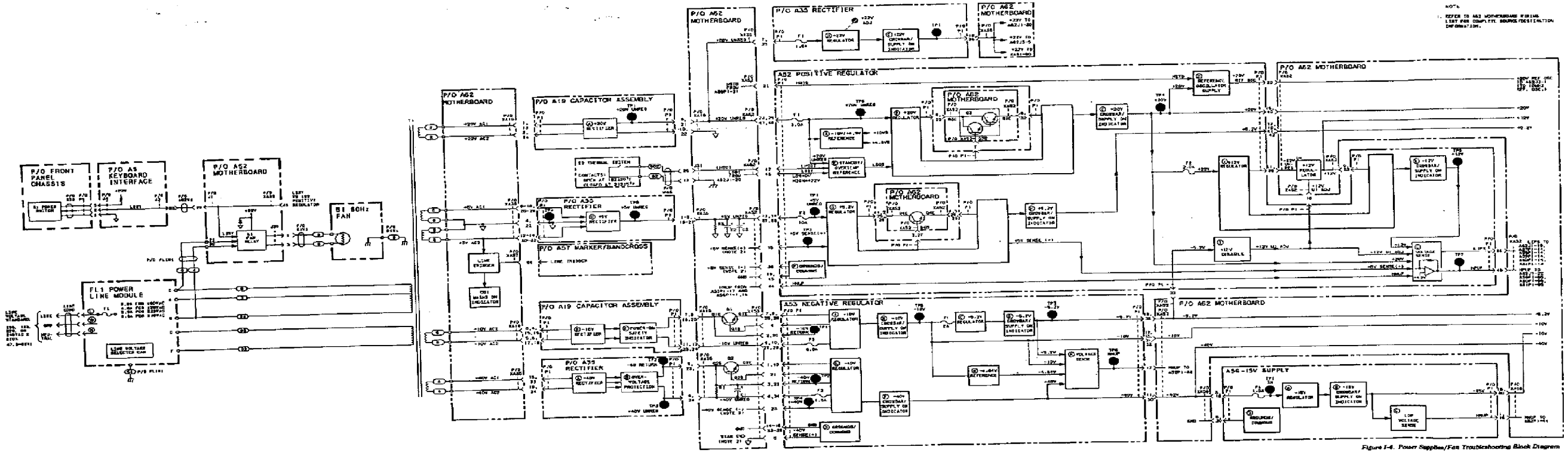


Figure 1-4. Power Supplies/Fan Troubleshooting Block Diagram

Table I-1. Power Supply Destination Chart

Assembly	Power Supply	Destination Assemblies/Connectors
A19	+20V UNREG	A35, A52
	−10V UNREG	A53
A35	−40V UNREG	A53
	+5V UNREG	A52, A3 (through A62J1), Rear Panel (through A62J31)
	+22V	A61, A3 (through A62J1), A51 (through A62J3)
A52	+20V	A21 through A28, A34, A36, A38, A40 through A43, A53 through A55, A57 through A61
	+5.2V	A21 through A28, A34, A36, A37, A39 through A43, A54, A55, A57 through A60, A50 (through A62J2), A16 and A20 (through A62J19)
	+12V	A23, A57 through A61, A3 (through A62J1)
A53	−10V	A21 through A28, A34, A36, A38 through A43, A54, A55, A57 through A61, A50 (through A62J2), A13 (through A62J18), A16 and A20 (through A62J19)
	−40V	A22, A23, A28, A34, A40, A54, A55, A56, A50 (through A62J2), A16 and A20 (through A62J19)
	−5.2V	A23, A27, A34, A52, A57 through A61, A3 (through A62J1), A50 (through A62J2), A16 and A20 (through A62J19)
A56	−15V	A27, A28, A54, A57 through A61

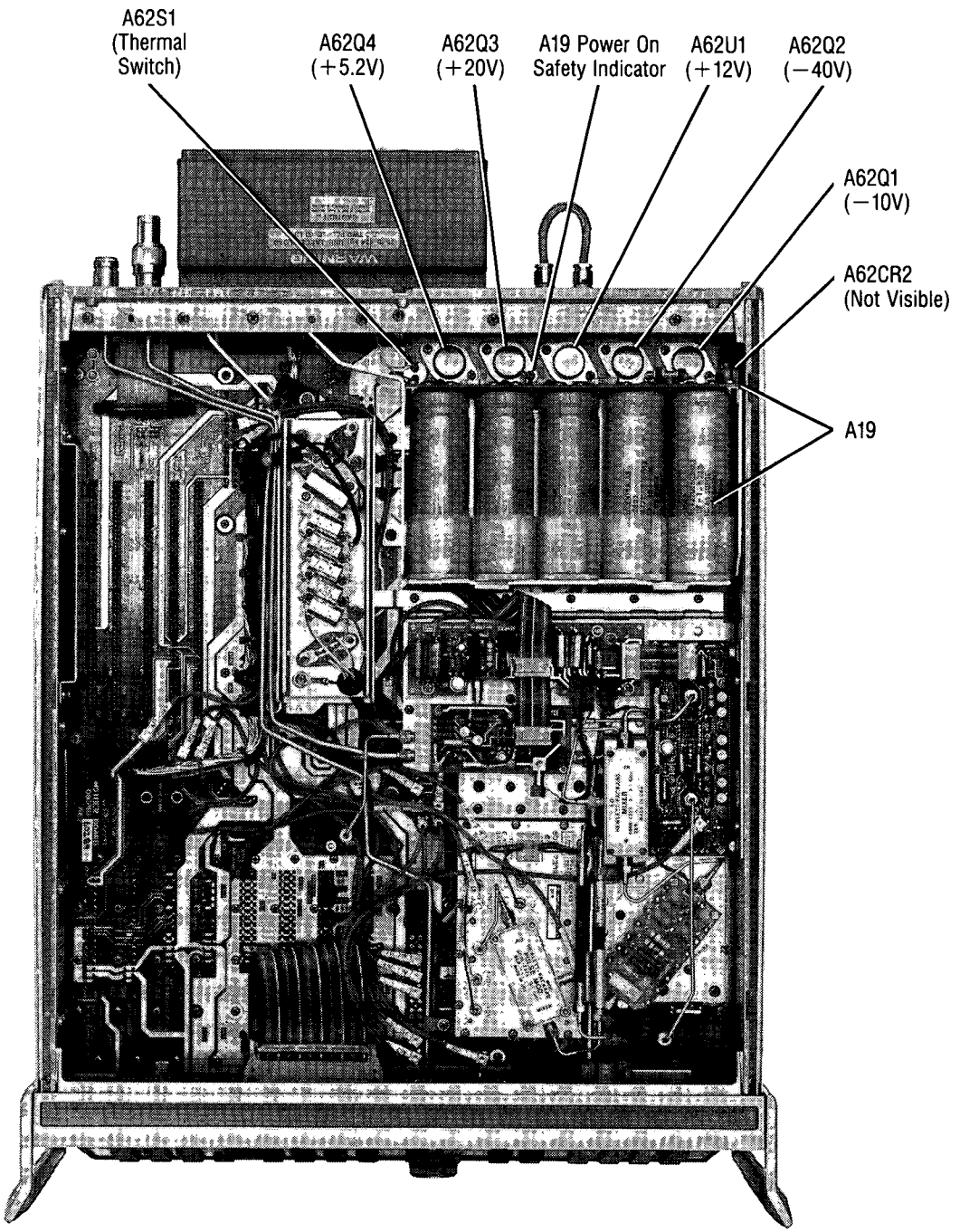


Figure I-5. Power Supplies/Fan Major Assemblies Location Diagram (1 of 2)

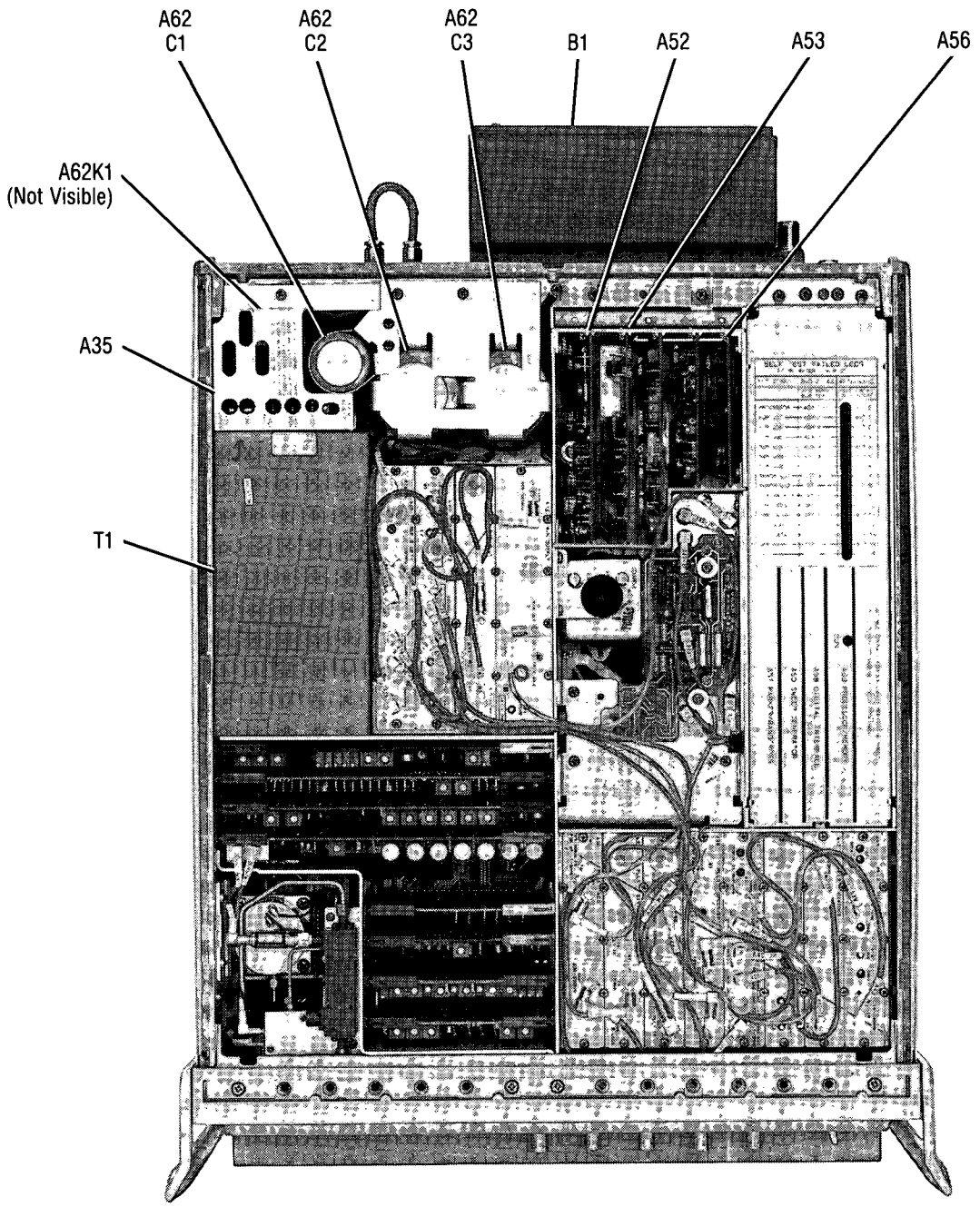


Figure I-5. Power Supplies/Fan Major Assemblies Location Diagram (2 of 2)

Power Supplies/Fan Repair Procedures

TRANSFORMER REPLACEMENT

Transformer Removal

Refer to Figure I-6.

1. Disconnect line power, and remove the instrument top and bottom covers.
2. Wait for the A19 power-on safety indicator to go out.
3. Remove the A19 capacitor assembly:
   a. Remove two flange screws (item 1).
   b. Remove two side panel screws (item 2).
4. Disconnect transformer wires from the A62 motherboard:
   a. Remove the seven screws (item 3) connecting the transformer secondary wires to the motherboard.
   b. Remove the wire clamp screw (item 4) from the side panel.
   c. Remove the two screws (item 5) holding the blue transformer secondary wires to the bottom of the motherboard.
5. Mechanically disconnect the rear panel assembly (item 6):
   a. Invert the instrument and remove three rear panel screws (item 7).
   b. Remove the A35 assembly protective cover.
   c. Remove three rear panel screws (item 8).
   d. From inside the instrument, push the rear panel out.
   e. Pull the rear panel out and away from the fan housing.
6. Desolder all transformer primary wires from the line module.
7. Remove the four 1/4 inch screws (item 9a), and the four 3/8 inch screws (item 9b), from the side panel.
8. Remove the last two screws as follows:
   a. Remove the cables from A25J1 and A25J2.
   b. Remove the A24, A25, A26, A27, and A28 assemblies.
   c. Using an offset posidriv, remove the two transformer screws on the side of the transformer enclosure closest to the front panel.
   d. Turn the instrument on its side and remove the transformer, carefully pulling one end out a short distance, and then the other.
   e. Remove the metal plate from the side of the transformer and place it on the new transformer.

Transformer Installation

1. Reverse the above procedure.

NOTES: When you reverse step 4a, do not allow the transformer secondary wires to touch adjacent A62 motherboard lugs.

Ensure that the white transformer secondary wire pair is reattached to the A62 motherboard lug labeled (9). DO NOT attach it to the taller, unmarked lug.

When reversing step 4a, ensure the blue transformer secondary wires are completely inside the plastic clamp. If the plastic clamp hardware is mounted in the wrong side panel hole, the A19 assembly will not go back in place.

Reinstall the A19 capacitor assembly as follows:

1. Lift the two grey cables out of the way.
2. Lower the A19 assembly flange-end first until the finger contact end drops in place.
3. Lift up slightly on the flange-end, and push down on the finger connector side until the fingers are fully seated.

LINE MODULE REPLACEMENT

Read the entire procedure before you start!

Line Module Removal

Refer to Figure I-6.

1. Ensure that the main line fuse and the selected line voltage are correct.
2. Disconnect line power, and remove the instrument top and bottom covers.
3. Wait for the A19 power-on safety indicator to go out.
4. Remove the portion of the rear panel that holds the line module:
   a. Remove two screws (item 12).
   b. Invert the instrument and remove three rear panel screws (item 7).
   c. Remove the A35 assembly protective cover.
   d. Remove three rear panel screws (item 13).
   e. Remove the fan.
   f. Remove three rear panel screws (item 8).
   g. From inside the instrument, push the rear panel out.
5. Desolder all wires from the line module.

6. The line module is held in by four plastic retainers and two metal clips. The metal clips are NOT part of the line module and must be removed before the line module can be removed:

   a. To release the metal clips, using wire cutters, cut the plastic retainers away at the base, flush with the body of the line module, well away from the tops of the metal clips. The metal clips do not come off if any plastic remains.

   b. With a flat head screwdriver, pry the metal clips away from the line module; lay them down as far as possible.

   c. Remove and discard the metal clips; remove the line module.

Line Module Installation

1. Select and install the proper fuse in the fuse holder.

2. Set the line voltage selection cam to the proper line voltage.

NOTE: The cam does not turn. To change the line voltage selection, remove the cam from the power line module and replace it in the proper position.

3. Place the metal retainers (HP part number 02932-00038) on the line module. the portion of the clip that is bent 90° (at each end of the clip) should fit under the plastic retainers on the line module.

4. When you insert the line module in the rear panel, ensure the line cord receptacle is on the side farthest from the instrument fan.

5. Push the line module in firmly until all clips engage on the inside of the rear panel.

6. Wire the new line module as shown in Figure I-4. Reinstall the rear panel by reversing step 4 of the line module removal procedure.

FAN REPLACEMENT

Fan Removal

Refer to Figures I-5a and I-6.

1. Disconnect line power, and remove the instrument top and bottom covers.

2. Wait for the A19 power-on safety indicator (red LED) to go out. This indicator is visible from the top of the instrument with the cover removed.

3. Remove the A35 assembly protective cover (item 10), the A35 assembly, and the nearby capacitor cover (item 11, in two pieces).

4. Disconnect the fan cable from J30 (located on the motherboard assembly.

5. Remove two screws (item 12) from the rear panel frame (top).

6. Remove three screws (item 13) from the rear panel frame (bottom). Note the location of the ground lug and of the small metal grounding plate.

7. Remove the four screws (item 13a) located on the rear panel. The fan assembly can now be separated from the instrument frame.

8. Remove four screws from each side of the fan housing. These screws must be discarded and replaced with new screws (HP part number 2200-0055).
9. Remove four screws holding the fan filter assembly to the front of the fan.
10. Remove two screws on the front of the fan housing. These screws must be discarded and replaced with new screws (HP part number 2200-0055).
11. Separate the fan housing.

NOTE: Carefully note the position of the two washers between the fan and the base plate. These must be placed properly when the fan is reassembled, or the fan can be permantly warped.

12. Remove the two screws holding the fan base plate.

Fan Installation

1. Reverse the above procedure.

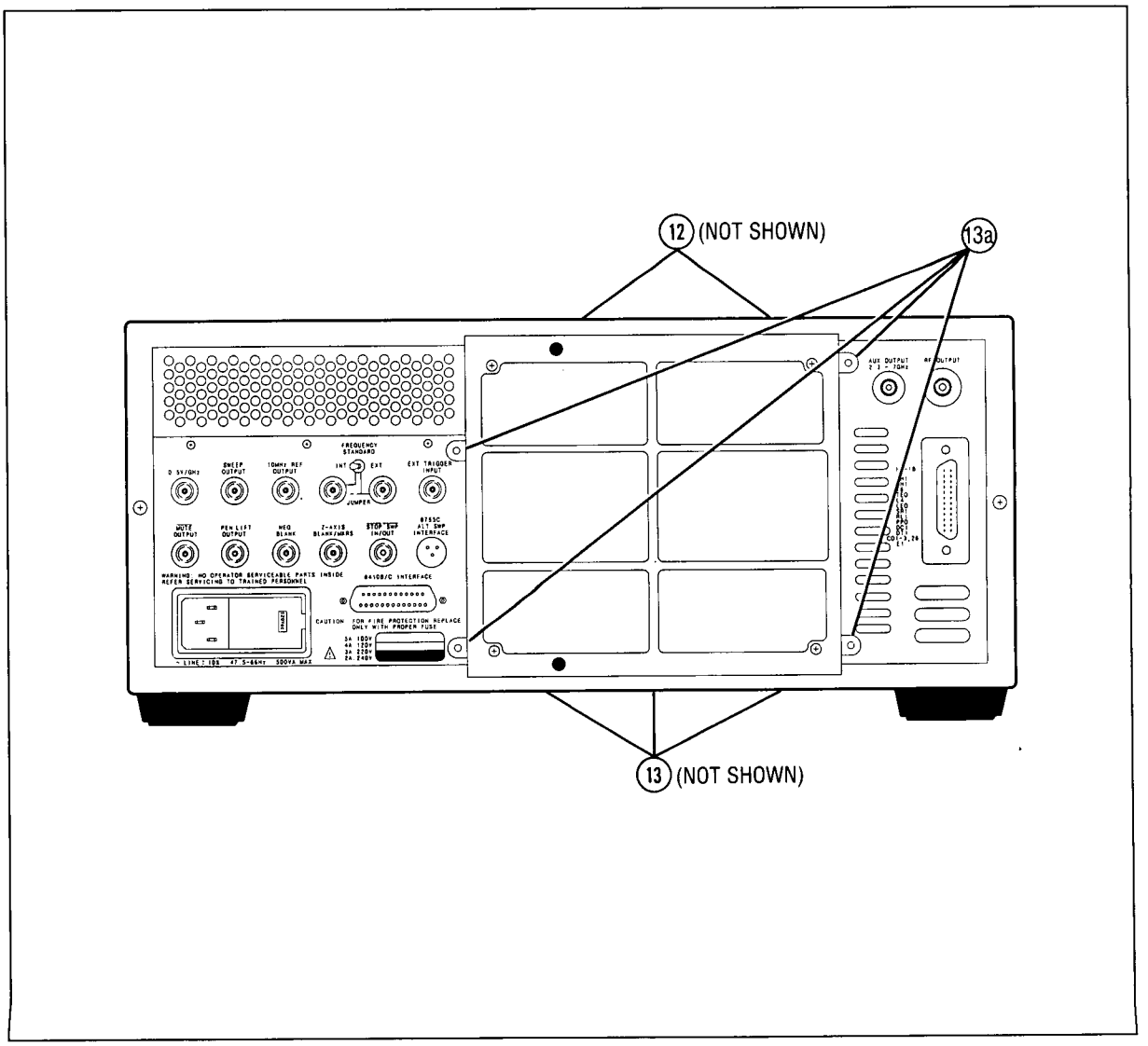
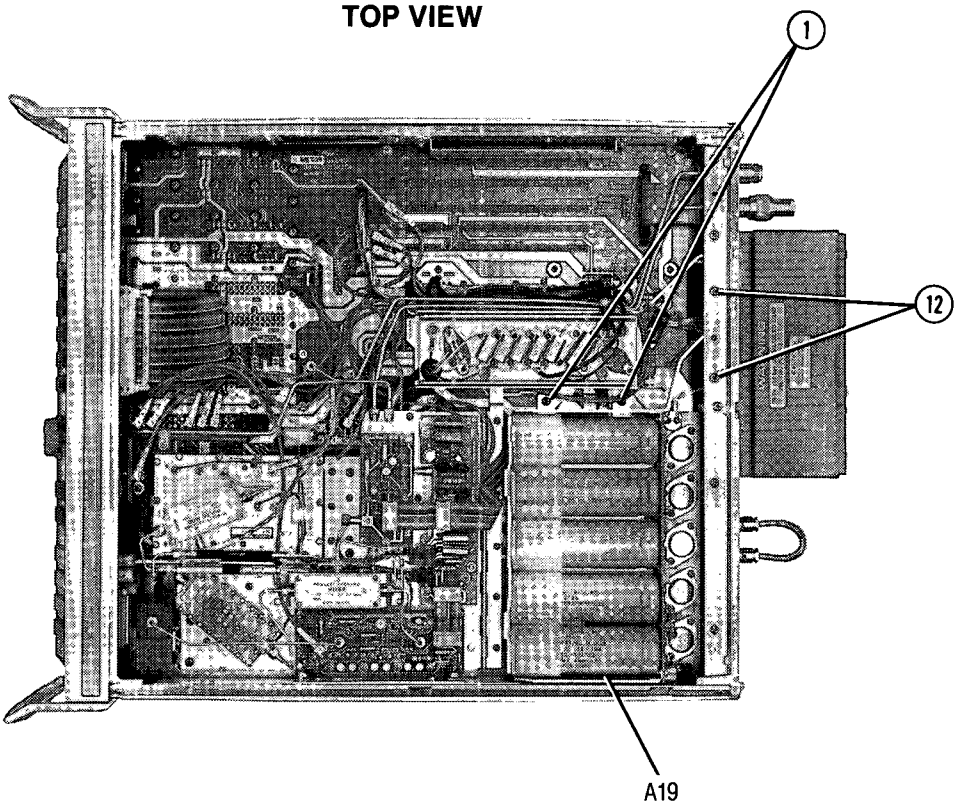


Figure I-5a. Mechanical Parts Attaching the Fan Assembly to the Rear Panel



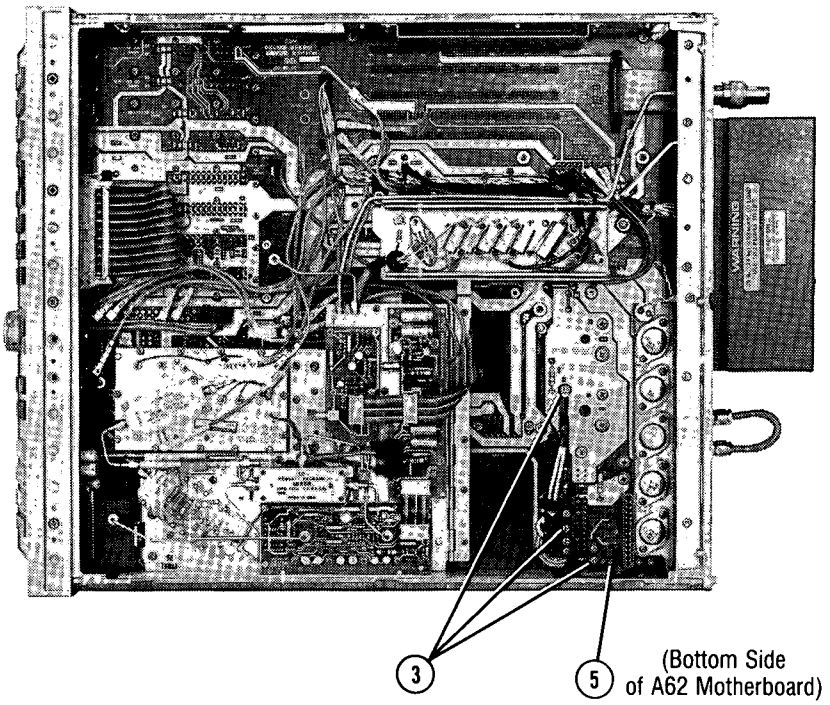


Figure I-6. Transformer/Line Module/Fan Replacement (1 of 2)

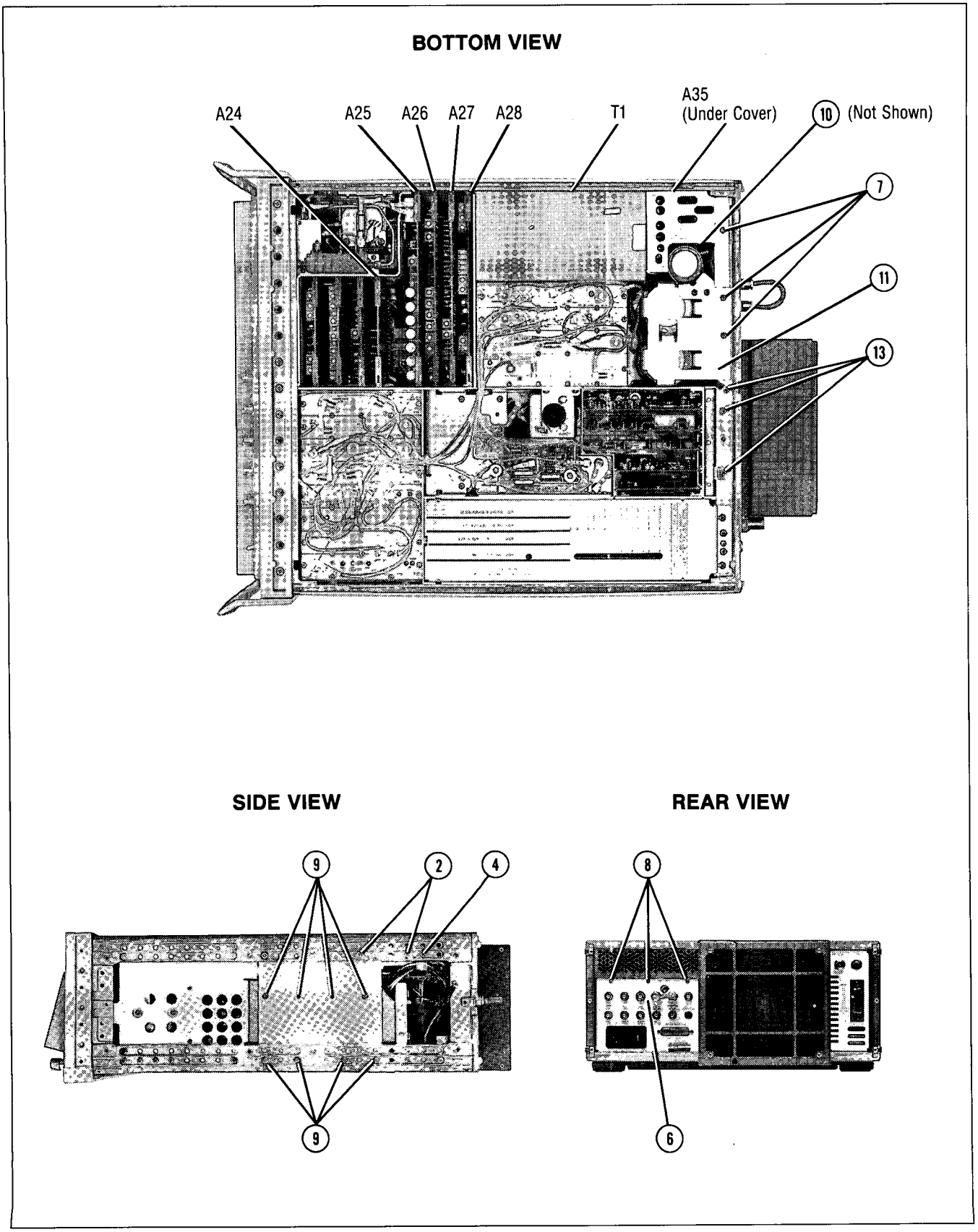


Figure I-6. Transformer/Line Module/Fan Replacement (2 of 2)

Power Supplies/Fan Replaceable Parts

This section lists power supplies/fan assembly-level replaceable parts.

Table I-2. Power Supplies/Fan Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A19	**08340-60258**	**9**	**1**	**A19 CAPACITOR ASSEMBLY**	**284800**	**8340-60258**
A35	**08340-60259**	**0**	**1**	**A35 RECTIFIER ASSEMBLY**	**28480**	**08340-60259**
A52	**08340-60179**	**3**	**1**	**A52 POSITIVE REGULATOR ASSEMBLY**	**28480**	**08340-60179**
A53	**08340-60160**	**4**	**1**	**A53 NEGATIVE REGULATOR ASSEMBLY**	**28480**	**08340-60160**
A56	**08340-60029**	**2**	**1**	**A56 −15V REGULATOR ASSEMBLY**	**28480**	**08340-60029**
A62C1	0180-3205	5	1	CAPACITOR-FXD 4200UF +75-10% 75VAC AL	28480	0180-3205
A62C2	0180-3017	7	2	CAPACITOR-FXD .045F +75-10% 25VAC AL	28480	0180-3017
A62C3	0180-3017	7		CAPACITOR-FXD .045F +75-10% 25VAC AL	28480	0180-3017
A62CR2	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A62K1	0490-0618	5	1	RELAY 2C 24VDC-COIL 5A 115VAC	28480	0490-0618
A62Q1	1854-0618	8	2	TRANSISTOR NPN SI DARL TO-3 PD=150W	04713	MJ3000
A62Q2	1854-0294	6	1	TRANSISTOR NPN SI TO-3 PD=150W FT=500KHZ	28480	1854-0294
A62Q3	1854-0618	8	1	TRANSISTOR NPN SI DARL TO-3 PD=150W	04713	
A62Q4	1854-0679	1	1	TRANSISTOR NPN 2N5885 SI TO-3 PD=200W	04713	2N5885
A62S1	3103-0108	2	1	THERMAL SWITCH	28480	3103-0108
A62U1	1826-0423	4	1	IC V RGL TR TO-3	27014	LM317K
B1	08340-60291	0	1	FAN ASSEMBLY Includes B1W1 and the following parts:	28480	08340-60291
	0360-0535	0	2	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
	0890-0029	0	1	TUBING-HS .187-D/.093-RCVD .02-WALL	28480	0890-0029
	0890-0983	5		TUBING-HS .125-D/.062-RCVD .02-WALL	28480	0890-0983
	1251-4223	1	2	CONNECTOR- CONT F .025	28480	1251-4223
	1251-6796	7	1	CONNECTOR HOUSING- 3 FEMALE IR	28480	1251-6796
	1400-0249	0	1	CABLE TIE .062-.625-DIA .091-WD NYL	06383	PLT1M-8
	1520-0230	3	4	SHOCK MOUNT .27-EFF-HGT 2-LB-LOAD-CAP	28480	1520-0230
	2190-0017	4	2	WASHER-LK HLCL NO. 8 .168-IN-ID	28480	2190-0017
	2200-0770	9	10	SCREW-MACH 4-40 .188-IN-LG 100 DEG	00000	ORDER BY DESCRIPTION
	2360-0119	8	4	SCREW-MACH 6-32 .438-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
	2360-0196	1	4	SCREW-MACH 6-32 .375-IN-LG 100 DEG	00000	ORDER BY DESCRIPTION
	2510-0135	7	2	SCREW-MACH 8-32 2.25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
	2680-0137	8	1	SCREW-MACH 10-32 .188-IN-LG PAN-HD-SLT	00000	ORDER BY DESCRIPTION
	3160-0371	1	1	FAN-TBAX 180-CFM 115V 50/60-HZ	28480	3160-0371
	8150-0011	0	1	WIRE 22AWG G 300V PVC 7X30 105C	28480	8150-0011
	8150-0447	6	1	WIRE 24AWG BK 300V PVC 7X32 80C	28480	8150-0447
	08340-00012	7	1	HOUSING FAN (TOP)	28480	08340-00012
	08340-00013	8	1	HOUSING FAN (BOTTOM)	28480	08340-00013
	08340-00097	8	1	HOUSING FAN (GRILLE)	28480	08340-00097
	08340-00016	1	1	BASE PLATE	28480	08340-00016
	08340-00017	2	1	GRILL AIR FILTER	28480	08340-00017
	08340-00018	3	1	FILTER-AIR	28480	08340-00018
	85660-20092	4	4	SNUBBER-SHOCK MOUNT	28480	85660-20092
F1	2110-0002	9	1	FUSE 2A 250V NTD 1.25X.25 UL (For 240V operation)	75915	312002
F1	2110-0003	0	1	FUSE 3A 250V NTD 1.25X.25 UL (For 200V operation)	75915	312003
F1	2110-0010	9	1	FUSE 5A 250V NTD 1.25X.25 UL (For 100V operation)	75915	312005
F1	2110-0055	2	1	FUSE 4A 250V NTD 1.25X.25 UL (For 120V operation)	75915	312004
FL1	08340-60257	8	1	LINE MODULE-FILTERED REPLACEMENT KIT (Includes 2 metal retainers)	28480	08340-60257
T1	9100-4133	1	1	TRANSFORMER	28480	9100-4133
	08340-60124	8		COMPLETE TRANSFORMER ASSEMBLY (Includes wiring harness and attached lugs) Individual transformer wire solder lugscan be ordered below:	28480	08340-60124
	0360-0037	7	6	TERMINAL-SLDR LUG PL-MTG FOR-#6-SCR	28480	0360-0037
	0360-0042	4	2	TERMINAL-SLDR LUG PL-MTG FOR-#6-SCR	28480	0360-0042
	0360-0043	5	1	TERMINAL-SLDR LUG PL-MTG FOR-#6-SCR	28480	0360-0043

Major Assemblies and Components Location – Chassis Parts Assembly-Level Service

CONTENTS

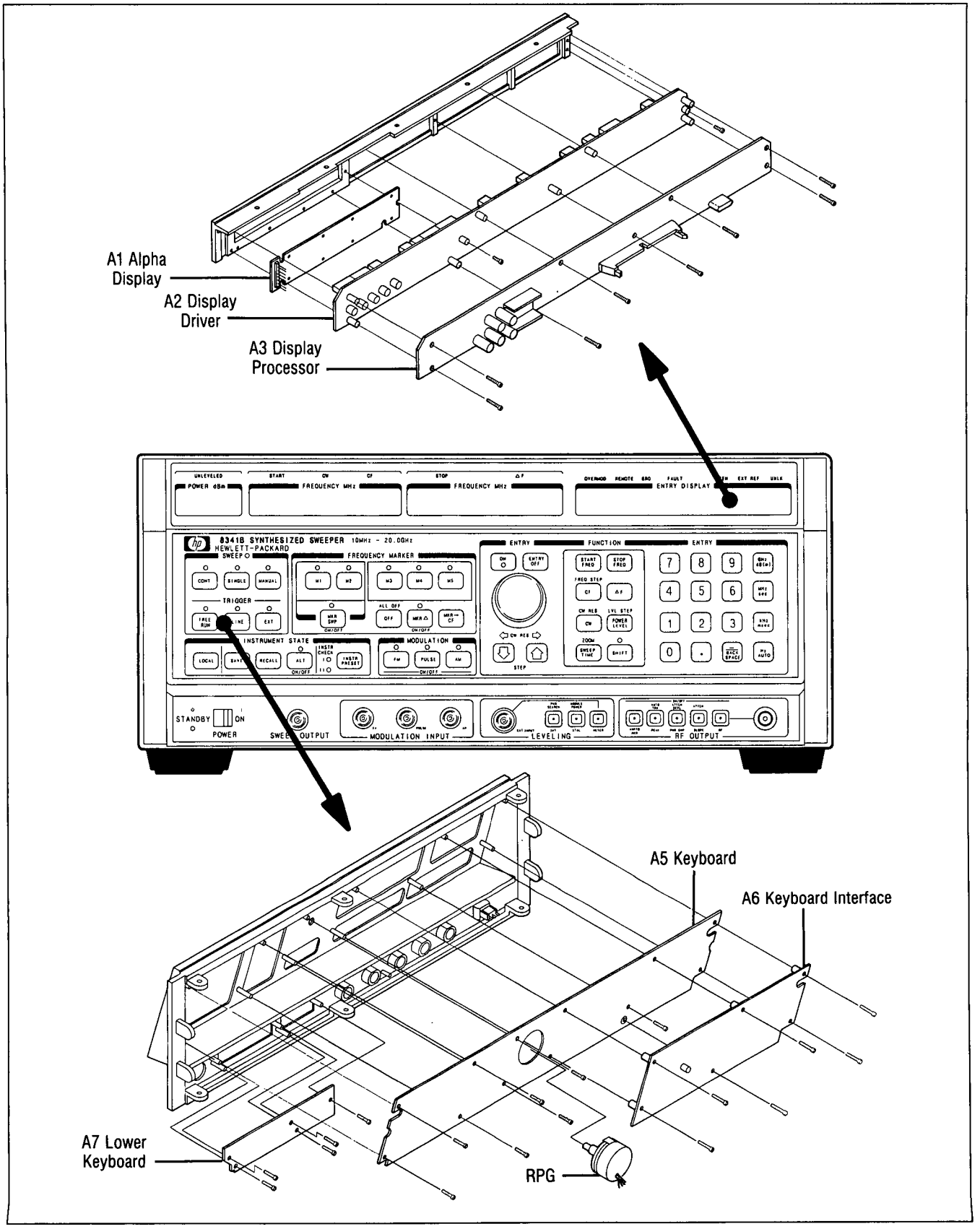


Figure J-1. Front Panel Assemblies

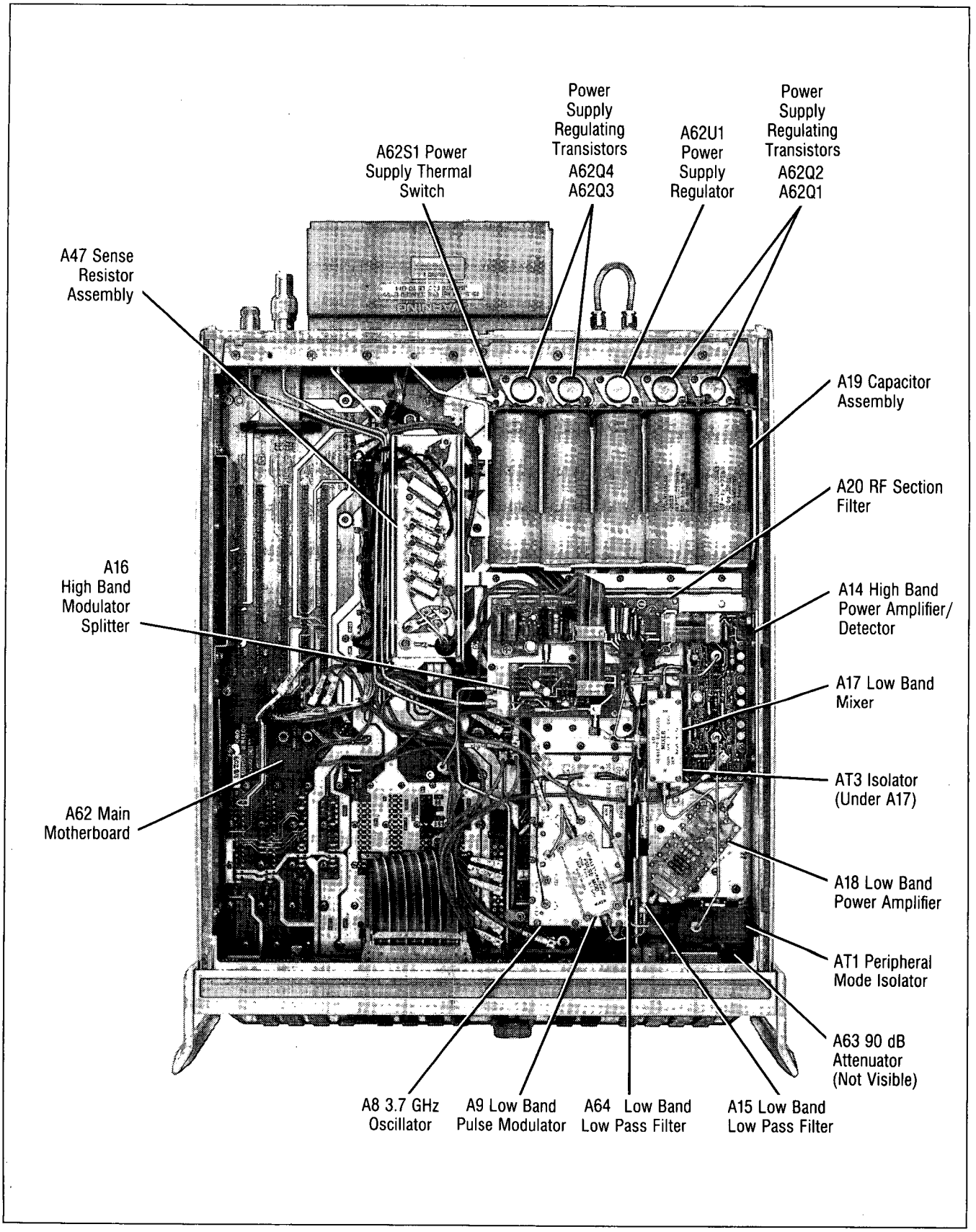


Figure J-2. Top View

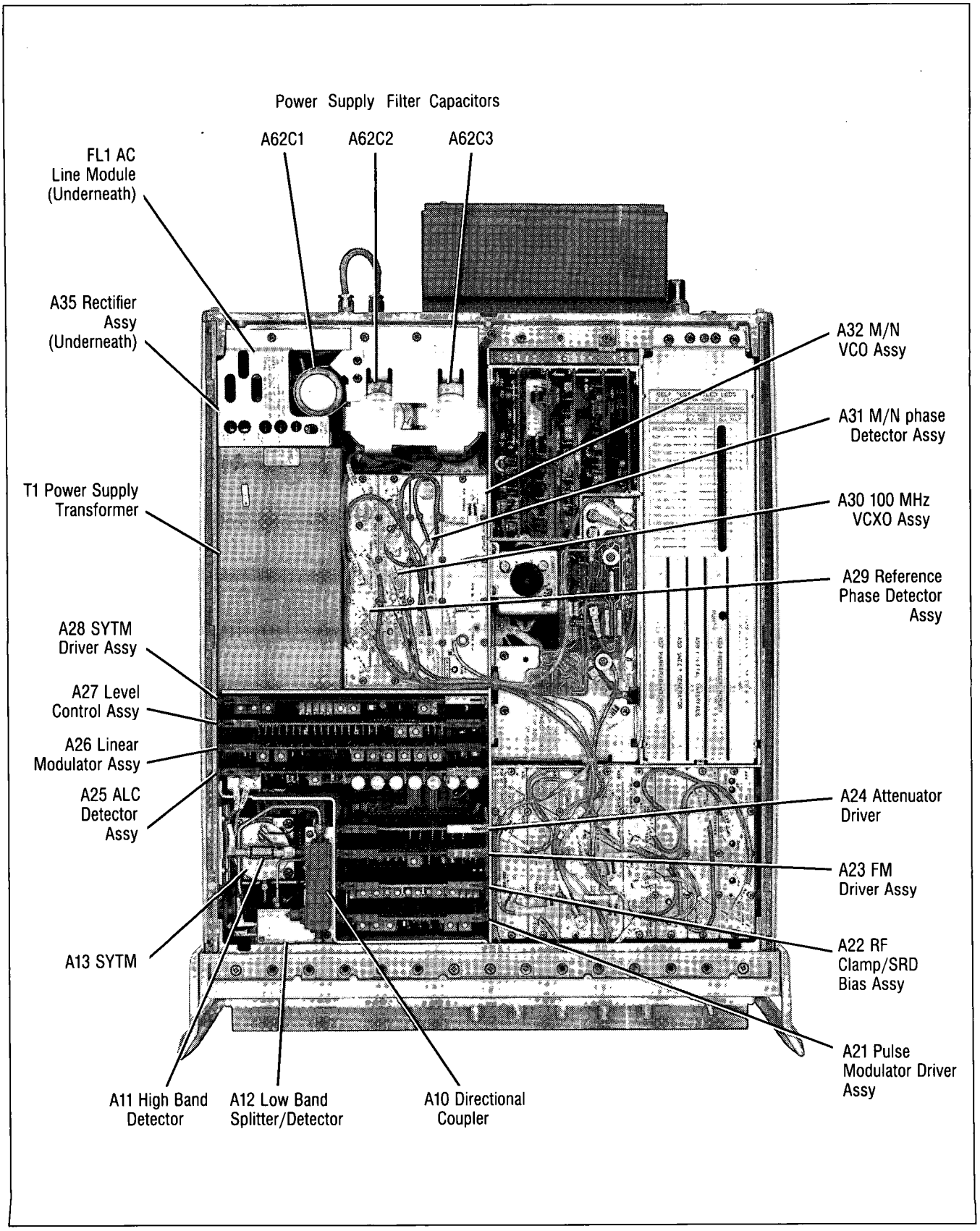


Figure J-3. Bottom View (1 of 2)

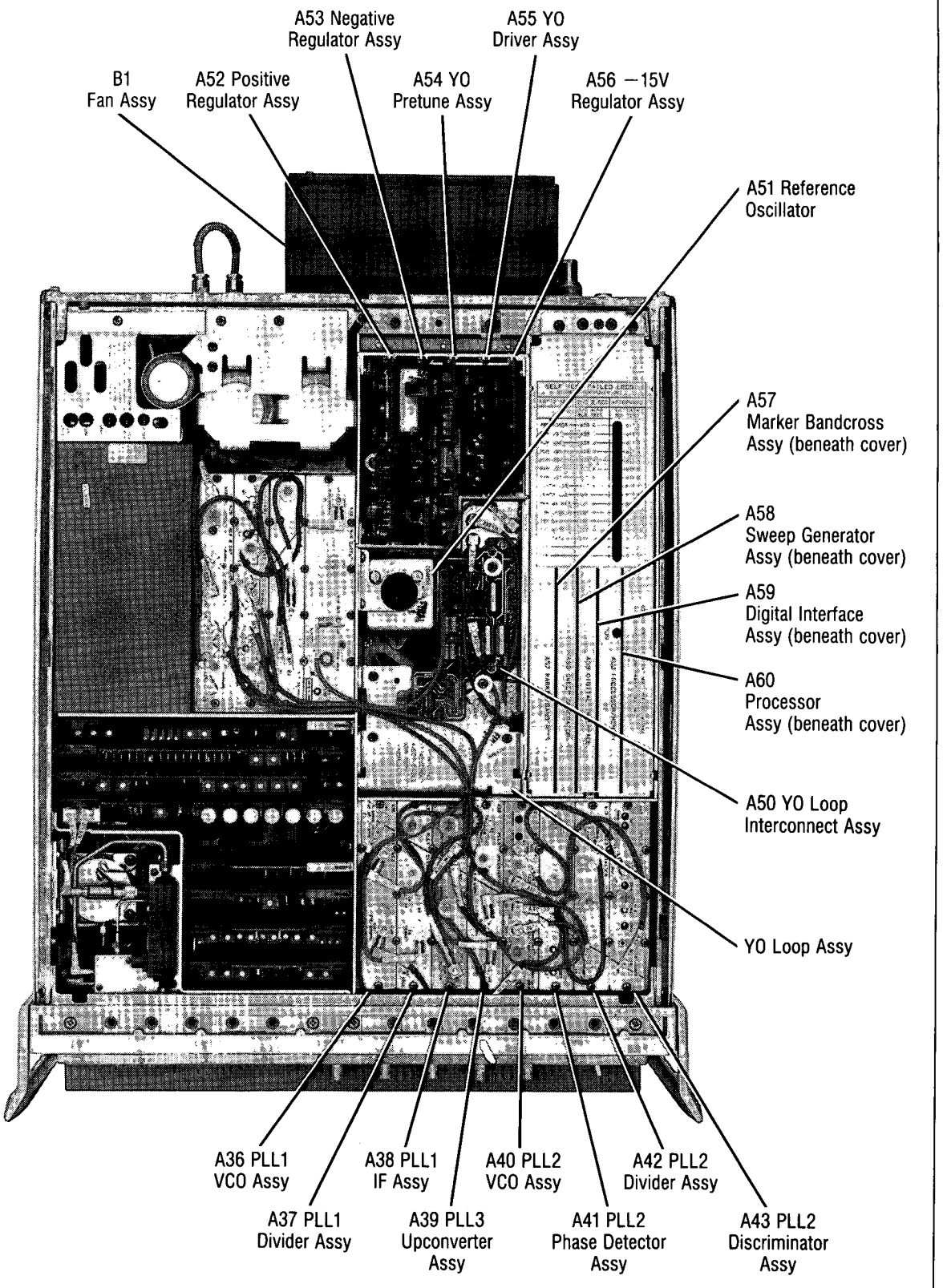


Figure J-3. Bottom View (2 of 2)

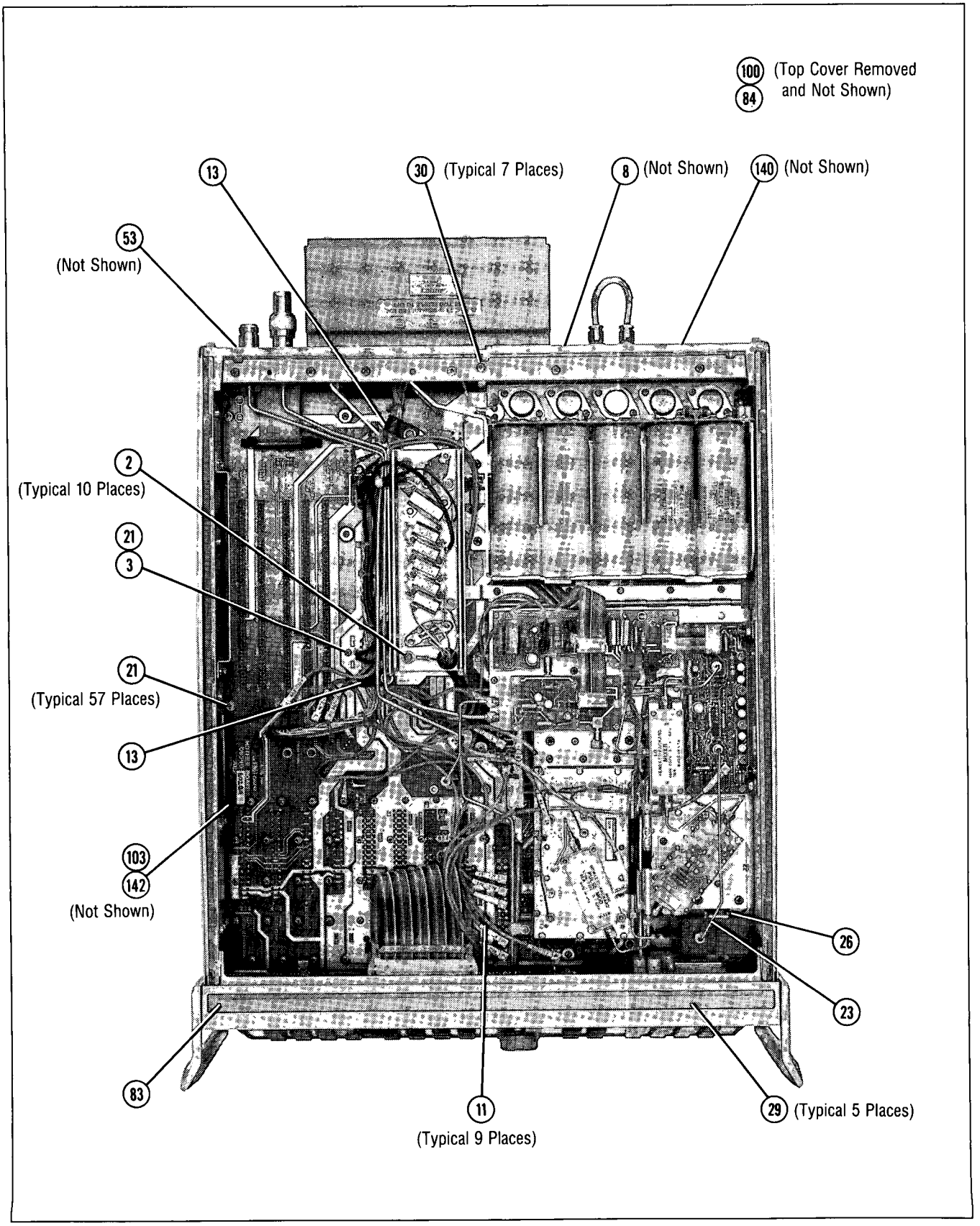


Figure J-4. Miscellaneous Mechanical & Chassis Parts (1 of 5)

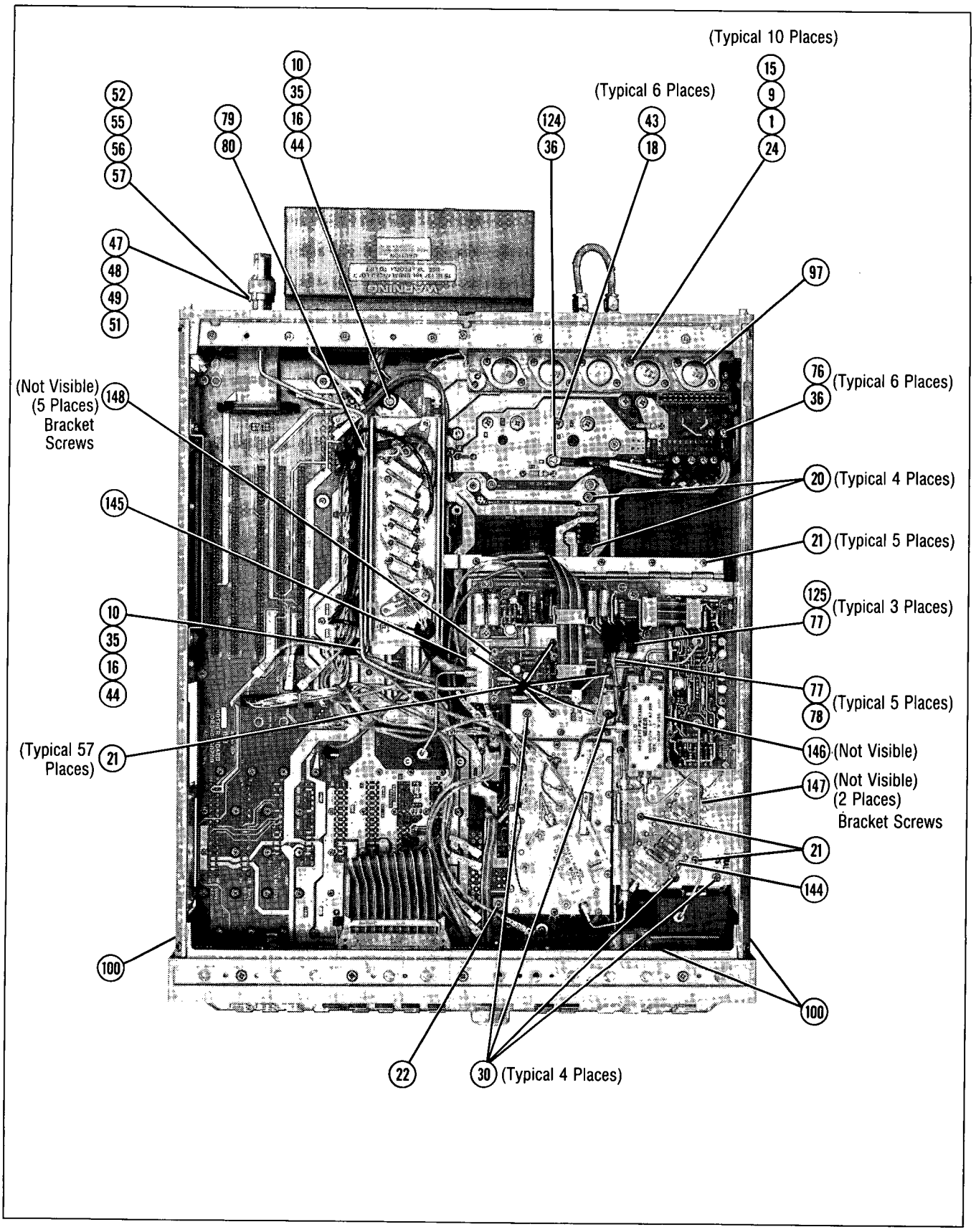


Figure J-4. Miscellaneous Mechanical & Chassis Parts (2 of 5)

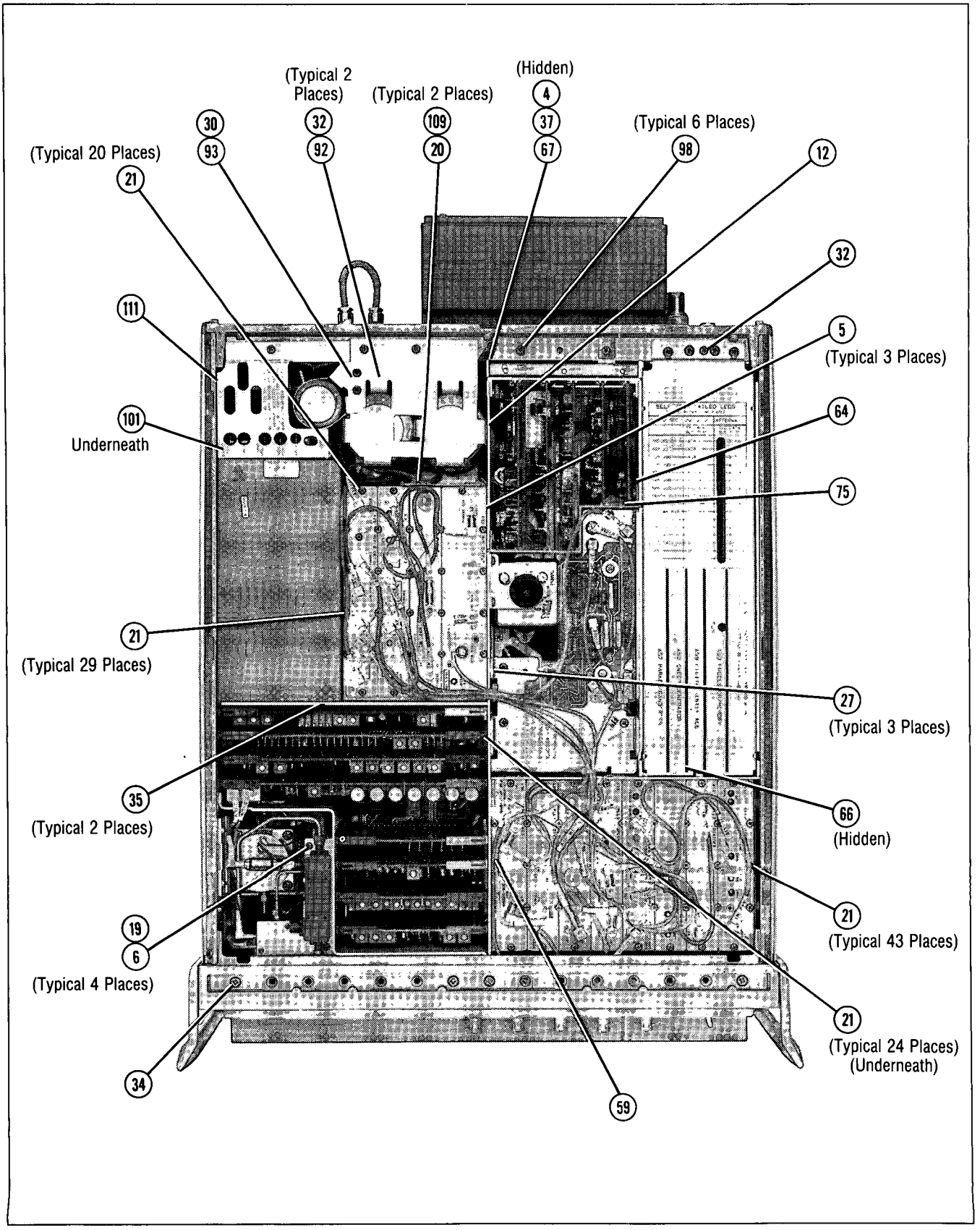


Figure J-4. Miscellaneous Mechanical & Chassis Parts (3 of 5)

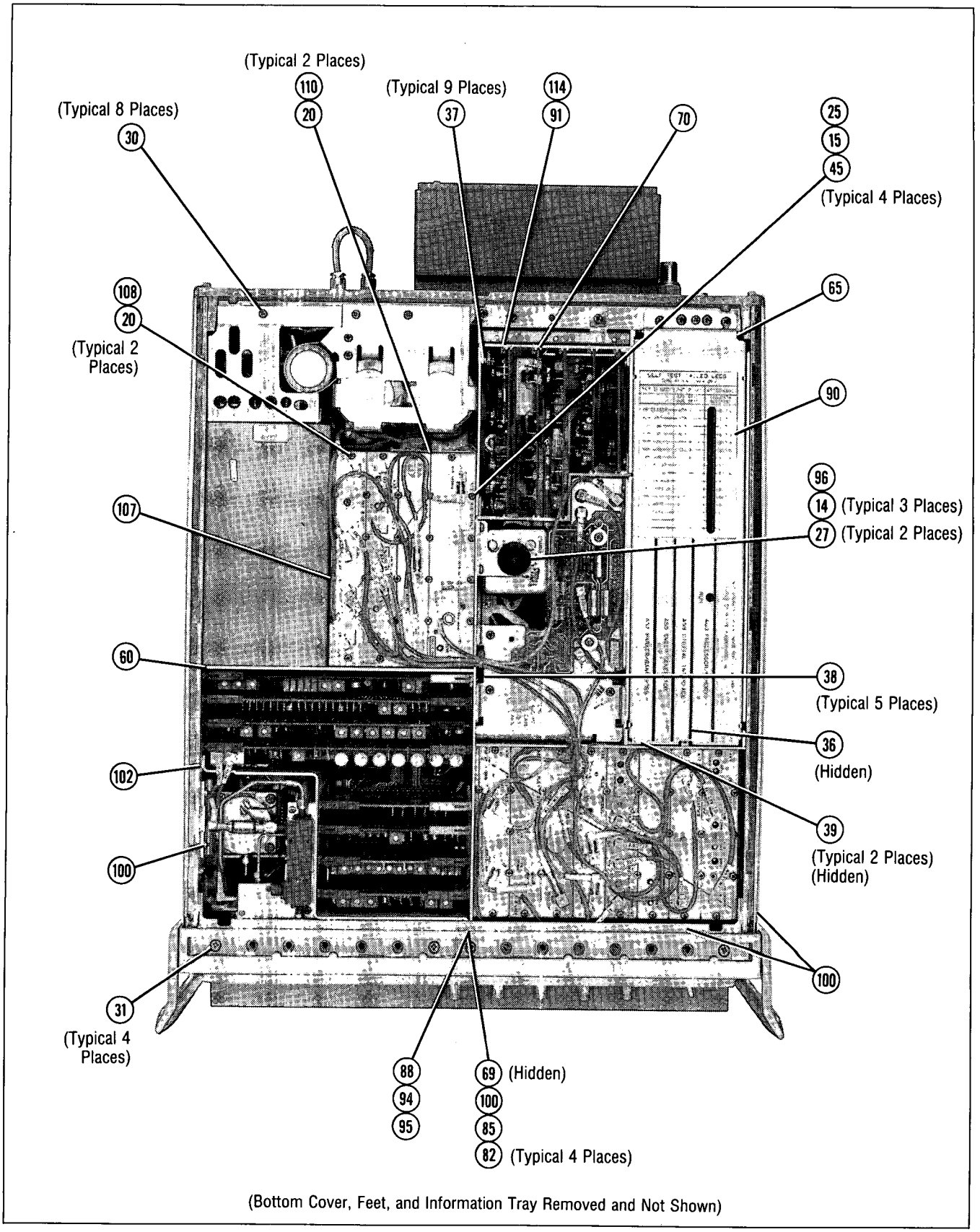


Figure J-4. Miscellaneous Mechanical & Chassis Parts (4 of 5)

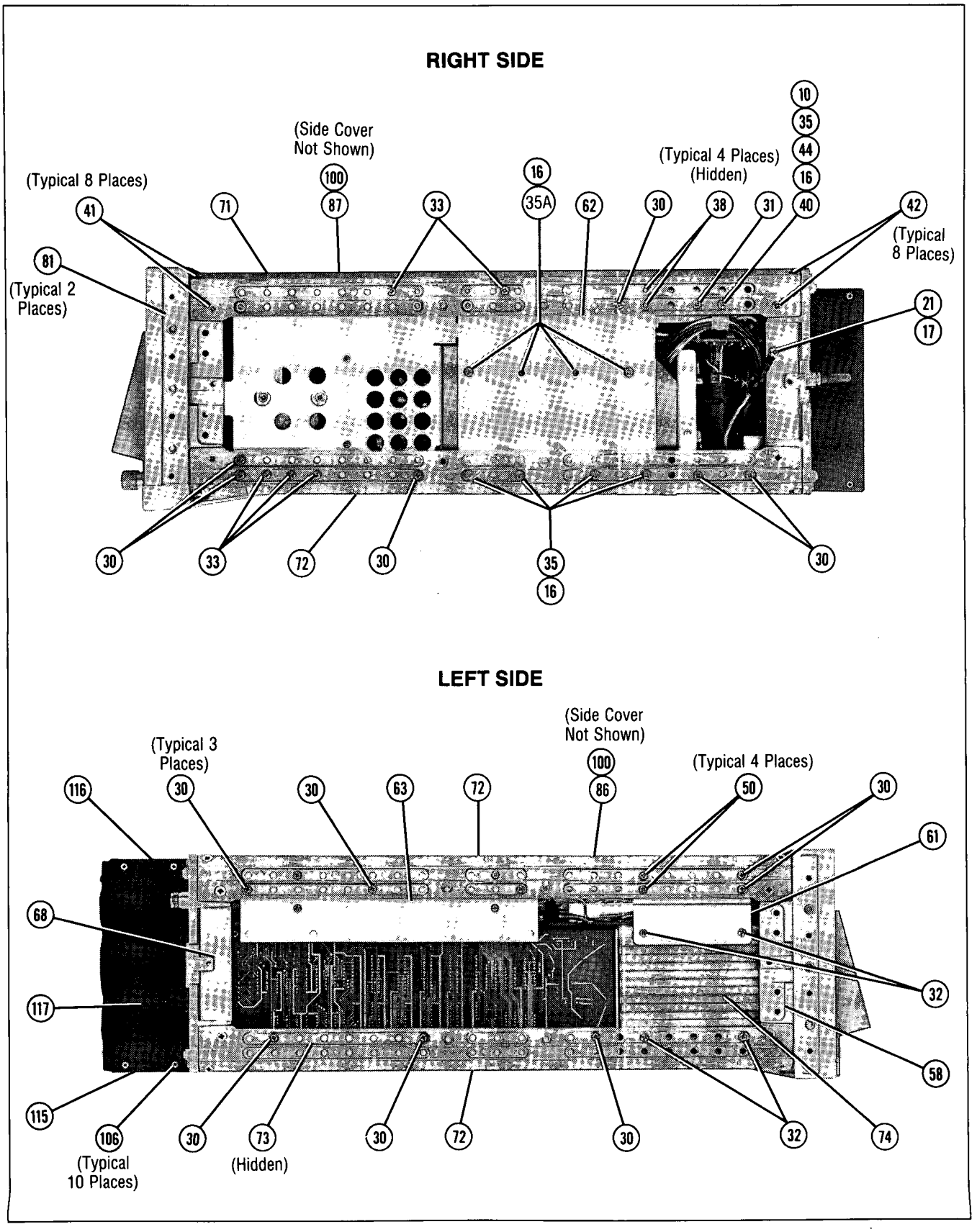


Figure J-4. Miscellaneous Mechanical & Chassis Parts (5 of 5)

Table J-1. Replaceable Miscellaneous & Mechanical Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
				MISCELLANEOUS MECHANICAL & CHASSIS PARTS		
1	0340-0923	8	10	INSULATOR-BSHG NYLON	28480	0340-0923
2	0360-0037	7	10	TERMINAL-SLDR LUG PL-MTG FOR-#6-SCR	28480	0360-0037
3	0360-0042	4	3	TERMINAL-SLDR LUG PL-MTG FOR-#6-SCR	28480	0360-0042
4	0400-0082	8	2	GROMMET-CHAN NCH .09-IN-GRV-WD	28480	0400-0082
5	0400-0219	3	3	GROMMET-RND .5-IN-ID .093-IN-GRV-WD	28480	0400-0219
6	0520-0127	6	4	SCREW-MACH 2-56 .188-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
7	0570-0632	3	10	SCREW-SPCL 4-40 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
8				NOT ASSIGNED		
9	1200-0043	8	5	INSULATOR-XSTR ALUMINUM	28480	1200-0043
10	1400-0031	8	3	CLAMP-CABLE .375-DIA .5-WD NYL	28480	1400-0031
11	1400-0249	0	9	CABLE TIE .062-.625-DIA .091-WD NYL	06383	PLT1M-8
12	1400-0510	8	4	CLAMP-CABLE .15-DIA .62-WD NYL	28480	1400-0510
13	1400-0907	7	2	CLAMP-CABLE .187-DIA .5-WD FRTD-NYLON	95987	3/16-HFR
14	1520-0205	2	3	SHOCK MOUNT .31 HGT.	28480	1520-0205
15	2190-0003	8	14	WASHER-LK HLCL NO. 4 .115-IN-ID	28480	2190-0003
16	2190-0006	1	15	WASHER-LK HLCL NO. 6 .141-IN-ID	28480	2190-0006
17	2190-0008	3	1	WASHER-LK EXT T NO. 6 .141-IN-ID	28480	2190-0008
18	2190-0011	8	6	WASHER-LK INTL T NO. 10 .195-IN-ID	28480	2190-0011
19	2190-0045	8	4	WASHER-LK HLCL NO. 2 .088-IN-ID	28480	2190-0045
20	2200-0103	2	4	SCREW-MACH 4-40 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
21	2200-0105	4	111	SCREW-MACH 4-40 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
22	2200-0107	6	1	SCREW-MACH 4-40 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
23	2200-0141	8	1	SCREW-MACH 4-40 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
24	2200-0149	6	10	SCREW-MACH 4-40 .625-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
25	2200-0153	2	4	SCREW-MACH 4-40 .875-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
26	2200-0166	7	3	SCREW-MACH 4-40 .312-IN-LG 82 DEG	00000	ORDER BY DESCRIPTION
27	2360-0111	0	5	SCREW-MACH 6-32 .188-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
28	2360-0113	2	13	SCREW-MACH 6-32 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
29	2360-0114	3	5	SCREW-MACH 6-32 .25-IN-LG 82 DEG	00000	ORDER BY DESCRIPTION
30	2360-0115	4	34	SCREW-MACH 6-32 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
31	2360-0116	5	4	SCREW-MACH 6-32 .312-IN-LG 82 DEG	00000	ORDER BY DESCRIPTION
32	2360-0117	6	10	SCREW-MACH 6-32 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
33	2360-0119	8	10	SCREW-MACH 6-32 .438-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
34	2360-0122	3	1	SCREW-MACH 6-32 .5-IN-LG 82 DEG	00000	ORDER BY DESCRIPTION
35	2360-0197	2	11	SCREW-MACH 6-32 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
35A	2360-0193	8	4	SCREW-MACH 6-32 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
36	2360-0331	6	9	SCREW-MACH 6-32 .25-IN-LG PAN-HD-POZI	28480	2360-0331
37	2360-0333	8	26	SCREW-MACH 6-32 .25-IN-LG 100 DEG	28480	2360-0333
38	2360-0334	9	9	SCREW-MACH 6-32 .312-IN-LG 100 DEG	28480	2360-0334
39	2360-0360	1	2	SCREW-MACH 6-32 .438-IN-LG 100 DEG	28480	2360-0360
40	2420-0002	6	2	NUT-HEX-DBL-CHAM 6-32-THD .109-IN-THK	28480	2420-0002
41	0515-1331	5	16	SCREW-MACH M4x0.7x6mm FH 90	28480	0515-1331
42	0515-0896	5	8	SCREW-MACH M4x0.7x10mm FH 90	28480	0515-0896
43	2680-0129	8	6	SCREW-MACH 10-32 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
44	3050-0066	8	2	WASHER-FL MTLC NO. 6 .147-IN-ID	28480	3050-0066
45	3050-0105	6	4	WASHER-FL MTLC NO. 4 .125-IN-ID	28480	3050-0105
46	3050-0227	3	7	WASHER-FL MTLC NO. 6 .149-IN-ID	28480	3050-0227
47	1250-0915	8	1	CONTACT-RF CONN SER APC-N FEMALE	9D949	131-149
48	1250-1577	0	1	CONNECTOR-RF FEMALE TYPE N	28480	1250-1577
49	2190-0104	0	1	WASHER-LK INTL T 7/16 IN .439-IN-ID	28480	2190-0104
50	2360-0115	4		SCREW-MACH 6-32 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
51	2950-0132	6	1	NUT-HEX-DBL-CHAM 7/16-28-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
52	5040-0306	0	1	INSULATOR	28480	5040-0306
53	08340-00011	6	1	PANEL-REAR (AUX OUTPUT)	28480	08340-00011
54	08340-00056	9	1	DEFLECTOR-AIR	28480	08340-00056
55	08555-20093	5	1	CONTACT JACK	28480	08555-20093
56	08555-20094	6	1	BODY-BULKHEAD	28480	08555-20094
57	08761-2027	4	1	INSULATOR	28480	08761-2027
58	5021-5805	4	1	FRAME-FRONT (METRIC)	28480	5021-5805
59	08340-00076	3	1	CENTER DIVIDER	28480	08340-00076
60	08340-00002	5	1	CHASSIS-RF MOD (REAR)	28480	08340-00002
61	08340-00003	6	1	BRACKET-20-30 MOUNT	28480	08340-00003
62	08340-00004	7	1	BRACKET-MOUNT TRANS	28480	08340-00004
63	08340-00005	8	1	SUPPORT-MOM BOARD	28480	08340-00005
64	08340-00020	7	1	DIVIDER PROCESSOR	28480	08340-00020
65	08340-00029	6	1	GUIDE PLATE-PC BOARDS	28480	08340-00029

Table J-1. Replaceable Miscellaneous Mechanical & Chassis Parts

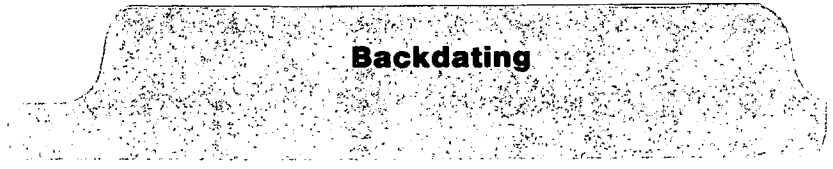
Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
66	08340-00031	0	1	SUPPORT-PC PROCESSOR	28480	08340-00031
67	08340-20051	6	1	SUPPORT-REAR CENTER	28480	08340-20051
68	08340-20234	7	1	FRAME (REAR) MOD (METRIC)	28480	08340-20234
69	08340-20054	9	1	SUPPORT-FRONT CENTER DIVIDER	28480	08340-20054
70	08340-20056	1	1	GUIDE-POWER SUPPLY	28480	08340-20056
71	08340-20236	9	1	STRUT-CORNER (TOP) (METRIC)	28480	08340-20236
72	08340-20238	1	3	STRUT-CORNER MOD (METRIC)	28480	08340-20238
73	85660-00004	6	1	BRACKET-PIVOT PROCESSOR	28480	85660-00004
74	85660-20190	3	1	HOUSING-20-30 MHZ	28480	85660-20190
75	86701-20006	2	1	GUIDE-FRONT PC	28480	86701-20006
76	0360-0037	7	6	TERMINAL-SLDR LUG PL-MTG FOR-#6-SCR	28480	0360-0037
77	1251-4223	1	10	CONTACT-CONN U/W-POST-TYPE FEM CRP	28480	1251-4223
78	1251-6594	3	1	CONNECTOR HOUSING-5 FEMALE IR	28480	1251-6594
79	8120-0579	2	1	CABLE-SHLD 22AWG 5-CNDCT JGK-JKT	28480	8120-0579
80	8150-0005	2		WIRE 22AWG BK 300V PVC 7X30 105C	28480	8150-0005
81	5001-0440	1	2	TRIM-SIDE F.F	28480	5001-0440
82	5040-7201	8	4	FOOT-BOTTOM	28480	5040-7201
83	5040-7202	9	1	TRIM STRIP (TOP)	28480	5040-7202
84	5061-9435	8	1	COVER FM TOP (METRIC)	28480	5061-9435
85	5061-9447	2	1	COVER FM BOTTOM (METRIC)	28480	5061-9447
86	5061-9462	1	1	COVER SIDE (METRIC)	28480	5061-9462
87	5061-9517	7	1	COVER FM PERFORATED (METRIC)	28480	5061-9517
88	5061-2033	8	1	INFO TRAY ASSY KIT	28480	5061-2033
89				NOT ASSIGNED		
90	08340-00074	1	1	HOLDER-PC COVER	28480	08340-00074
91	08340-00040	1	1	HOLDER-POWER SUPPLY BOARDS	28480	08340-00040
92	08340-00060	5	1	PLATE-CAP HOLDER	28480	08340-00060
93	08340-00061	6	1	HOLDER-CAP HOLDER	28480	08340-00061
94	08340-90246	8	1	INFO	CARD #1	2848008340-90246
95	08340-90247	9	1	INFO	CARD #2	2848008340-90247
96	85660-00025	1	1	SHOCK MOUNT	(TOP)	2848085660-00025
97	85660-00027	3	1	INSULATOR-HEAT SINK	28480	85660-00027
98	86701-00028	6	1	SPRING-FLAT	28480	86701-00028
99	1990-0720	1	1	DISPLAY-SPECIAL .1 HI	28480	1990-0720
100	8160-0226	0	12	RFI RND STR .050D	28480	8160-0226
101	08340-00006	9	1	SUPPORT-PC RECT.	28480	08340-00006
102	08340-00008	1	1	CHASSIS RF MOD (FRONT)	28480	08340-00008
103	08340-00064	9	1	POCKET (Holds Cal. Constant Data)	28480	08340-00064
104	6960-0009	1	1	HOLE PLUG .531-D-HOLE	28480	6960-0009
105	0380-0644	4	2	STANDOFF-HEX .400-IN-LG 6-32 THD	28480	0380-0644
106	2200-0164	5	10	SCREW-MACH 4-40 .188-IN-LG	28480	2200-0164
107	5021-3208	7	1	HOUSING-MACHINED	28480	5021-3208
108	86701-00029	7	1	BAFFLE-AIR TOP	28480	86701-00029
109	86701-00024	2	1	SCOOP-AIR	28480	86701-00024
110	86701-00030	0	1	BAFFLE-AIR BOTTOM	28480	86701-00030
111	08340-00067	2		COVER-RECT. BOARD	28480	08340-00067
112	08340-00018	3		FAN FILTER	28480	08340-00018
113	08340-00017	2		GRILL-AIR	28480	08340-00017
114	3030-0152	1	2	SCREW-SET 4-40 .312-IN-LG SMALL CUP PT	28480	3030-0152
115	08340-00016	1	1	FAN HOUSING-BOTTOM	28480	08340-00016
116	08340-00012	7	1	FAN HOUSING-TOP	28480	08340-00012
117	08340-00014	9		FAN GRILL HOUSING	28480	08340-00014
118	1520-0230	3	4	SHOCK MOUNT	28480	1520-0230
119	08340-00016	1	1	BASE PLATE-FAN	28480	08340-00016
120	85660-20092	4	4	RUBBER SHOCK MOUNT	28480	85660-20092
121	2360-0196	1	4	SCREW-MACH 6-32 .375-IN-LG 100 DEG	28480	2360-0196
122	2190-0009	4	2	WASHER-LK INT T NO. 8 .168-IN-ID	28480	2190-0009
123	2510-0051	6	2	SCREW-MACH 8-32 .625-IN-LG PAN-HD-POZI	28480	2510-0051
124	0360-0043	5		TERMINAL-SLDR LUG PL-MTG FOR-NO. 6-SCR	28480	0360-0043
125	1251-6796	7		CONN-POST TYPE	28480	1251-6796
126	0360-1632	0	4	TERMINAL-SLDR LUG LK-MTG FOR-#3/8-SCR	28480	0360-1632
127	0362-0227	1	2	CONNECTOR-SGL CONT SKT 1.14-MM-BSC-SZ	28480	0362-0227
128	1250-0083	1	8	CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0083
129	1250-0102	5	3	CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0102
130	1251-0064	0	1	CONNECTOR 25-PIN F D SERIES	28480	1251-0064
131	1251-2942	7	2	CONNECTOR-RACK & PANEL LOCK	28480	1251-2942
132	1251-3653	9	26	CONNECTOR CONTACT FEMALE .025	28480	1251-3653
133	1251-6781	0	1	CONNECTOR RECEPTACLE 3 MALE CONTACT	28480	1251-6781
134	1251-7374	9	1	CONNECTOR HOUSING-28 FEMALE 2R	28480	1251-7374
135	2190-0016	3	4	WASHER-LK INTL T 3/8 IN .377-IN-ID	28480	2190-0016

Table J-1. Replaceable Miscellaneous Mechanical & Chassis Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
136	2190-0068	5	3	WASHER-LK INTL T 1/2 IN .505-IN-ID	28480	2190-0068
137	2190-0104	0	1	WASHER-LK INTL T 7/16 IN .439-IN-ID	28480	2190-0104
138	2950-0001	8	8	NUT-HEX-DBL-CHAM 3/8-32-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
139	2950-0054	1	3	NUT-HEX-DBL-CHAM 1/2-28-THD .125-IN-THK	00000	ORDER BY DESCRIPTION
140	08340-00082	1	1	REAR PANEL	28480	08340-00082
141	3101-0163	5	1	SWITCH KIT	28480	3101-0163
142	9222-0090	9	1	PLASTIC JACKET (Holds Cal. Constant Data)	28480	9222-0090
143	08340-00070	7	1	BRACKET	28480	08340-00070
144	08340-00089	4	1	A18 MOUNTING PLATE	28480	08340-00089
145	08340-00090	7	1	A16 MOUNTING PLATE	28480	08340-00090
146	08340-00079	6	1	A17 MOUNTING PLATE	28480	08340-00079
147	2200-0164	5	2	SCREW-MACH 4-40 .188-IN-LG	UNCT 82 DEG	00000ORDER BY DESCRIPTION
148	2200-0165	6	5	SCREW-MACH 4-40 .25-IN-LG 82 DEG	00000	ORDER BY DESCRIPTION

Table J-2. HP 8341B Option Configurations

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
				HP 8341B OPTION CONFIGURATIONS		
				OPTION 004: REAR PANEL RF OUTPUT WITH ATTENUATOR		
				DELETE THE FOLLOWING:		
J5	08341-60001	1	1	RF OUTPUT CONNECTOR ASSEMBLY	28480	08341-60001
	08340-20076	5	1	RF CONNECTOR BRACKET	28480	08340-20076
W19	08340-20117	5	1	CABLE ASSY-RIGID COAX A63J2 TO J5	28480	08340-20117
				ADD THE FOLLOWING:		
J20	5061-5304	2	1	RF OUTPUT CONNECTOR (REAR PANEL USE ONLY)	28480	5061-5304
W20	08340-20122	2	1	CABLE ASSY-RIGID COAX A63J2 TO J20	28480	08340-20122
	83592-20063	2	1	PLUG BUTTON-FRONT PANEL	28480	83592-20063
	83595-20004	4	1	FRONT PANEL CONNECTOR SPACER	28480	83595-20004
	1400-0053	4	1	CLAMP-CABLE .172-DIA .375-WD NYL	28480	1400-0053
	2190-0104	0	1	WASHER-LK INTL T 7/16 IN .439-IN-ID	28480	2190-0104
	2950-0132	6	1	NUT-DBL-CHAM 7/16-28-THD .094-IN-THK	28480	2950-0132
	2200-0145	2	1	SCREW-MACH 4-40 .438-IN-LG PAN-HD-POZI	28480	2200-0145
	2190-0019	6	1	WASHER-LK HLCL NO.4 .155-IN-ID	28480	2190-0019
	3050-0105	6	1	WASHER-FL MTLC NO.4 .125-IN-I	28480	3050-0105
				OPTION 806: CHASSIS SLIDE KIT		
				DELETE THE FOLLOWING:		
	5061-9517	7	1	CHASSIS COVER (SIDE) PERFORATED	28480	5061-9517
	5061-9462	1	1	CHASSIS COVER (SIDE)	28480	5061-9462
				ADD THE FOLLOWING:		
	08340-60136	2	1	SLIDE RACK MOUNT	KIT	2848008340-60136
				OPTION 850:INTERFACE CABLE FOR OPERATION WITH HP 8410B/C		
				ADD THE FOLLOWING:		
	08410-60146	9	1	INTERCONNECT CABLE	28480	08410-60146
				OPTION 908: RACK FLANGES WITHOUT HANDLES		
				ADD THE FOLLOWING:		
	5061-9678	1	1	RACK FLANGES WITHOUT HANDLES KIT	28480	5061-9678
				OPTION 913:RACK FLANGES WITH HANDLES		
				ADD THE FOLLOWING:		
	5061-9772	6	1	RACK FLANGES WITH HANDLES KIT	28480	5061-9772


Backdating

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Cable: HEWPACK

February, 1986

S E R V I C E N O T E

SUPERSEDES: None

HP 8341B Synthesized Sweeper

Serial Numbers: 0000A00000 / 9999A99999

Rear Panel to Front Panel Retrofit Instructions

Duplicate Service Notes:

8340A-22
8340B-05
8341A-11

Situation:

This service note contains the parts and process required to retrofit an 8340A/B and 8341A/B option 004 (rear panel output with attenuator) to a standard unit (front panel output with attenuator), and from an option 005 (rear panel without attenuator) to an option 001 (front panel output without attenuator).

This retrofitting can be done to any unit and any serial number.

Solution/Action:

Order parts and follow process.

Continued

DATE: 06 January 1993

ADMINISTRATIVE INFORMATION

SERVICE NOTE CLASSIFICATION: **MODIFICATION AVAILABLE**		
ACTION CATEGORY: AGREEABLE TIME		■ PERFORMANCE ENHANCEMENT ☐ SERVICE/RELIABILITY ENHANCEMENT
LOCATION CATEGORY:	■ CUSTOMER INSTALLABLE ☐ ON-SITE ☐ HP LOCATION	AVAILABLE UNTIL: January 1994
AUTHOR: DM	ENTITY: 5300	ADDITIONAL INFORMATION:

HEWLETT PACKARD

Parts:

Option 004 to Standard Retrofit

Item	Part Number
RF Connector Bracket	08340-20076
Cable Attenuator to Front Panel	08340-20117
Screw (1)	2360-0333
Screw (1)	2360-0122
Resistor 2.37K 1% .125W	0698-3150
Resistor 2.61K 1% .125W	0698-0085

Option 005 to Option 001 Retrofit

Item	Part Number
RF Connector Bracket	08340-20076
Cable Attenuator to Front Panel	08340-20121
Screw (1)	2360-0333
Screw (1)	2360-0122
Resistor 2.37K 1% .125W	0698-3150
Resistor 2.61K 1% .125W	0698-0085

Procedure:

This process applies to the HP 8340A/B and the HP 8341A/B. The steps are identical for each of the 4 products.

1. Switch the instrument to STANDBY. Remove the power cord. Remove the top cover.
2. Completely remove the front panel (you must disconnect A62J9, J15, J16, J26, A61W1P1, W1P2, and the ground wire connected to A6P2).
3. Disconnect the A62J10 SMB cable (front of instrument).
4. Disconnect the sense resistor assembly cable (A47W1) from connector A62J29.

   Unscrew the ground lug next to A62J29.

5. Remove the semi-rigid cable W3 (connects YO loop output to the A16 modulator/splitter).

CAUTION

The A63RF attenuator and the A10 directional coupler connectors are 3.5 mm, and the RF output cable connector is SMA. Take extreme care when disconnecting or connecting an SMA cable and a mating 3.5 mm connect. The SMA cable center conductor must align with the 3.5 mm connector center conductor. If there is any axial force on the cable when disconnecting the SMA fitting, the 3.5 mm connector center conductor can be damaged.

6. Disconnect the RF output cable from the attenuator (standard instrument) or the directional coupler (option 005).
7. Remove the RF output cable and connector. Remove the cable from the connector. Attach the connector to the bracket and connect the new cable (08340-20117 on standard unit and 08340-20121 on option 001).
8. Remove the front panel plug button labeled RF OUTPUT.
9. Remove the pem (pressed in nut) from front panel next to the RF connector (see figure 1). This nut is a pressed in part. To remove the pem drive it out by putting a screw into the pem from the bottom side and a socket on the other side for support while driving it out. Take care in removing the pem, if the frame is broken a new front frame will need to be installed.

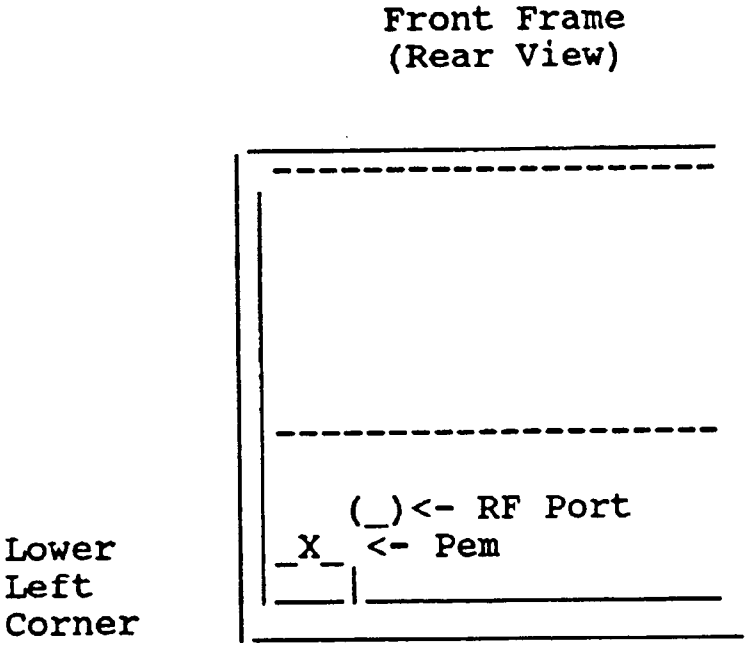


Figure 1

10. Connect the RF output cable to the attenuator (standard instrument) or to the directional coupler (option 001).

11. Secure the RF output connector's mounting bracket on the front frame using 1 (2360-0333) screw in the second hole from the end.

    For proper alignment of the RF output connector and cable W19 or W20, you may need to install both screws that mount the RF output connector bracket. If this is the case, the mounting bracket screw closest to the instrument's side panel must be removed before installing the front panel.

12. On standard instruments tighten the connectors on the directional coupler to attenuator cable, and the connectors on the attenuator to the RF output cable. On Option 004 instruments tighten the connectors on the directional coupler to RF output connector cable.

13. Reinstall the front panel and reconnect the cables removed in steps 2 through 5.

14. Install the plug in the hole for the rear panel RF output.

15. Remove the A27 level control assembly.

    Replace A27R70 jumper wire with a 2.37K ohm resistor (0698-3150) and add A27R71 a 2.61K ohm resistor (0698-0085).

16. To access and change the calibration constants to reflect the retrofit to front RF output, press:

    [SHIFT] [GHz] [5] [9] [Hz]
    [SHIFT] [MHz] [1] [2] [Hz]
    [SHIFT] [KHz] [2] [2] [Hz]

    Cal Constant 59 - For instruments retrofitted to a standard configuration (front RF output with attenuator), add 200 to the value of calibration constant 59 (shown in the entry display). With the keyboard, enter this new number, and press [Hz]. This turns off the attenuator switching at an ALC level of -12dBm.

    Cal Constant 60 - For both retrofits (from rear to standard and option 004) cal constant 60 needs to be reset. To access cal constant 60, press the up arrow step key. Subtract 4 from the cal constant value. Enter the new number and press [Hz]. This removes the rear panel calibration constant configuration.

    To store the working calibration data (and the new values for cal constants 59 and 60) in the protected area, press:

    [SHIFT] [MHz] [1] [4] [Hz]
    [SHIFT] [KHz] [5] [3] [4] [9] [Hz]

    Enter the new values for the cal constants 59 and 60 on the calibration data hard copy, located under the instrument top cover.

17. Perform steps 1 through 31 of the flatness verification and adjustment procedure in paragraph 5-38 of the HP 8340 Operating and Service Manual.

18. Because the values for the cal constants 13 through 16 were changed in step 18, store the new values in protected data by pressing:

    [SHIFT] [MHz] [1] [4] [Hz]
    [SHIFT] [KHz] [5] [3] [4] [9] [Hz]

19. To access cal constant 13, press:

    [SHIFT] [GHz] [1] [3] [Hz]
    [SHIFT] [MHz] [1] [2] [Hz]
    [SHIFT] [KHz] [2] [2] [Hz]

    Note the value of cal constant 13 in the ENTRY DISPLAY, and update the cal constants hard copy to reflect the new value.

20. To access cal constants 14 through 16, press the up arrow step key.

    Update the cal constants hard copy to reflect the new values.

21. Verify the instruments' operation by performing the frequency range and CW mode accuracy test in paragraph 4-10, and the maximum leveled output power and power accuracy test in paragraph 4-14 of the Operationg and Service Manual.

ANDERSON,ERIC / HPATC3/02 - HPDesk print.

Message. Dated: 03/05/93 at 1214.
Subject: MID Service Memo
Sender: Sally CARSTENSEN / HP5300/M0 Contents: 2.
TO: Eric ANDERSON / HPATC3/02

Part 1.

TO: DISTRIBUTION

Part 2.

8340-1192-1

INTER-OFFICE SERVICE MEMO

March 5, 1993

To: ALL HP INSTRUMENT SALES AND SERVICE OFFICES

FROM: MICROWAVE INSTRUMENT DIVISION (5300)
SANTA ROSA, CALIFORNIA 95403-1799

SUBJECT: HP 8340A opt. H02 UPGRADE KIT
HP 8341A opt. H19 UPGRADE KIT
HP 8341B opt. 003 UPGRADE KIT

SERIAL NUMBERS AFFECTED

HP 8340A opt. H02 SERIAL PREFIX 2801A AND BELOW
HP 8341A opt. H19 SERIAL PREFIX 2743A AND BELOW
HP 8341B opt. 003 SERIAL PREFIX 2745A AND BELOW

DESCRIPTION This document describes MID's strategy and policies for four service kits for the HP 8340 (HP 8340A/B and the 8341A/B) product family. These kits are for upgrading the hardware and software in the HP 8340A option H02, 8341A option H19 and the 8341B option 003. Performing this upgrade allows these instruments to be field supportable.

WHY WEREN'T THE EARLY VERSIONS FIELD SUPPORTABLE? These three models provide improved performance (lower harmonics) over the standard instrument. This is accomplished by using a 2 ball SYTM in the RF section. Initially, instruments with a two ball SYTM was difficult to service. We learned that a high degree of specialization was required for our production technicians to adjust one of these instruments. Therefore, we decided that any repair or adjustment to the RF section could not be performed in the field. In fact, the only way to successfully

support these instruments has been to return them to the MID for service.

In September 1987 the high band amplifier was replaced with the amplifier detector.

The new circuitry makes the instrument field supportable by making the adjustments easy to perform. The assemblies in each of these kits allows the field to convert these instruments to the new design.

UPGRADE KIT

Table 1-1 Upgrade Kits

Model	Standard Kit
HP 8340A opt. H02 2801A and below	08340-60351
HP8341A opt. H19 2743A and below	08340-60351
HP 8341B opt 003 2745A and below	08341-60032

Table 1-1 list the instrument model numbers, the serial prefixes affected and the kit part numbers that are available. Each kit contains several assemblies (table 1-2 and table 1-3), a set of UVEPROMs, connectors, documentation, and assorted hardware. The documentation includes an HP 8341B option 003 manual set and detailed instructions for installing the upgrade kit. Once modified, the instrument can be repaired or adjusted in the field.

Table 1-2 HP 8340A opt H02 and HP 8341A opt H19 Kits

Assemblies in the 08340-60351	
A14	High Band Amp/Detector
A20	RF Filter
A21	Pulse Mod Driver
A22	RF Clamp/SRD Bias
A24	Attenuator Driver
A25	ALC Detector
A26	Linear Modulator
A28	SYTM Driver

INTERNAL USE ONLY

INTER-OFFICE SERVICE MEMO 1-2

Table 1-3, HP 8341B opt 003 Kits

Assemblies in the 08341-60032	
A14	High Band Amp/Detector
A20	RF Filter
A21	Pulse Mod Driver
A22	RF Clamp/SRD Bias
A24	Attenuator Driver

HOW TO IDENTIFY AN INSTRUMENT THAT HAS BEEN UPGRADED

Remove the cover from the bottom of the instrument. An instrument that has been upgraded will have an A22 (Clamp/SRD Bias) printed circuit assembly installed. If there is no A22 assembly in the instrument, it has not been upgraded.

IMPLEMENTATION

This upgrade should be performed only when a repair or adjustment is required in the RF or ALC section of one of the following models:

- HP 8340A option H02 with serial prefix 2081A and below.
- HP 8341A option H19 with serial prefix 2743A and below.
- HP 8341B option 003 with serial prefix 2745A and below.

WHO PAYS?

MID will accept warranty charges for installation of the exchange kit and instrument performance test for instruments that qualify. MID will not accept the billings for upgrades performed during routine preventive maintenance, calibration, or non related instrument repair or adjustments. MID will accept billings until February 1, 1995.

If customers request the upgrade and there is no failure in the instrument, the upgrade can be performed at customers expense.

INTERNAL USE ONLY

INTER-OFFICE SERVICE MEMO 1-3

HOW TO BILL MID

For instruments in warranty, bill the cost for the repair and the upgrade as a repair type 02N. Please use the appropriate repair classification for the failure.

For instruments that are out of warranty, bill the cost of the repair to customer and bill the cost of the upgrade to MID as repair type 02G. Use repair classification of MO (modification).

For extended warranty repairs under MID's two year microcircuit warranty, bill the cost for the repair and the upgrade as repair type 02G. Please use the appropriate repair classification for the failure.

ORDERING INFORMATION The kits are set up at SMO and can only be ordered by HP service people. Please use the appropriate repair classification for the failure.

INSTALLATION This is an extensive upgrade and it should be performed ONLY at a HP service center. In addition to replacing several assemblies, a new set of UVPROMs and a new printed circuit assembly (A22) will be installed. The new circuit assembly requires soldering an edge connector and several jumper wires to the mother board. A full performance test must be performed on the upgraded instrument.

SUPPORT EQUIPMENT A microwave test station is required to performance test the instrument.

SPECIAL TOOLS REQUIRED An anti static work surface is required.

A 60 watt soldering iron (with grounded tip) and a short #8 soldering tip (HP P/N 8690-0073) is required when soldering to the mother board. This will supply sufficient heat to the mother board without damaging the assembly.

PERFORMANCE TEST Since a full performance must be performed on the upgraded instrument MID recommends using the HP 11877A Performance Test software. MID will not accept labor cost for manual performance test.

TRAINING No special training is required. Complete instructions are included with each kit.

WARRANTY The normal warranty for the upgrade kit will not be affected. Parts supplied in the kit are covered by the standard parts warranty.

CUSTOMER SUPPORT CONTACT MID Factory Support
Dan McNamee
Telnet 577-2201
Non Telnet (707) 577-2201

INSTALLATION NOTE

Supersedes: P-08341-69032

SUPPORT UPGRADE FOR HP 8341B OPTION 003

PURPOSE

The purpose of this Installation Note is to provide instructions on how to upgrade an HP 8341B Option 003 instrument, so that, any future service requirements can be performed by any qualified service person.

Table 1. Contents of the Package (HP Part Number 08341-60032)

Quantity	Description
1	A14 High Band Power Amplifier
1	A20 RF Filter
1	A21 Pulse Modulator Driver
1	A22 RF Clamp/SRD Bias
1	A24 Attenuator Driver
1 set	A60U34 through U37 UVEPROMs
1	A26R87, 3k Ohm Resistor
1	A13A1R1, 100 Ohm Resistor
1	A13A1C1, 1000 pF Capacitor
1	XA22 PC Board Connector
1	A62J21 SMA Connector
1	Coax Cable (A14J3 to A62J21)
4	IC Sockets
3.5 ft (109 cm)	Wire
5	Jumper Wires
1	Tube of Epoxy
1	Label, A62 Motherboard Part Number
1	Installation Note, Support Upgrade for HP 8341B Option 003
1 set	HP 8341B Option 003 Operating and Service Manual

INSTRUMENTS AFFECTED

Any HP 8341B Option 003 instrument prior to and including, serial prefix number 2730A (unless previously modified, identified by the presence of an A22 RF clamp/SRD bias assembly), requires this support upgrade.

DESCRIPTION OF THE UPGRADE PROCEDURE

In this procedure, you will:

- inspect and modify the calibration constants.
- modify and replace hardware.
- adjust the instrument.
- fully performance test the instrument.

HP Part Number 08341-90121
Printed December 1990

HEWLETT PACKARD

CAUTION

STATIC SENSITIVE DEVICES

You will be handling assemblies that have static sensitive components. Use an anti-static wrist strap and work on an anti-static surface. Never place assemblies on a surface covered with static generating material.

PROCEDURE

Initial Operating Inspection

1. Connect the power cord and turn the instrument ON. Verify that both INSTR CHECK LEDs turn off after the instrument completes self test. The OVEN LED will be on and possibly the UNLK LED as well. After *15 minutes* warm up however, none of the red warning LEDs should be on.

   If the above sequence does not occur, refer to the "In Case of Difficulty" section located in Volume 1 of the Option 003 manual.

2. Activate the instruments PEAKING function. Press **[SHIFT] [PEAK]**. Verify that no front panel, fault indicators are on.

3. Activate the instrument's controller diagnostics. Press **[SHIFT] [M4]**. The ENTRY DISPLAY indicates, first, `DIAGNOSTIC TESTS IN PROGRESS`, then the diagnostic results. `TEST: ? FULL DIAGNOSTIC PASS`, will be displayed if passed otherwise, it will display an error code. If the diagnostic fails, refer to the A60 processor troubleshooting information in the Option 003 manual.

Inspecting and Verifying Calibration Constants

4. Switch the instrument to STANDBY and disconnect the power cord. Remove the top cover. Remove the printed (backup) copy of the instrument's calibration constants that is stored in a bracket on the inside of the instrument.

   The calibration constants are stored in memory on the A60 processor assembly. The UVEPROMs will be replaced with the ones provided in this installation kit. Therefore, the instrument's calibration constants must be verified before replacing the UVEPROMs.

   Calibration constant verification consists of: inspecting the instrument's calibration constants and comparing the displayed calibration constants to the printed copy of the constants and if necessary changing the printed copy so that they both agree.

5. Connect the power cord and turn the instrument ON.

6. On the instrument press:

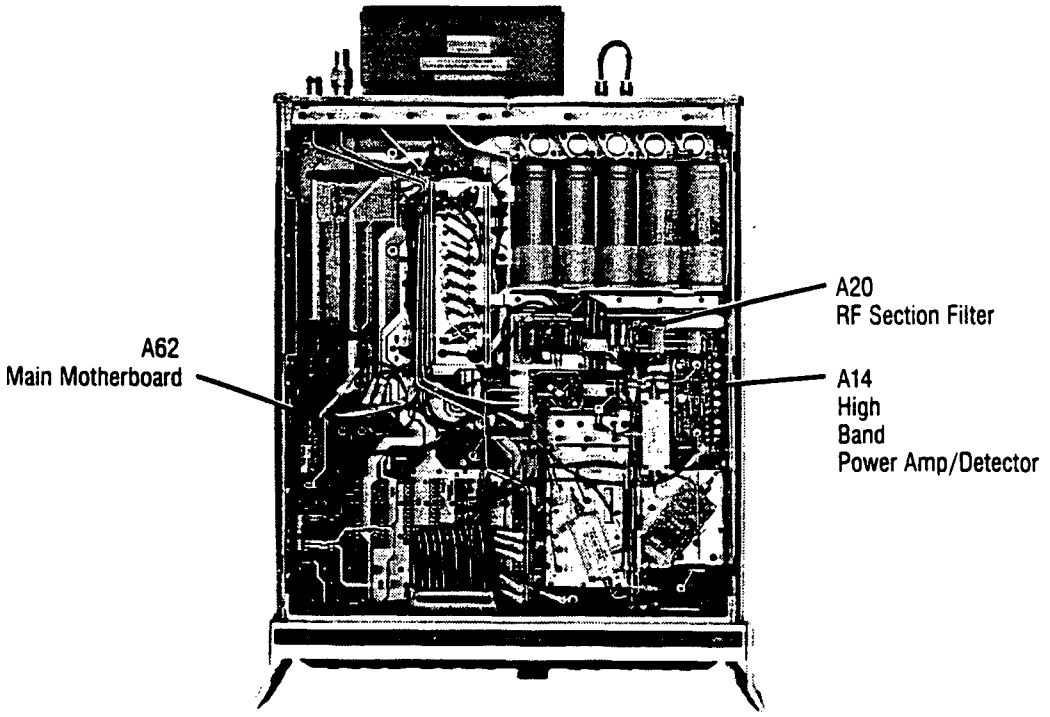
   [SHIFT] [GHz] [1] [Hz]
   [SHIFT] [MHz] [1] [2] [Hz]
   [SHIFT] [kHz] [2] [2] [Hz]

   Calibration constant 1 and its value are displayed on the entry display. For calibration constant 1, compare the printed copy value to the number in the entry display. If the numbers are not the same, change the printed copy to the number that is in the entry display.

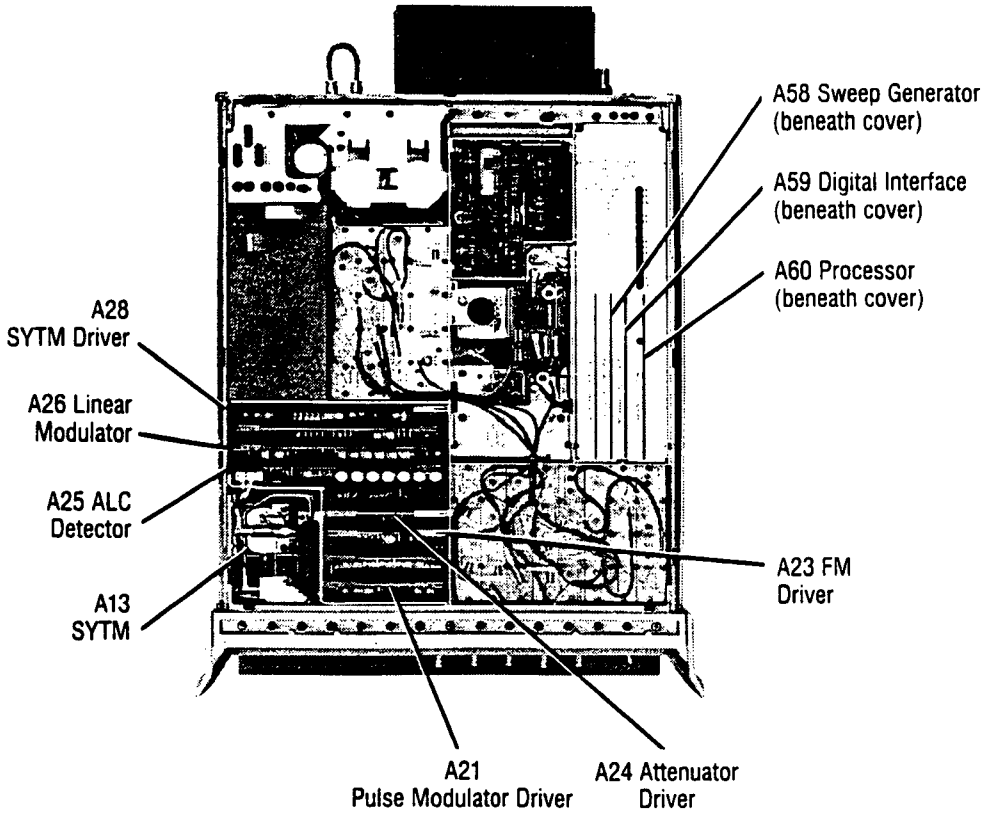
7. Press the UP ARROW key [▲] to advance to the next calibration constant. Compare the printed value to the displayed value and if necessary change the printed copy so that they are the same value.

8. Repeat step 7 until 98 calibration constants are inspected, verified, and corrected on the printed copy as necessary. Calibration constant 99 is a CHECKSUM and is updated each time a calibration constant is changed.

9. Switch instrument to STANDBY. Disconnect power cord.



a) Top View



b) Bottom View

Figure 1. Assembly Locations

Modifying the Hardware

10. Remove the bottom and perforated side covers.

11. Place the instrument on its left side (as viewed from the front).

12. Place the RF section (hinged deck) in the service position. Refer to Figure H-24 in Volume 3 of the Option 003 manual.

13. Refer to Figure 1. Locate and remove the assemblies listed below.

    A20 RF filter
    A21 pulse driver
    A23 FM driver
    A24 attenuator driver

    Set these assemblies aside.

CAUTION

In several of the following steps you will solder connectors and jumper wires to the A62 motherboard. The motherboard is a multi-layer assembly which, if damaged, necessitates the return of the entire instrument to the factory for repair. Use extreme caution when soldering to this assembly.

NOTE: Use a 60 watt soldering iron (with a grounded tip) and a short #8 soldering tip (HP P/N 8690-0073) when soldering to the motherboard. These supply sufficient heat to the motherboard without damaging the assembly.

14. Install SMA connector J21 (provided in this package) in the opening on the motherboard labeled J21. Refer to Figure 2.

15. Install XA22 PC edge connector (provided in this package) in the opening on the motherboard labeled XA22.

16. Place the instrument in its normal operating position.

CAUTION

Do not open the RF deck more than 45° from its closed position to avoid crushing A20 components mounted near the RF deck hinge.

17. Use a pencil or a similar non-conductive object to hold the RF section in the open position.

18. Refer to Figure 2. Install the following jumper wires:

FROM	TO	MNEMONIC
A22 pin 7	A27 pin 13	SYTM TEMP
pin 8	A21 pin 19	BIAS S/H PULSE
pin 12	A21 pin 29	L HET
pin 16	A21 pin 34	SPARE
pin 17	A21 pin 27	HRFON
pin 25	A24 pin 20	HLB0
pin 26	A24 pin 21	HLB1
pin 27	A24 pin 22	HLB2
pin 30	A24 pin 6	+1.4V/GHz
pin 31	A24 pin 25	SRD BIAS
pin 35	A24 pin 35	SYTM GND
pin 36	A24 pin 36	REFGND
pin 34	A26 pin 20	MODHI

19. Use the epoxy supplied in this package, to secure the jumper wires installed in the previous step to the A62 motherboard.

20. Place the 60289 label supplied in this package, onto the A62 motherboard over the 60234 number located adjacent to A62J31.

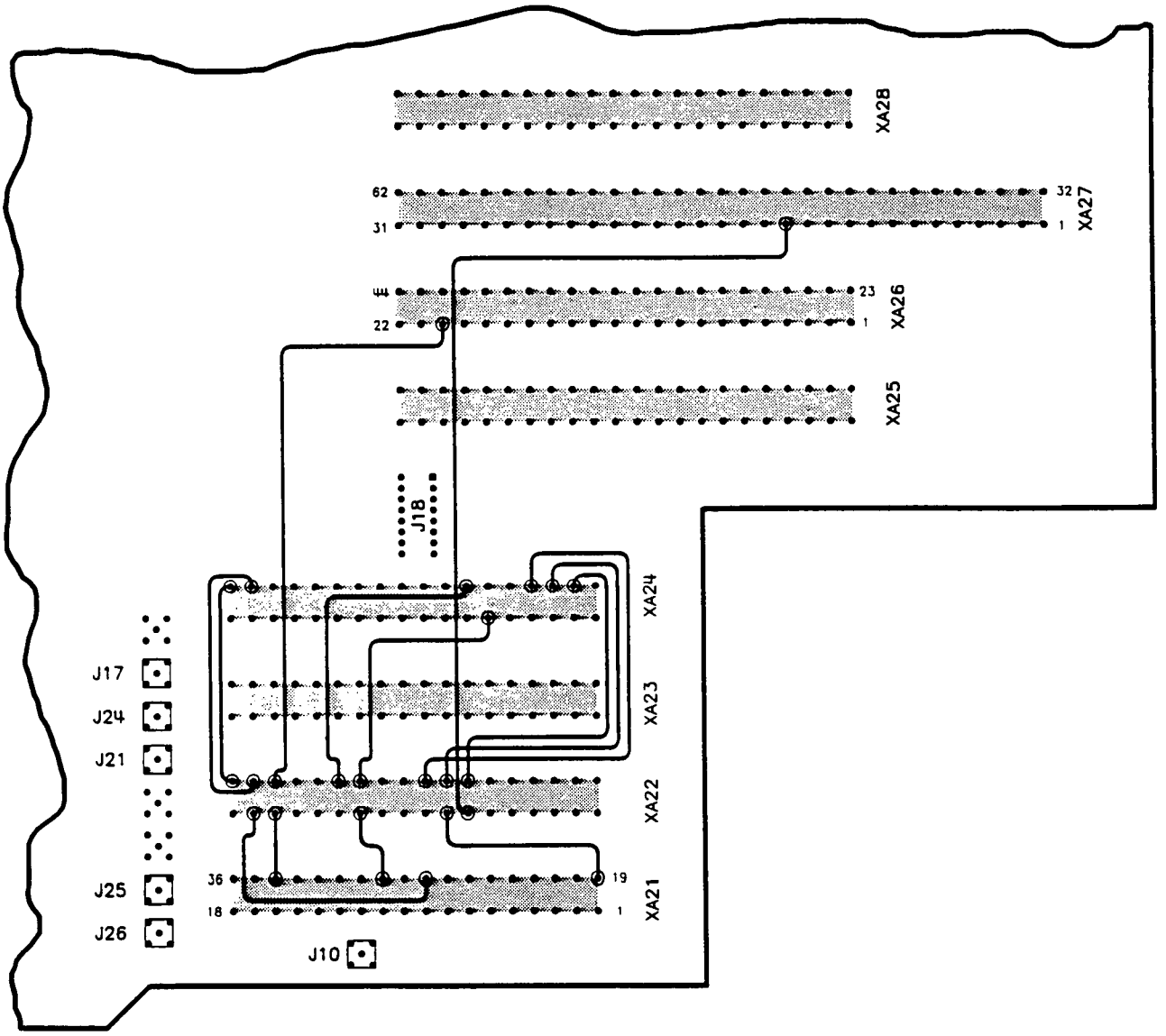


Figure 2. A62 Motherboard Jumper Wire Locations

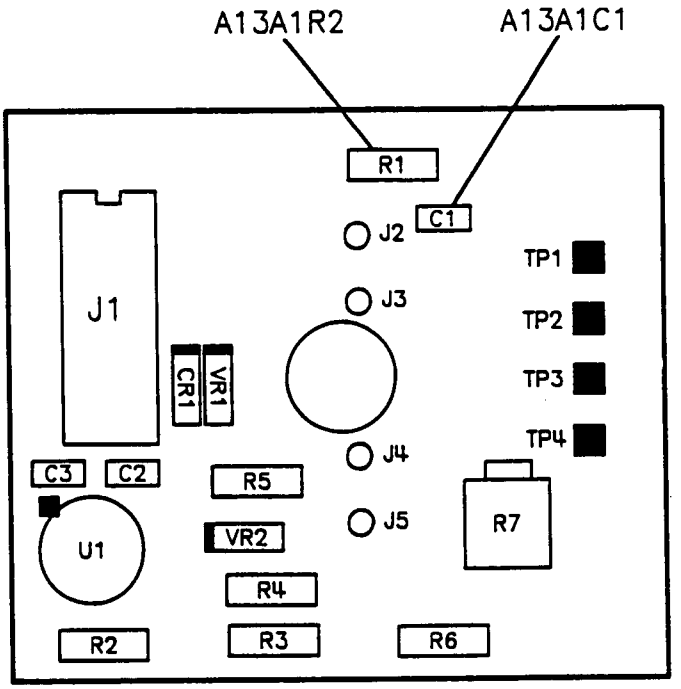


Figure 3. A13A1 SYTM Bias Assembly Component Locations

CAUTION

STATIC SENSITIVE DEVICES

The A13 SYTM BIAS ASSEMBLY is VERY static sensitive. Use an anti-static wrist strap, grounded tip soldering iron, and work on an anti-static surface. Never place the assembly on a surface covered with static generating material.

21. Remove the A13 high band SYTM assembly. Refer to the "A13 High Band SYTM Replacement Procedure", located in the RF section, in Volume 3, of the Option 003 manual.

    a. Refer to Figure 3. Locate and remove A13A1R1 and A13A1C1.

    b. Install A13A1R1 and A13A1C1 provided in this package into the SYTM bias assembly.

22. Replace the A13 high band SYTM assembly. Close the RF deck and reverse the access procedure.

23. Refer to Figure 4. Locate and remove the A14 high band power amplifier. Set it aside.

NOTE: To remove A14, it may be necessary to remove A20J3 ribbon cable. Note the orientation before removal.

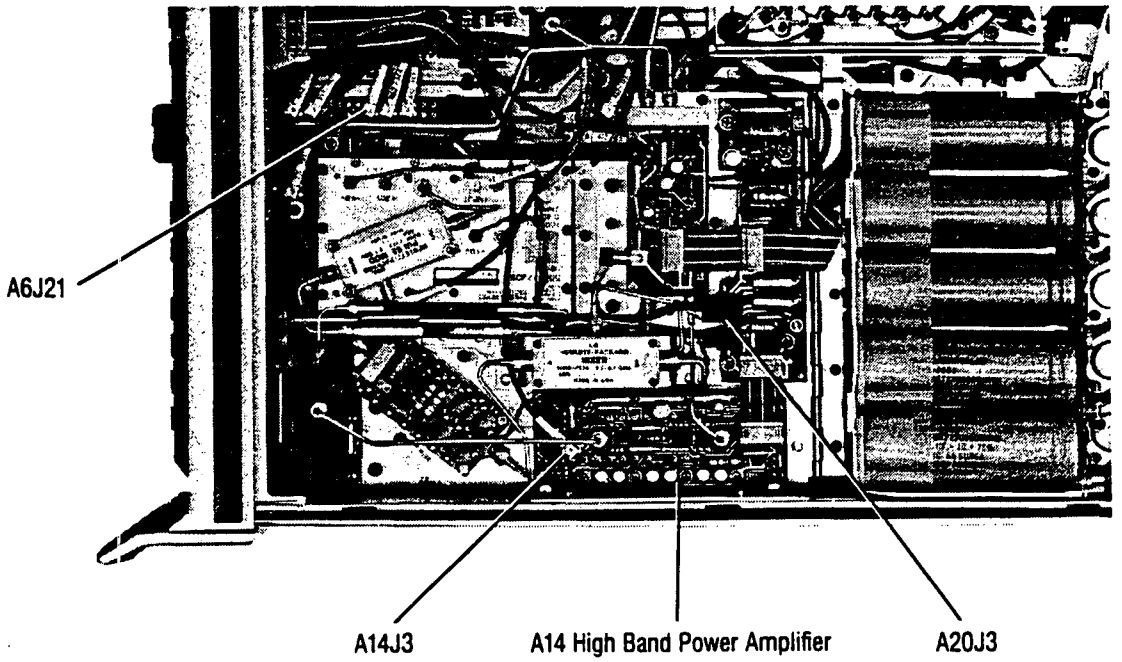


Figure 4. Location of A14 High Band Power Amplifier and Associated Components After Installation

24. Install the A14 amplifier provided in this package into the instrument.

25. Refer to Figure 4. Install the coaxial cable, J21, provided in this package between A14J3 and A62J21.

26. Install the A20, A21, A22, and A24 assemblies provided in this package into their respective connectors. Install the original A23 assembly into its connector.

27. Refer to Figure 1. Locate and remove the A25 ALC detector assembly.

28. Refer to Figure 5. Insert a jumper wire (W1, provided in this package) into location A25W1 and solder into place. Remove the A25W2 jumper wire. Reinsert the A25 assembly.

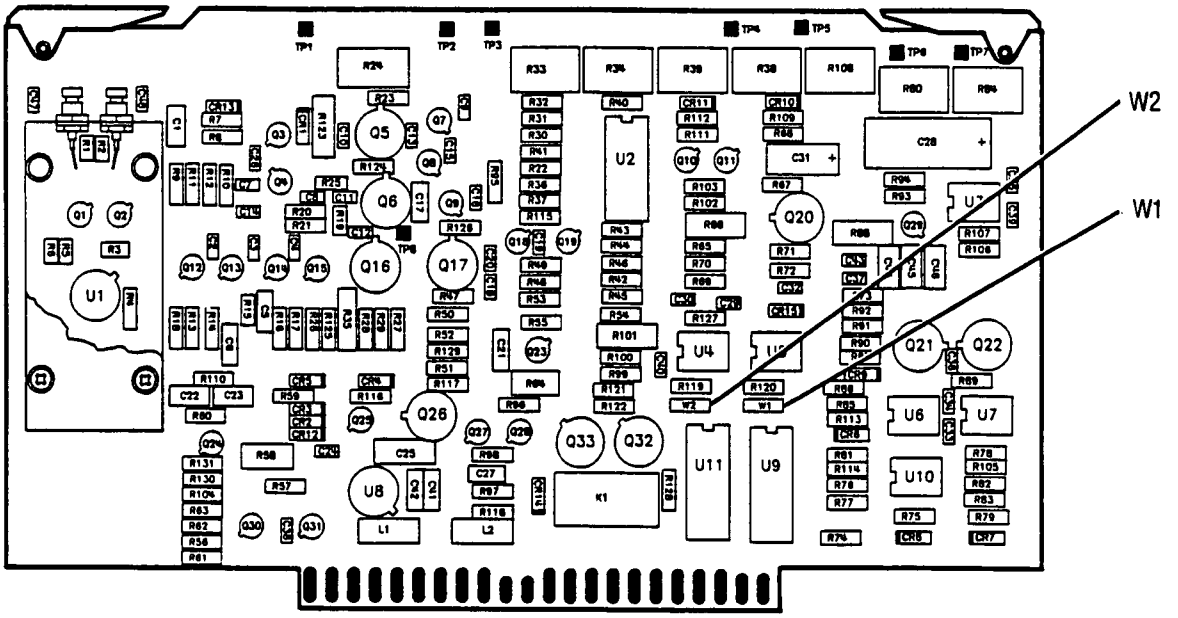


Figure 5. Location of W1 & W2 on the A25 ALC Detector

29. Refer to Figure 1. Locate and remove the A26 linear modulator assembly.

30. Refer to Figure 6. Locate and remove A26R87 and replace it with the 3k resistor provided in this package. Locate jumpers W1 and W2. Solder W1 into position "B". Solder W2 into position "C".

31. Note and record the part number of the A26 assembly.

    A26 Linear Modulator _____

    Reinsert the A26 assembly.

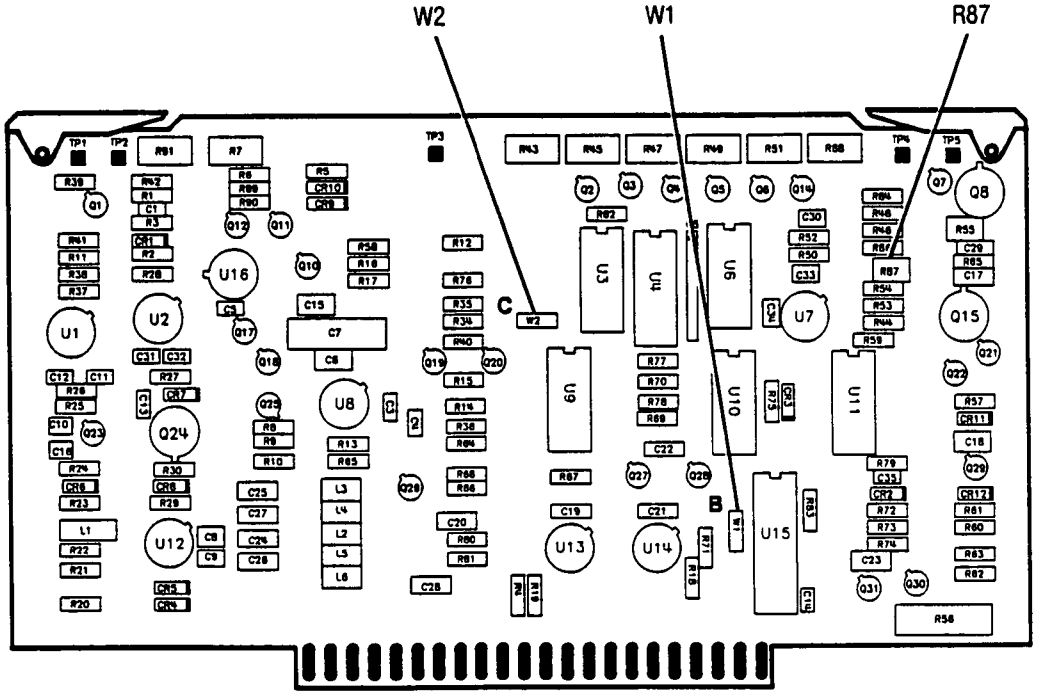


Figure 6. A26 Linear Modulator Component Locations

Replacing UVEPROMs

32. Refer to Figure 1. Remove the controller section cover. Locate and remove the A60 processor assembly.

33. Locate and remove the four UVEPROMs from the A60 assembly (see Figure 7).

NOTE: Early revisions of the instrument firmware required two UVEPROMs (U36 and U37). This revision requires four (U34 through U37).

34. If the processor assembly does not have sockets for the UVEPROMs, use the four sockets provided in this package (solder the sockets in the positions shown in Figure 7).

35. Insert each UVEPROM in the appropriate socket.

NOTE: Notch indicates pin 1 position.

36. Replace the A60 assembly in the instrument. Do not replace the controller section cover yet.

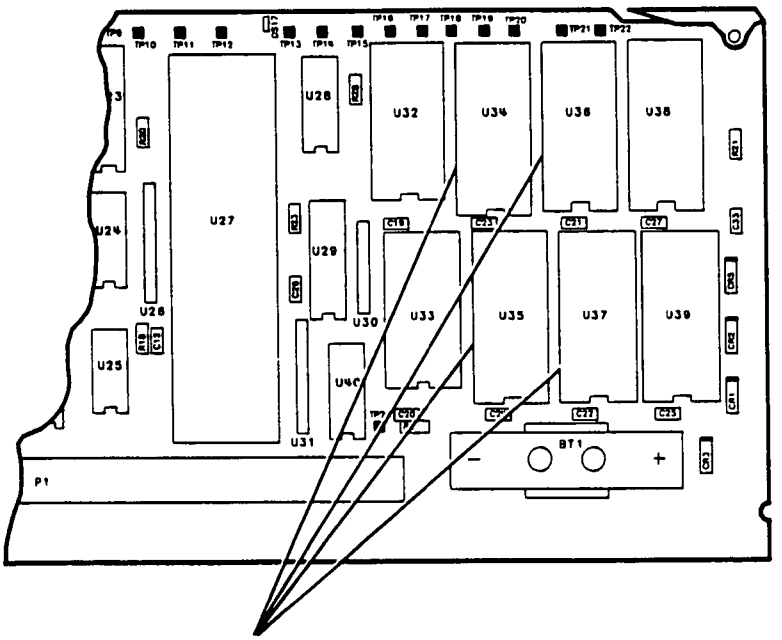
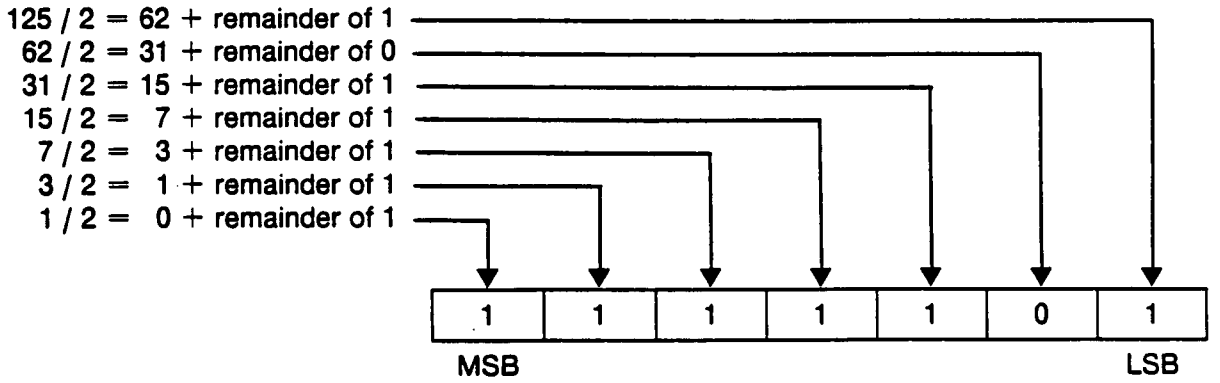


Figure 7. A60 UVEPROM Locations

Tutorial – Decoding Calibration Constants

To decode a calibration constant, read the decimal number of the calibration constant and determine the binary equivalent.

To determine the binary equivalent of a decimal number, use the method of repeated division by two. For example, beginning with the LSB (least significant bit) and ending with the MSB (most significant bit), find the binary equivalent of decimal number 125 as follows:



The binary equivalent of decimal number 125 is 1111101. The LSB is the first remainder, and the right most binary bit.

NOTE: Because a binary number derived from a decimal number may or may not have 16 bits, when you fill in the table for a calibration constant binary equivalent, write the binary number from right to left, from the LSB. Fill in any remaining bits with zero.

Decoding and Calculating Calibration Constants

37. Inspect, decode, and possibly recalculate the following calibration constants. Follow the instructions for each calibration constant and make all indicated changes on the *printed copy*.

    Calibration Constants: 54, 55, 56, 59, and 83

38. For calibration constant **54**, change 20,000 to 2,000 on the printed copy.

39. For calibration constant **55**, change the printed copy from 10 to 1.

40. For calibration constant **56**:

    a. Read the value of calibration constant 56 from the printed copy and enter that value on line A in Table 2. This is the decimal value for calibration constant 56.

Table 2. Calibration Constant 56 Computation

A. Decimal Value of Calibration Constant 56	
B. Decimal value of Bit 14	+ 16384
C. Results	

    b. Determine the binary equivalent of the decimal number on line A using the method of repeated division by 2 (see Tutorial). Write the binary value in Table 5. Remember to write the number from right to left.

Table 3. Calibration Constant 56 Binary Equivalent

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																	LSB

c. Locate and read bit 14. If bit 14 is a "1", the calibration constant is correct; go to step 41. If not, go to step 40d.

d. Add lines A and B of Table 2. Enter the results both on line C, and on the printed copy for calibration constant 56.

41. For calibration constant **59**:

a. Read the value of calibration constant 59 from the printed copy and enter that value on line A in Table 3.

Table 3. Calibration Constant 59 Computation

A. Decimal Value of Calibration Constant 59
B. Decimal value of Bit 14 & 13 _____
C. Temporary Results
D. Decimal value of Bit 11 _____
E. Results

b. Determine the binary equivalent of the decimal number on line A in Table 3 using the method of repeated division by 2. Write the resulting binary equivalent in Table 4.

Table 4. Calibration Constant 59 Binary Equivalent

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																	LSB

c. Refer to step 31.

If the part number of the A26 linear modulator assembly is:

08340-60021, go to step 41f.

08340-60156 or 08340-60212, go to step 41e.

08340-60264 or higher, go to step 41d.

d. Locate and read bits 14 and 13. If bit 14 is a "0" and bit 13 is a "1", they are correct. Copy the number from line A to line C and go to step 41g.

If bit 14 is a "0" and bit 13 is a "0", write 8192 on line B of Table 3. Add lines A and B and enter the results on line C. Go to step 41g.

If bit 14 is a "1" and bit 13 is a "0", write 8192 on line B of Table 3. Subtract line B from A and enter the results on line C. Go to step 41g.

If bit 14 is a "1" and bit 13 is a "1", write 16384 on line B of Table 3. Subtract line B from A and enter the results on line C. Go to step 41g.

e. Locate and read bits 14 and 13. If bit 14 is a "1" and bit 13 is a "0", they are correct. Copy the number from line A of Table 3 to line C and go to step 41g.

If bit 14 is a "0" and bit 13 is a "0", write 16384 on line B of Table 3. Add lines A and B and enter the results on line C. Go to step 41g.

If bit 14 is a "0" and bit 13 is a "1", write 8192 on line B of Table 3. Add lines A and B and enter the results on line C. Go to step 41g.

If bit 14 is a "1" and bit 13 is a "1", write 8192 on line B of Table 3. Subtract line B from A and enter the results on line C. Go to step 41g.

f. Locate and read bits 14 and 13. If bit 14 is a "0" and bit 13 is a "0", they are correct. Copy the number from line A of Table 3 to line C and go to step 41g.

If bit 14 is a "0" and bit 13 is a "1", write 8192 on line B of Table 3. Subtract line B from line A and enter the results on line C. Go to step 41g.

If bit 14 is a "1" and bit 13 is a "0", write 16384 on line B of Table 3. Subtract line B from line A and enter the results on line C. Go to step 41g.

If bit 14 is a "1" and bit 13 is a "1", write 24576 on line B of Table 3. Subtract line B from A and enter the results on line C. Go to step 41g.

g. Remove the A58 sweep generator assembly. Note its part number below.

A58 Sweep Generator _____

Reinsert the A58 assembly in the instrument.

h. If the A58 part number is:

08340-60298, go to step j.

08340-60154, go to step i.

i. In Table 4, locate bit 11. For the 08340-60154 assembly, bit 11 must be a "0".

If bit 11 is a "0", copy the number from line C in Table 3 to both line E, and the printed copy for calibration constant 59. Go to step 42.

If bit 11 is a "1", write 2048 on line D in Table 3. Subtract line D from line C. Enter the results on both line E, and the printed copy for calibration constant 59. Go to step 42.

j. In Table 4, locate bit 11. For the 08340-60298 assembly, bit 11 must be a "1".

If bit 11 is a "1", copy the number from line C in Table 3 to both line E, and the printed copy for calibration constant 59. Go to step 42.

If bit 11 is a "0", write 2048 on line D in Table 3. Add line D and line C. Enter the results on both line E, and the printed copy for calibration constant 59. Go to step 42.

42. For calibration constant **83**, change the printed copy from "unused" to "Analyzer Sweep Rate" with a value of 178.

43. Locate and remove the A59 digital interface assembly (Figure 1) and the A28 SYTM driver assembly. Record their part numbers in the space provided below.

A28 SYTM Driver _____

A59 Digital Interface _____

44. On the A59 digital interface assembly, inspect jumpers W1, W2, W3 (see Figure 8).

a. If the A28 SYTM driver assembly part number is 08340-60213, 08340-60256, or 08341-60016, install A59W1 and go to step 44c. If not, go to step 44b.

b. If the A28 SYTM driver assembly part number is 08340-60015, 08340-60025, or 08340-60159, remove A59W1 and go to step 44c.

c. If the A59 digital interface assembly is part number 08340-60013, 08340-60153, or 08340-60226, install A59W3.

45. Insert the A28 SYTM driver and A59 digital interface assemblies into the instrument.

NOTE: The instrument's FAULT annunciator and, potentially, one or more of the other failure indicators are on. This is normal. After you perform step 53, all failure indicators should turn off.

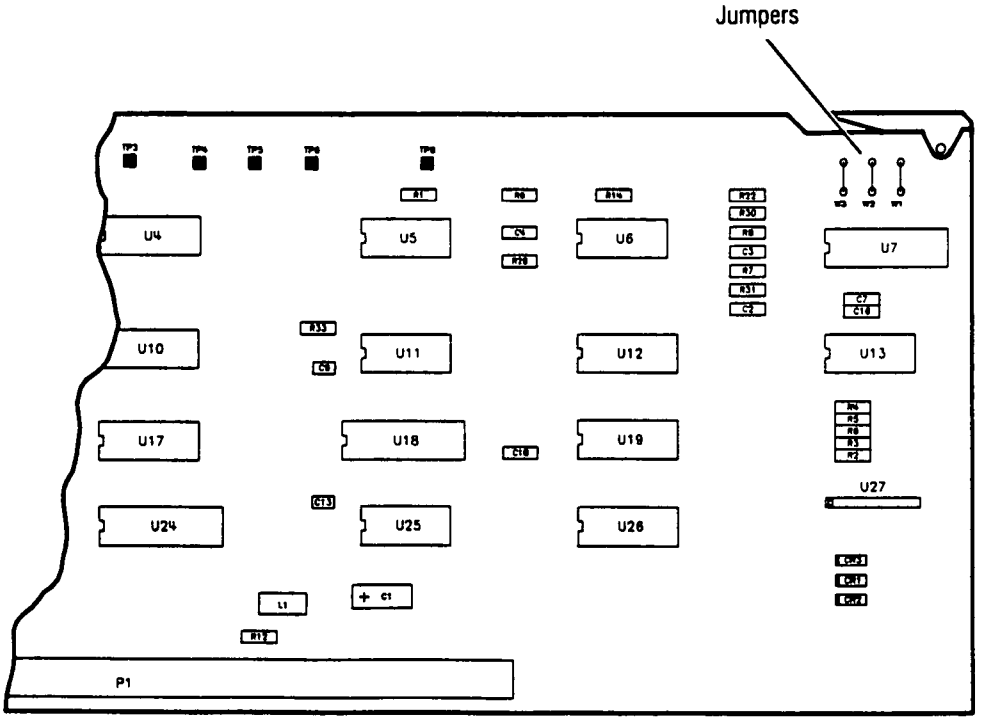


Figure 8. Jumper Locations on the A59 Digital Interface Assembly

Loading Calibration Constants into Temporary Memory

46. Connect the power cord.
    Switch the instrument to ON.
    Press **[INSTR PRESET]** twice.
    Cycle power to standby then ON.

To access the calibration constants, press:

[SHIFT] [GHz] [1] [Hz]
[SHIFT] [MHz] [1] [2] [Hz]
[SHIFT] [KHz] [2] [2] [Hz]

The ENTRY DISPLAY indicates calibration constant number 1 and its value.

47. Using the front panel keys, enter the value of calibration constant 1 from the printed copy into temporary instrument memory. To terminate the entry, press **[Hz].**

48. To advance to the next calibration constant, press the front panel STEP UP **[▲]** key. Enter the value for that calibration constant from the printed copy. Press **[Hz].**

49. Repeat step 48 for all calibration constants through constant 98 (calibration constant 99 contains the CHECKSUM, which is computed automatically each time you make an entry).

NOTE: You can use STEP UP **[▲]** or STEP DOWN **[▼]** keys to move from one calibration constant to another.

Storing Calibration Constants into Protected Memory

50. After you enter and check all the calibration constants, store them into protected memory. Press:

[SHIFT] [MHz] [1] [4] [Hz]
[SHIFT] [kHz] [5] [3] [4] [9] [Hz]

51. When CALIBRATION STORED is displayed in the ENTRY DISPLAY, press:

[INSTR PRESET]
[SHIFT] [PEAK]

52. If the A58 sweep generator assembly is 08340-60298, press:

[SHIFT] [MHz] [3] [3] [Hz]
[SHIFT] [kHz] [7] [8] [6] [5] [9] [4] [3] [1] [2] [9] [3] [Hz]

53. Activate the controller section diagnostics. Press:

[SHIFT] [M4]

This activates an instrument diagnostic and recalibrates the ADC on the A27 level control assembly. The instrument's front panel and A27 level control assembly fault annunciators turn off. If there are no other problems with the instrument, all other failure indicators are off.

54. Switch the instrument to STANDBY and then back ON. The HP-IB address and firmware revision are displayed in the ENTRY DISPLAY. Copy the firmware revision (REV) onto the printed copy of the calibration constants. Return the printed copy to its storage location in the instrument.

55. Replace the instrument's controller section cover.

Adjusting the Instrument

56. Perform the following adjustments:

    5-14 Unleveled RF Output
    5-15 ALC (ALC adjustments only)
    5-16 Leveled RF Output
    5-17 RF Output Flatness
    5-18 Pulse
    5-19 External Module Leveling

    These adjustments are located in Volume 2 of the Option 003 manual.

57. Remove the "Special Service Instructions" label located on the transformer.

Testing the Instrument

58. Perform the complete performance test procedures as indicated in Volume 2 of the Option 003 manual, or use the HP 11877A performance test software to fully test the instrument.

The *HP 8341B Option 003 Operating and Service Manual* supplied in this package contains the documentation needed to support this modified instrument. This completes the support upgrade procedure.